PROCESSING OF INTEGRATED CIRCUITS

1. Overview
2. Silicon Processing
3. Lithography
4. Layer Processing
5. IC Packaging
6. Yields in IC Processing

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1. Overview

- **Integrated Circuit (IC)** - a collection of electronic devices such as transistors, diodes, and resistors that are fabricated and electronically interconnected onto a small flat *chip* (die) of semiconductor material, resulting in 'Solid State Electronics.'
- Materials in IC:
  - Silicon(Si) - Most common due to its properties and low cost
  - Germanium (Ge)
  - Gallium Arsenide (GaAs)
- Analog
  - Operate with continuous and variable voltages.
  - Examples: Amplifiers, Oscillators, Voltage regulators
- Digital
  - Operate on signals of two discrete energy levels, 0 or 1.
  - Examples: Microprocessors and Memory devices for data storage

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Trends in IC's

- ICs are on a chip (a square or rectangular silicon plate (0.5mm thick and 5-25mm on each side)) connected by fine lines of conducting material (Al).
- IC's are categorized by size and density of devices per unit area, or integration.
- Packaging

Integration Level	# of Devices on a Chip	Yr introduced
Small Scale Integration (SSI)	10-50	1959
Medium Scale Integration (MSI)	50-10^3	1960s
Large Scale Integration (LSI)	10^3-10^4	1970s
Very large Scale Integration (VLSI)	10^4-10^6	1980s
Ultra Large Scale Integration (ULSI)	10^6-10^8	1990s
Giga Scale Integration	10^9-10^{10}	2000s

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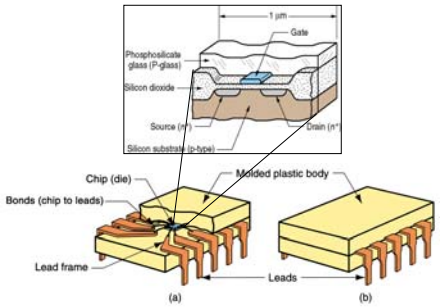
Transistor and Packaging

Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)



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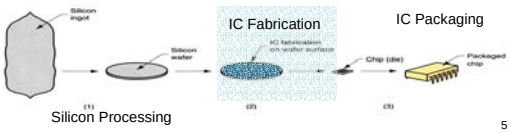
Processing Sequence Steps

A. Silicon Processing
   A. A large single crystal Silicon log (boule)
   B. Slicing into a wafer.

B. IC fabrication (Planar Process)
   A. Add (PVD & CVD), alter (Ion implantation, diffusion and thermal oxidation), remove (chemical and plasma etchants) a layer of materials in selected regions (lithography) of the wafer
   B. Finish and clean surface of wafer
   C. The processed wafer is cut into chips

C. IC Packaging.



Silicon Processing

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Clean Rooms

- Reduce free air particles through filtration, bunny suits.
- Control Humidity, Temperature.
- Control Radiation, Light filters.
- Protect from processing gases, solvents, acids and bases, organics, etc.

A number (in increments of ten) to indicate the quantity of particles of size 0.5 μm or greater in one cubic foot of air

- A *class 100* (*10)* clean room must maintain a count of particles of size 0.5 μm or greater at less than 100(10)/ft^3
- The clean room is air conditioned to 21°C (70°F) and 45% relative humidity

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2. Silicon Processing

- Production of Electron Grade Silicon (EDS)
  - Start with very pure SiO_2, quartzite
  - Submerge in an electron arc furnace with coke, coal, and wood chips to add Carbon, Heating will produce MGS (Metallurgical Grade Si) (98% pure)
    - SiO_2 + C -> MGS + SiO +CO
  - Grind MGS into a powder, react with HCL
    - MGS + 3HCl -> $SiHCl_{3\ gas}$ + $H_{2\ gas}$
  - $SiHCl_3$ will separate itself from impurities by evaporation.
    - $SiHCl_3(gas) + H_2(gas) \rightarrow Si + 3HCl(gas)$
  - Introduce more hydrogen gas to separate Si from HCl_3
  - EDS: nearly pure Si (less than 1ppb impurity).

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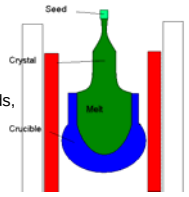
Crystal Growth

- The silicon substrate for microelectronic chips must be made of a single crystal whose unit cell is oriented in a certain direction
- Czochralski process
  - Start with a single crystal seed of known orientation.
  - Somewhere along its length will be the interface of the melt to air. In other words, melt half of it.
  - Slowly pull up into air.
  - Crucible material will reintroduce some impurities at the surface of boule.



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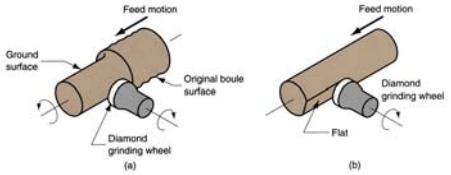
Shaping of Si into Wafers

- Ingot Preparation
  - Seed and tang ends are cut off
  - Portions that don't meet electronic specifications are removed
    - Resistivity and Crystallographic Specifications.
- Shaping by cylindrical grinding for identification, orientation and mechanical location



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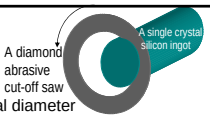
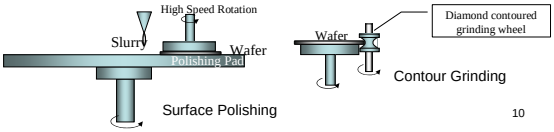
Wafer Preparation



- Thin saw blade with diamond grit on internal diameter
  - Thin saw to reduce waste of Si
  - Internal diameter cutting for better control over flatness, thickness, parallelism, surface characteristics
- Edges are rounded to reduce chipping and to minimize accumulation of photoresist at rims of wafer
- Chemical etch to create uniform surface topography and chemistry
- A flat polishing operation using a slurry of SiO_2 to prepare the surface for photolithograph
- Cleaning operation to remove residue and organic film



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3. Lithography

- An IC consists of many microscopic regions on the wafer surface that make up the transistors, devices and intraconnections imposed by the circuit design.
- In the planar process, the regions are fabricated by steps that add, alter, or remove layers in selected areas of the wafer surface
- Each layer is determined by a geometric pattern from circuit design, which is transferred to the wafer surface by *lithography*
- Photolithography
  - Uses light radiation (*ultraviolet* (UV) light) to expose a coating of photoresist on the surface of the wafer
  - A *mask* containing the required geometric pattern for each layer covers the light source from the wafer, so that only the portions of the photoresist not blocked by the mask are exposed
  - Flat plate of transparent glass (2 mm thick) onto which a PVD/CVD-coated thin film of metal(few to less than one μm thick) of mask (patterned metal, usually Cr). Created by CAD, Pattern Generator and photolithography techniques

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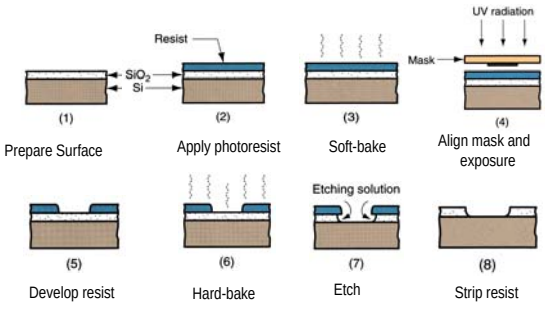
Photolithograph Processes



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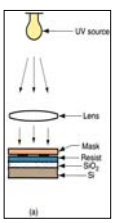
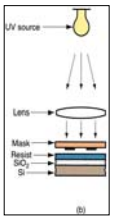
Three Exposure techniques

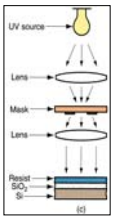
1. Contact - Wears mask, large resolution size, relatively inexpensive, high throughput
2. Proximity - No wear, large resolution size
3. Projection - No wear, high resolution, serial processing: lower throughput, must be able to focus the beam.



Contact Printing



Proximity Printing



Projection Printing

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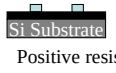
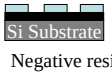
Photoresist

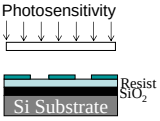
- An organic polymer polymer that is sensitive to light radiation in a certain wavelength range.
- The sensitivity causes either an increase or decrease in solubility of the polymer to certain chemicals
- Typical practice in semiconductor processing is to use photoresists sensitive to ultraviolet light. UV light has a short wavelength compared to visible light, permitting sharper imaging of microscopic circuit details
- Polymer must have good
  - Adhesion, Etch resistance, Resolution and Photosensitivity
- Positive, Negative, Image Reversal



Positive resist



Negative resist



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3.2 Other Lithography Techniques

- Electron Beam Lithography
  - Very small feature size, down to 1nm, No mask needed.
  - Costly equipment, Highly skilled user, slow.
- X-ray Beam Lithography
  - Can't focus, Must use contact or proximity methods.
  - Very small features.
- Electron & Ion Beam Lithography
  - Uses mask, can be focused.

Method	Wave Length (nm)	Finest Feature Size (nm)
UV	365	350
Deep UV	248	250
Extreme UV	10-20	30-100
X ray	0.01-1	20-100
Electron Beam	-	80

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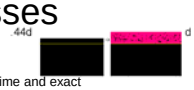
4. Layer Processes



- Thermal Oxidation
  - SiO_2 on Si acts as an insulator or a mask.
  - To grow SiO_2, expose Si to oxygen gas and heat. Time and exact temperature effect thickness.
  - The Si wafer must have .44d to get the depth, d, of SiO_2
- Chemical Vapor Deposition
  - Plasma-enhanced CVD takes place at a lower temperature.
  - Add layers of SiO_2, Si_3N_4 and Si
    - A SiO_2 layer is formed by thermal oxidation.
    - A Si_3N_4 layer is used as a masking layer.
    - Polycrystalline silicon
  - Epitaxial Deposition
    - controls the orientation of crystals
    - Vapor-phase, Liquid-phase and molecular-beam epitaxy
- Introduction of Impurities
  - Doping – adding impurities into silicon surface
    - Used to create p-n junctions that function as transistors, diodes and other devices
    - p-type – Boron
    - n-type – P(phorous), As(Arsenic), Sb(Antimony)
  - Methods
    - Thermal Diffusion
    - Ion Implantation

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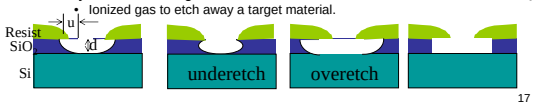
4. Layer Processes

- Metallization
  - Deposition of conductive materials
    - Form certain components
    - Provide intraconnecting conduction path
    - Connect the chip to external circuits
  - Metallization materials
    - Aluminum with Si and Cu
    - Other materials such as polisilicon, Au, refractory metals, silicides and nitrides
  - Processes – vacuum evaporation, sputtering, CVD and electroplating
- Etching Techniques
  - Material removal by etching away the unwanted materials
  - Wet Chemical Etching
    - Acid to etch away a target material
  - Dry Plasma Etching
    - Ionized gas to etch away a target material.

Degree of Anisotropy: $A = \frac{d}{u}$



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5. IC Fabrication Sequence

- Si_3N_4 mask is deposited by CVD onto the Si.
- SiO_2 insulator layer is grown in the exposed regions by thermal oxidation.
- Si_3N_4 is stripped by etching.
- Additional SiO_2 is grown on areas just exposed to act as a gate.
- Polysilicon is blanket deposited by CVD and doped n-type using ion implantation.
- Selective etch of polysilicon, remaining acts as a gate.
- Dope source and drain with As by ion implantation.
- P-glass is deposited as a protective layer on the surface by CVD.

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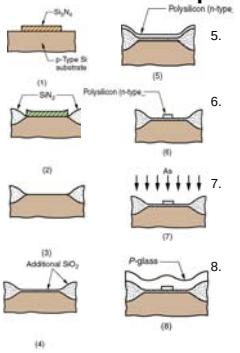
IC Fabrication sequence

1. A layer of Si_3N_4 is deposited by CVD onto Si substrate using photolithography to define the regions – the layer will serve as a mask for thermal oxidation in step (2)
2. SiO_2 is grown in exposed regions of surface by thermal oxidation. SiO_2 regions are insulating and will isolate this device from other devices
3. The Si_3N_4 mask is stripped by etching
4. Another thermal oxidation to add a thin gate oxide layer to previously uncoated surfaces and to increase thickness of previous SiO_2 layer



5. Polysilicon is deposited by CVD onto surface and then doped n-type using ion implantation
6. The polysilicon is selectively etched using photolithography to form gate electrode of transistor
7. The polysilicon is selectively etched using photolithography to form gate electrode of transistor
8. Phosphosilicate glass (P-glass) is deposited onto the surface by CVD to protect the circuitry beneath

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6. Packaging Manufacturing

The final series of operations to transform the wafer into individual chips, ready to connect to external circuits and prepared to withstand the harsh environment of the world outside the clean room

- Design Issues
  - Electrical connections to external circuits
  - Materials to encase chip and protect it from the environment (humidity, corrosion, temperature, vibration, mechanical shock)
  - Heat dissipation
  - Performance, reliability, and service life
  - Cost
- Manufacturing Issues
  - Chip separation.
  - Connecting the chip to the package.
  - Encapsulating the chip.
  - Circuit testing.
- Materials – Ceramics and Plastics

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Packaging Considerations

Rent's Rule:

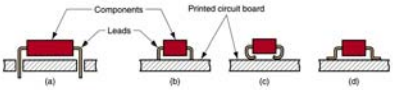
Determine the number of Input/Output leads.

$n_{io} = cn_c^m$

where n_{io} = # I/O leads required

n_c = # of devices in the IC

c, m = 4.5, 0.5 for modern VLSI



(a) through-hole, and several styles of surface mount technology: (b) butt lead, (c) "J" lead, and (d) gull-wing

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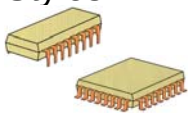
Major IC Package Styles

- Dual in-line package (DIP)
  - the most common form, available in both through-hole and surface mount configurations
- Square package
  - Leads are arranged around periphery so that number of terminals on a side is $n_{io}/4$
- Pin grid array
  - Two dimensional array of pin terminals on underside of a square chip enclosure
  - Square matrix of pins maximizes number of leads on a package
  - Entire bottom surface of package, except center area of package with no pins due to IC chip, is fully occupied by pins, so pin count in each direction is square root of n_{io}
    - Some of these are available in both through-hole and surface mount styles, while others are designed for only one mounting method



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Processing Steps

1. Wafer testing - test chips while they are still part of the wafer using a multiprobe.
2. Chip separation using a thin, diamond tipped saw. Adhesive tape holds individual chips in place during and after sawing
3. Die bonding - attach chips to the package by bonding with metal or epoxy.
   1. Eutectic die bonding – for ceramic packages
   2. Epoxy die bonding – for plastic packages
4. Wire bonding - connect chip to package leads using a wire deposited by thermocompression, thermsonic, or ultrasonic bonding.
5. Package sealing
   1. Ceramics (Alumina) –Hermeticaly sealed, lamination by pressing and sintering
   2. Plastics (epoxies, polyimides, and silicones) – Cost effective, postmolded or premolded.
6. Final Test
   – Determine which units, if any, have been damaged during packaging
   – Measure performance characteristics of each device

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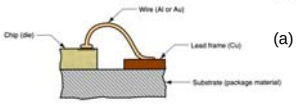
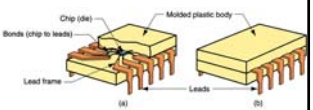
Wire Bonding

- Ultrasonic Bonding
- Thermocompression Bonding
- Thermosonic Bonding

After die is bonded to package, electrical connections are made between contact pads on chip surface and package lead frame using small diameter wires



Packaging of an integrated circuit chip



(a) cutaway view showing the chip attached to a lead frame and encapsulated in a plastic enclosure

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7. Yields in IC Processing

- Fabrication of ICs consists of many processing steps performed in sequence
- At each step, a chance that something may go wrong results in the loss of the wafer or portions of it corresponding to individual chips
- A simple probability model to predict the final yield of good product is:

$$Y = Y_c Y_s Y_w Y_m Y_t$$

  - *Crystal yield Yc* - material in boule relative to starting amount of electronic grade silicon: *Yc* ~ 50%
  - *Crystal-to-slice yield Ys* - material left after grinding boule and sawing into wafers (kerf losses): *Ys* ~ 50%
  - *Wafer yield Yw* - wafers surviving processing relative to starting quantity: *Yw* ~ 70%
  - *Multiprobe yield Ym* – proportion passing multiprobe test: *Ym* < 10% to *Ym* > 90%
  - *Final test yield Yt* – proportion to pass final test after packaging: *Yt* = 90% to 95%

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Electronics Assembly and Packaging

1. Electronic Packaging
2. Printed Circuit Board (PCB)
3. PCB Assembly
4. Surface Mounting Technology
5. Electrical Connector Technology

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1. Electronics Packaging

The physical means by which components in a system are electrically interconnected and interfaced to external devices; it includes the mechanical structure that holds and protects the circuitry

- Functions of a well-designed electronics package:
  - Power distribution and signal interconnection
  - Structural support
  - Protection from physical and chemical hazards
  - Heat dissipation
  - Minimize delays in signal transmission

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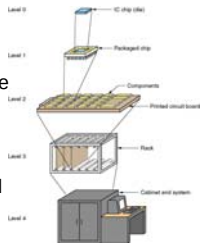
Levels in the Packaging Hierarchy

Level	Description of interconnection
0	Intraconnections on the chip
1	Chip to package interconnections to form IC package (e.g., dual in-line package)
2	IC package to circuit board interconnections
3	Circuit board to rack; card-on-board packaging
4	Wiring and cabling connections in cabinet



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Level 0 Packaging Materials

- Semiconductor Materials
  - Silicon (Si), Gallium Arsenide (GaAs), Hydrogenated amorphous silicon (a-Si-H)
  - $Al_xGa_{1-x}As$, $In_y(Al_xGa_{1-x})_{1-y}P$, Germanium (Ge), Si-Ge alloys
  - Wide-bandgap semiconductor, Tellurides, Diamonds
- Attachment Materials
  - Si, Polyurethane, Arcylic, Epoxynovolak, Phenolic, Bisphenol A, Polyimide
- Substrate Materials
  - Various ceramics – BeO, SiC, AlN, Si, Si3N4, SiO2, Al2O3, Diamond, Quartz, Steatite, Forsterite, Titanate, Cordierite, Mullite
  - Molydenum, Cu:W, Tunsten, Kovar

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2. Printed Circuit Boards (PCB)

- One or more thin sheets of insulating material with thin copper lines on one or both surfaces that interconnect the components attached to the board to each other.
- Advantages:
  - Provide a convenient structural platform.
  - Mass production of PCB's can be consistent.
  - Soldering of PCB's can be completed in one step.
  - Have reliable performance.
  - Can be removed from work system and serviced separately

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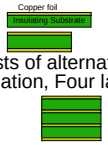
Structures, Types and Materials

- Insulating Materials Structure
  - Polymer composites reinforced with E-glass.
  - Substrate layer thickness = 0.8 to 3.2 mm
- Material Properties - electrically insulating, strong and rigid, resistant to warpage, flame retardant.
- Copper foil thickness is ~ 0.04 mm
- 3 types
  - Single sided board
  - Double sided board
  - Multilayer board - consists of alternating layers of conducting foil and insulation, Four layer board most common



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Production

- Starting Board
  - Press multiple sheets of woven glass fiber that are impregnated with epoxy.
  - Place **Cu foil** on one or both sides of laminate stack. If it is to be single sided, a thin release film will be placed on one side.
  - Heat and pressure are applied by a hydraulic press.
  - Cool and trim.
- Copper Foil - Produced by continuous electroforming, in which a rotating smooth metal drum is partially submersed in an electrolytic bath containing copper ions
  - The drum is the cathode, causing the copper to plate onto its surface
  - As the drum rotates out of the bath, the thin copper foil is peeled.
- Completed Board - Consists of a glass fabric reinforced thermoset panel with copper over its surface on one or both sides
  - Usually produced in large standard widths designed to match the board handling systems in PCB processing and assembly equipment
  - For a smaller size, several units can be processed together on the same larger board and then separated later

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Circuit Fabricator Processes

- The circuit fabricator employs a variety of processes to produce a finished printed circuit board, ready for assembly of components
  - Operations include cleaning, shearing, hole drilling or punching, pattern imaging, etching, and electroless and electrolytic plating
  - Some operations must be performed under clean room conditions, especially for boards with fine tracks and details

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Processes in PCB Fabrication

- Board Preparation
  - Shearing, hole-making, and other shaping operations to create tabs, slots, and similar features
  - The holes, called *tooling holes*, are made by drilling or punching
  - Bar coded for identification
  - cleaning to remove dirt and grease from board surface
- Hole Making
  - Mostly drilled but sometimes punched, using the tooling holes for location
    - Drilled holes using standard twist drills are cleaner, but punching is faster
    - Most holes in PCB fabrication are drilled
  - For high production jobs, a stack of three or four panels may be drilled together or multiple spindle drills are sometimes used
  - Functional Holes:
    - *Insertion holes* for insertion of component leads
    - *Via holes* - to be copper-plated and used as conducting paths between two sides of the board
    - To fasten certain components such as heat sinks and connectors to the board
- Circuit Pattern Imaging and Etching
- Plating

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Circuit Pattern Imaging & Etching

- Two basic methods to transfer circuit pattern to the copper surface of the board
  1. Screen printing
  2. Photolithography
- Both methods use a resist coating on the board surface to determine where etching of the copper will occur to create the tracks and lands of the circuit
  - Covered areas = circuit tracks and lands
  - Uncovered areas = open regions between them
- *Etching* is used to remove the copper cladding in the unprotected regions from the board surface, usually by means of a chemical etchant
  - Transforms solid copper film into interconnections for an electrical circuit

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Plating

- Plating is needed on hole surfaces for conductive paths from one side to the other in double-sided boards, or between layers in multilayer boards
- Two plating processes used in PCB fabrication:
  1. Electroplating - higher deposition rate but coated surface must be metallic (conductive)
  2. Electroless plating - slower but does not require a conductive surface

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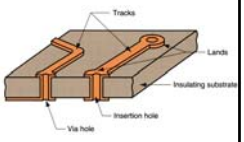
PCB Fabrication

- Circuitization
  - The sequence of transforming a copper-clad board of reinforced polymer into PCB
  - Subtractive, additive and semi-additive methods
- Processing of different board types
  - Single-sided board
  - Double-sided board
  - Multilayer board
- Processes of Single-sided board
  - Cut to size, tooling hole & clean
  - Photoresist
  - Expose to UV
  - Resist developed
  - Etching
  - Strip remaining resist
  - Lead hole making



Double-sided board

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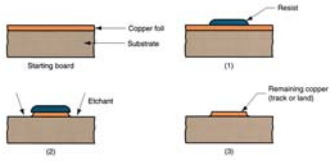
Subtractive Circuitization Method

- Open portions of copper cladding on starting board are etched away from surface, so that tracks and lands of desired circuit remain.

(1) apply resist to areas not to be etched, using photolithography to expose the areas that are to be etched, (2) etch, and (3) strip resist



See Additive and Semi-additive Methods in Textbook

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Testing and Finishing

- After fabricated on the board surface, it must be inspected and tested for its functions and quality.
- Two procedures are common:
  1. *Visual inspection* - by human eye or machine vision to detect open/short circuits, errors in hole locations, and other faults
  2. *Continuity testing* - use of contact probes brought simultaneously into contact with tracks and lands on board surface
- Apply a thin solder layer on tracks and lands to protect the copper from oxidation and contamination.
- Apply solder resist to all areas except lands, which will be soldered during assembly.
- An identification legend is printed.

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3. PCB Assembly

Electronic (e.g., IC packages, resistors, capacitors) and mechanical components (e.g., fasteners, heat sinks) mounted on a PCB

- *Level two* in electronic packaging
- PCB assembly is based on either
  1. Pin-in-hole (PIH) technology
  2. Surface mount technology (SMT)
  - Some include both leaded and surface mounted components
- Insertion - Hundreds of components to be inserted into the board (PIH)
  - Mostly by automatic insertion machines and a small proportion (perhaps 5% to 10%) by hand for nonstandard components.
- Onsertion - Components are placed onto board surface after adhesive application by automatic placement machines (SMT)
  - Place up to 4 components per second

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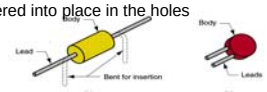
Pin-In-Hole (PIH) Technology

Processing of PCB assemblies with leaded components:

1. Component insertion – insertion of leads into through-holes
2. Soldering - leads are soldered into place in the holes
3. Cleaning
4. Testing
5. Rework



Automatic Insertion Machines - perform component insertion either semi-automatically (position controlled by a human operator) or fully automatically (controlled by a program prepared directly from circuit design data)

- In Automatic insertion machines, components are loaded into these machines in the form of reels, magazines, or other

Manual Insertion - typically for a nonstandard configuration such as switches, connectors, resistors, capacitors and other components

- High cost due to much lower production

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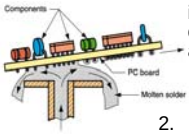
Soldering



1. Wave soldering - Mechanized technique in which PCBs containing inserted components are moved by conveyor over a standing wave of molten solder
   - Use the combination of capillary action and upward force of wave
   - All solder joints are made in a single pass
2. Hand soldering - Skilled operator using soldering iron makes the circuit connections
   - Slow since each joint is made one at a time
   - Generally for small lot production and rework
   - Prone to human error
   - Sometimes used after wave soldering to add delicate components that would be damaged in the wave soldering chamber

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Cleaning, Testing, and Rework

- *Cleaning* - hand cleaning with appropriate solvents and vapor degreasing to remove flux, oil and grease, salts, and dirt
- *Inspection and Testing*:
  - Visual inspection to detect missing or damaged components, soldering faults, etc.
  - Functional tests to insure proper circuit operation
- *Rework* - manual repair of defects found in inspection and/or testing

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Surface Mount Technology (SMT)

Component leads are soldered to lands on PCB surface rather than into holes running through the board

- Inherent limitations of PIH in terms of packing density
  - mounted on only one side of board
  - Relatively large center-to-center distances between lead pins
- Advantages of SMT
  - Increased packing densities
  - Require only 20% to 60% of board surface compared to PIH
  - Mounted on both sides of board
  - No drilling of many through holes
- Component Placement - Correctly positioning component on PCB and affixing it sufficiently until soldering provides a permanent connection
  1. *Adhesive bonding* and *wave soldering*
  2. *Reflow soldering*
  3. Combined SMT-PIH Assembly
- Certain types of SMT components are more suited to one method or the other

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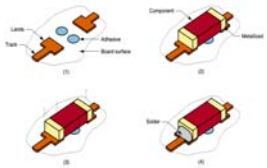
Adhesive Bonding and Wave Soldering

- Adhesive bond-fixes components to the surface until soldering attaches them permanently.
  - Brush liquid adhesive through a stencil.
  - Automatic dispensing machine using x-y positioning.
  - Pin transfer method.
- Cure Adhesive
- Wave Solder



(1) adhesive is applied to areas on the board where component will be placed;
(2) component is placed onto adhesive-coated areas;
(3) adhesive is cured; and
(4) solder joints are made by wave soldering

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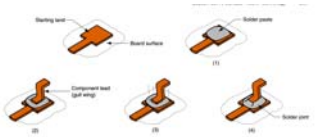
Reflow Soldering

Solder paste = suspension of solder powders in a flux binder

- Three functions:
  1. the *solder* - 80% to 90% of total paste volume
  2. the *flux*
  3. the *adhesive* to secure components to the board surface
- Methods of applying solder paste to board surface include *screen printing* and *syringe dispensing*



(1) apply solder paste
(2) place components onto board,
(3) bake paste, and
(4) solder reflow

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Cleaning, Inspection, Testing and Rework

- Difficult due to smaller component size and increased density.
- SMT Inspection
  - More difficult due to denser packing, smaller solder joints, and different joint geometries than PIH assemblies
  - In SMT assembly, components are held by adhesive or paste
    - During soldering this method is not as secure as PIH, and component shifting can occur
  - Another problem with smaller sizes is greater likelihood of solder bridges forming between adjacent leads, resulting in short circuits
- SMT Circuit Testing
  - Smaller scale also poses problems in circuit testing because of less space around each component. Contact probes must be physically smaller and more probes are required because SMT assemblies are more densely populated
  - One way of dealing with this issue is to design the circuit layout with extra lands whose only purpose is to provide a test probe contact site
    - Dilemma: this runs counter to the goal of higher packing densities

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4. Electrical Connector Technology

- Printed circuit board assemblies must be connected to back planes, and into racks and cabinets, which must be connected to other cabinets and systems using cables
- The performance of any electronic system depends on the reliability of the individual connections
- Connector technology is usually applied at the third and fourth levels of electronics packaging
- Two Basic Connection Methods
  1. *Soldering* - most widely used technology in electronics
  2. *Pressure connections* - electrical connections in which mechanical forces establish electrical continuity between components
     - *Permanent* or *Separable solderless* connections.

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Permanent Connections

- High-pressure contact between two metal surfaces, in which one or both of the parts is mechanically deformed during the assembly process
- Permanent connection methods include:
  - Crimping of connector terminals
    - Mechanically deforming the terminal barrel to form a permanent connection with the stripped end of a wire inserted into it by hand tools or by crimping machines
  - Insulation displacement
    - Permanent connection method in which a sharp, prong-shaped contact pierces the insulation and squeezes against the wire conductor to form an electrical connection

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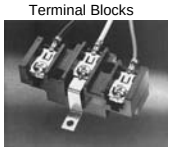
Separable Connectors

Electrical connectors designed to permit disassembly and reassembly multiple times

- When connected, metal-to-metal contact between mating components with high reliability and low electrical resistance
- Typically consist of multiple contacts contained in a plastic molded housing, designed to mate with a compatible connector or with individual wires or terminals

Cable Connectors

Terminal Blocks



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