Switched-Capacitor Bidirectional Voltage Buck-Boost dc-ac Converter with Single SiC Leg

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Abstract—This article presents a switched-capacitor (SC) bidirectional voltage buck-boost converter for implementing dc-ac and ac-dc power conversion. The SC converter employs a SiC switched-capacitor circuit augmented with the main Si converter circuit to the power source. It is thus providing unique features that cannot be attained by the traditional voltage-source inverter (VSI) or boost VSI. The additional features include doubling the area of the linear modulation region, eliminating both the large inductor in the boost dc-de stage and the large filtering capacitor. The SiC leg operate at a switching frequency higher than the switching frequency of the Si inverter legs. Thus high efficiency can be attained with maintaining the charging current of the switched-capacitor under control. To describe the operating principle, we focus on one example: a bidirectional SC converter for dc-ac and ac-dc power conversion in electric and hybrid electric vehicles.

I. INTRODUCTION

VSIs are inherently buck converters. Therefore, the dc-link voltage has to be higher than the dc or ac input voltage. For applications where the available dc voltage is limited, an additional dc-de boost converter is needed to obtain the desirable ac voltage [1]. For the commercial traction electric drive, the battery connected to the inverter with an intermediate dc-de boost stage. The boost stage typically includes an inductor. The inductor size is proportional to the battery size. At high currents, the inductor losses render the entire drive system less efficient. In [2], we recently proposed a unique circuitry that overrides the need for an inductor by using a switched-capacitor circuit augmented to the main converter, as shown in Fig. 1. In the first version of the SC converter, Si-based switches were used. One of the interesting findings in [2] was that the negative proportional relationship between the charging current and the switching frequency of the SC converter.

\[ \Delta V_{\text{max}} = \frac{3AM_i\bar{I}}{4CF_{\text{sw}}} \]

Therefore, to limit the charging current or in another objective, reduce the size requirement of the switched-capacitors, the operating switching frequency has to be increased. In this paper, we propose a new SVPWM method that enables increasing the switching frequency of the switched-capacitor circuit without increasing the switching frequency of the inverter legs. To achieve this type of operation, the switched-capacitor circuit is replaced with SiC switches. As it is known, SiC switches are able to turn-on and turn-off at higher speed with results in less switching losses. Since the inverter legs remain operating at the same lower switching frequency, Si-based switches are used. The main advantage of this structure is to achieve higher power density without relying totally on the expensive SiC switches.

II. MODIFIED SPACE VECTOR PULSE WIDTH MODULATION OF SC CONVERTER

The switched-capacitor circuit at Fig. 1 can have two possible states: one when the capacitor is charging

\[ V_{\text{bat}} = v_{\text{cap}} = v_i, \]  

and one when the capacitor is discharging

\[ V_{\text{bat}} = v_{\text{cap}}; \quad v_i = 2V_{\text{bat}}, \]

\[ i_i = S_a i_a + S_b i_b + S_c i_c. \]

In addition to these options, the other phase legs feature the eight known inverter states. There are fourteen overall feasible states in the SC converter, and they are depicted in the space vector hexagon shown in Fig. 2. One can observe that the
states of the SC converter resemble a four-level inverter with phase voltage possibilities \( \{ \pm V_{bat}, \pm 2V_{bat} \} \).

To derive the dwell time for each vector, a few assumptions are made. First, in each sector, the four adjacent active vectors and the two zero vectors are used to synthesize the reference voltage vector. Second, during the discharge time, the capacitor voltage is assumed to be constant and equal to the battery voltage. Therefore, the dwell time during the discharge time needs to be minimized to allow minimum voltage drop during the capacitor discharge.

Assume that the reference voltage vector \( V_{ref} \) can be synthesized using the following virtual vectors:

\[
V_{ref}T_x = V_x t_x + V_y t_y + V_0 t_0
\]

where

\[
V_x t_x = V_{11} t_{11} + V_{12} t_{12}
\]

and

\[
V_y t_y = V_{21} t_{21} + V_{22} t_{22}
\]

With some algebraic manipulation, the following dwell time for the four active vectors can be obtained:

\[
t_{11} = (1 - A) t_x
\]

\[
t_{12} = At_x
\]

where

\[
t_x = \sqrt{3} T_s M_i \sin \left( \frac{\pi}{3} - \theta \right)
\]

and

\[
t_{21} = (1 - A) t_y
\]

\[
t_{22} = At_y
\]

where

\[
t_y = \sqrt{3} T_s M_i \sin \theta.
\]

The factor \( A \in [0, 1] \) is the boost factor and is expressed as follows:

\[
A = \begin{cases} 
0, & 0 \leq M_i \leq \frac{1}{\sqrt{3}} \\
\sqrt{3} M_i - 1, & \frac{1}{\sqrt{3}} < M_i \leq \frac{2}{\sqrt{3}}
\end{cases}
\]

where the modulation \( M_i \) is defined as

\[
M_i = \frac{|V_{ref}|}{V_{bat}}.
\]

From this result, it is easy to see that when the modulation index \( M_i \leq \frac{1}{\sqrt{3}} \), \( t_{11} = t_x \), \( t_{21} = t_y \) and \( t_{12} = t_{22} = 0 \). The capacitor is maintained in parallel with the dc source, and no discharge occurs at any time. The SC converter operation in this case is identical to the operation of a conventional two-level inverter. The authors refer to this operation mode as abstemious mode.

On the other hand, when \( \frac{1}{\sqrt{3}} < M_i \leq \frac{2}{\sqrt{3}} \), then \( 0 < A \leq 1 \), and the capacitor is charged and discharged with a rate proportional to the value of \( A \). The authors refer to this operation mode as gluttonous mode.

When \( M_i = \frac{2}{\sqrt{3}} \), \( t_{11} = t_{21} = 0 \), \( t_{12} = t_x \), \( t_{22} = t_y \). In this case, the capacitors are only charged during the zero vector implementation. Therefore, the six-step operation cannot be performed in the gluttonous mode, and the minimum zero vector time must be ensured to maintain the capacitor charge level.

The same rules in (10) and (13) can be applied for calculating the dwell times of the vectors in sectors II to VI if modified \( \theta_k \) for the \( k \)th sector is used instead of \( \theta \) used in the calculations.

\[
\theta_k = \theta - (k - 1) \frac{\pi}{3}.
\]

The space vector sequence should assure that the load line voltage has the quarter-wave symmetry to reduce the even harmonics in their spectra. To reduce the switching frequency, it is also necessary to execute the switching sequence in such a way that the transition from one to the next is performed by switching only one inverter leg at a time. For instance, if the reference vector falls in sector I, the switching sequence is shown in Fig. 3. The capacitor discharge intervals are placed...
in the middle of the active vectors intervals to maintain the switching of only one inverter leg at a time.

III. SIMULATION AND EXPERIMENTAL RESULTS

To verify the proposed method, a simulation model of the SC converter is built using Simulink simulation software. Fig. 1 shows the circuit configuration and Fig. 4 shows the simulation results of the SC converter using the conventional SVPWM proposed in [2]. The switched-capacitor network switches at a minimal switching rate resulting in a higher value of voltage drop across the capacitor, which corresponds directly to higher discharge current. On the other hand, Fig. 5 shows the simulation results using the modified SVPWM, where the switched-capacitor network switches at higher switching frequency resulting in a lower voltage drop across the capacitor and therefore, less value of the charging current and the input inverter current. Fig. 8 shows the experimental results of the SC converter using the modified SVPWM method. Note that for both simulation and experimental results, the battery voltage is set to 200 V and the boost ratio $A = 0.5$. In this case, the maximum voltage experienced be the DC-link is 400 V.

IV. CONCLUSION

This paper has presented a modified SVPWM to control the switched-capacitor power converter (SC) for implementing dc-ac power conversion. The SC converter employs a switched-capacitor circuit augmented with the main converter circuit to the power source, thus providing unique features that cannot be attained by the traditional VSI or boost VSI. One of these unique features is doubling the area of the linear modulation region. The modified SVPWM method allows increasing the switching frequency of the switched-capacitor network resulting in a lower voltage drop across the capacitor. To balance the switching losses in the converter, SiC switches are used from the switched-capacitor networks, and Si-based switches are used for the three inverter legs. The structure allows achieving the high switching frequency capabilities without increasing the cost of the converter.

The SC converter eliminates the need for the cumbersome and costly inductor to boost the voltage. Instead, it relies on only the capacitor to achieve the voltage boost, which allows higher power density.

The simulation and experimental results have validated the operating principle and modulation methods of the proposed
 converter. The SC converter can boost or buck voltage, minimize component count, increase power density, and reduce cost.

REFERENCES


Fig. 6: Simulation results of the modified SVPWM-3X method of the SC converter.

Fig. 7: Simulation results of the modified SVPWM-4X method of the SC converter.

Fig. 8: Experimental results of the modified SVPWM method of the SC converter.