Poly-Diamond Gated Field-Emitter Display Cells

D. Hong and D. M. Aslam

***Abstract*—A microchip containing gated field-emitter display (FED) cells is designed and fabricated using vapor-deposited p-type polycrystalline diamond films and employing an integrated circuit (IC)-compatible diamond film technology on oxidized 4-in Si wafers. Current–voltage ($I-V$) data, measured in a diode configuration at 10^{-6} torr, show Fowler–Nordheim (F–N) field emission behavior. A 1 $\times$ 4 pixel diamond gated display cell is demonstrated for the first time using phosphor-coated glass as an anode.**

***Index Terms*—CVD diamond films, diamond technology, field emission display.**

I. Introduction

A growing need for developing low-cost and high-performance flat-panel displays has spurred a strong research effort in field-emission display (FED) technology. A 6-in diagonal color prototype FED [1] was demonstrated using the Spindt-type [2] microtip metal field emitters. For this type of FED, it is necessary to fabricate micron-sized microtips and grids over large area panels, which results in a high cost. In addition, the use of sulfide-based color phosphors is a potential problem due to contamination of metal tip from loose phosphor powder particles.

Due to its chemical inertness and negative electron affinity [3], diamond is an excellent field-emitter material. The chemical vapor deposition (CVD) of inexpensive polycrystalline diamond (poly-diamond) films [4], [5] has led to a great interest in the use of CVD diamond as a preferred field-emitter material [6]. Although a black and white 1-in diagonal prototype FED was demonstrated in a diode configuration using amorphous diamond as the emitter material [7], its further development has been hindered due primarily to relatively high switching voltage and lack of a technology compatible with integrated circuit (IC) fabrication.

In this paper, we report for the first time the fabrication and testing of a poly-diamond microchip containing gated FED cells. The development of FED chip was possible due to our earlier field emission study [8] and development of IC-compatible diamond-film technology [9], [10]. The emitter threshold fields and the gate switching voltages are in the ranges of 0.07–0.2 MV/cm and 20–100 V, respectively. A successful operation of a 1×4 pixel FED was confirmed using a phosphor-coated glass anode.

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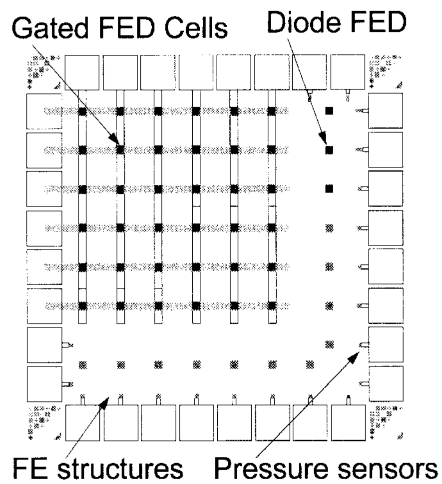


Fig. 1. Overview of the field emission display test chip.

II. Sample Fabrication

An overview of a testchip containing a number of device structures including a gated 6×6 FED array is shown in Fig. 1. The details of other structures shown on the chip are reported elsewhere [9], [11]. A four mask fabrication process used for the fabrication of the gated FED is depicted in Fig. 2. Positive photoresist mixed with diamond powder having an average particle size of 0.1 μm [12], [13] is spin-coated and patterned using a standard lithographic process. The sample is then heated to 900 °C resulting in evaporation of photoresist leaving behind the diamond particles which act as seeds for diamond growth in a hot filament CVD (HFCVD) reactor [10], [12], [13]. The *in situ* doping of an approximately 1-μm thick diamond film is accomplished using pure boron powder which is heated to 900 °C. The film resistivity, as measured by the four-point probe method, is approximately 27 Ω cm. A lower diamond quality (small grains and low sp^3/sp^2 ratio), as monitored by scanning electron microscopy (SEM) and Raman spectroscopy, was used as the emitter material. Such a lower quality film was found to result in higher current density in another study [9].

Approximately 200-nm thick Cr is thermally evaporated and patterned to serve as the cathode contact, as shown in Fig. 2(b). As indicated in Fig. 2(c), approximately half of the Cr thickness is etched away uniformly; as a result, some parts of the diamond film are exposed due to its rough surface. Pure photoresist is now spin-coated at a spin speed of 1000 r/min to produce a 2-μm thick resist layer and pattern, as seen in Fig. 2(d). Finally, a layer of Al is evaporated and patterned, and the sacrificial photoresist layer is removed, as shown in Fig. 2(e) and (f).

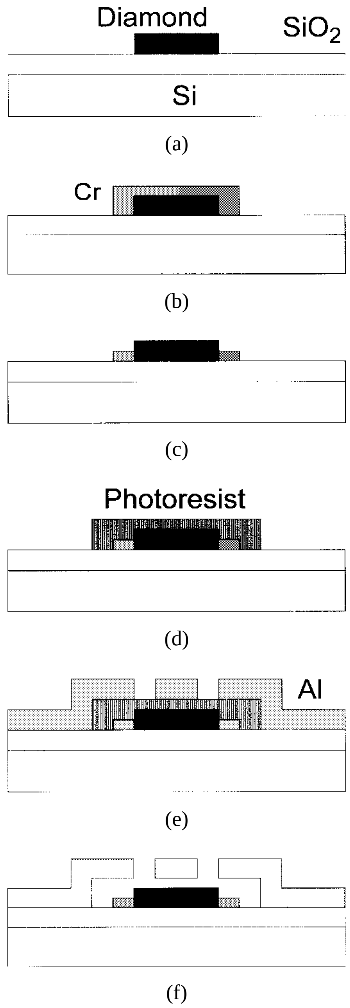


Fig. 2. Gated FED cell fabrication.

The diamond emitter area depicted by the SEM micrograph shown in Fig. 3(a), which corresponds to Fig. 2(a), consists of either an array of diamond dots or a continuous film. In the 6×6 FED shown in Fig. 1, the array size is varied from 2×2 to 15×15 dots to study 1) the effect of patterning on the emitter current [9] and 2) the process development. It may be pointed out that the number of stray diamond particles found in undesired areas in Fig. 3(b) is larger than that shown in Fig. 3(a). These stray particles are due to remaining diamond particles, which are not washed away completely during the development process of the diamond-loaded photoresist. They can affect the yield if they form a continuous film or if their size becomes too large. A double-layer process was developed to suppress the diamond particles in undesired areas. The earlier patterning method [13] and the double-layer modification are shown in Fig. 4(a) and (b), respectively. In the double-layer process, the presence of a pure photoresist layer reduces the number of diamond particles, making a direct contact with the substrate during the photoresist development process. The efficacy of the double-layer method is obvious from the SEM micrographs shown in Fig. 3(a).

The separation between the Al grid and the diamond emitter is approximately 2 μm. Al is also evaporated on part of the Cr pattern to serve as a cathode contact. The completed samples are annealed at 400 °C in N_2 ambient for 30 min using a rapid thermal processor. It may be pointed out that the cross-sectional view shown in Fig. 2(f) has only two holes in the Al layer. Actually, it typically has a 15×15 array of 4×4 μm^2 holes, as shown in Fig. 3(b), to permit the electron supply to the anode.

As the grid structure hangs over the entire emitter area and is kept at a positive potential, the grid current was equal to or larger than the anode current. To reduce the grid current, we developed a self-aligned grid structure using spin-on-glass (SOG) as the insulator between the grid and the emitter, as shown in Fig. 5. A patterned diamond emitter structure is deposited on an oxidized Si wafer. A layer of SOG (Emulsitone's Silicafilm 10 000) is spin-deposited and treated at 200 °C for 15 min follwed by annealing at 450 °C for 60 min in air to obtain a final thickness of approximately 3 μm. A Cr film is then evaporated and patterned to etch holes with a diameter of 200 μm. Finally, a bigger hole is etched in SOG to produce the final structure shown in Fig. 5. As discussed in the next section, this new structure reduced the grid current substantially.

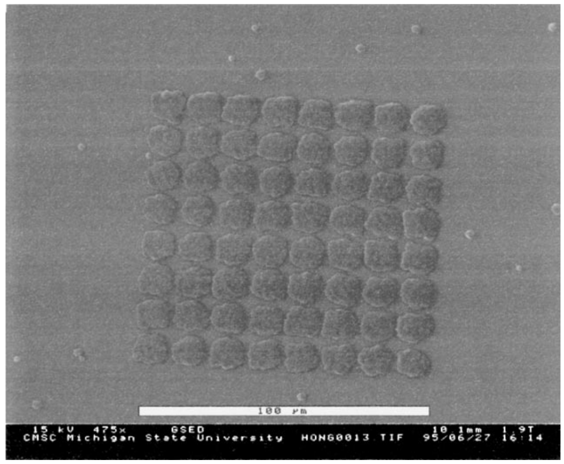
III. Test and Discussions

A. I–V Data

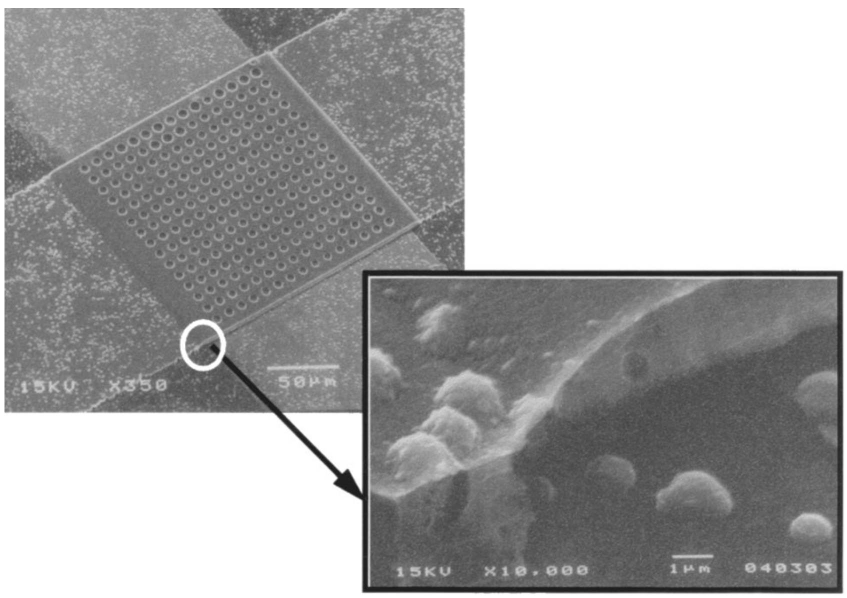
The field-emitter test devices located on the FED microchip were characterized by the current–voltage (I-V) measurements in a diode configuration using the setup shown in Fig. 6(a). As evident from Fig. 6 (b), the I-V data measured at 10^{-6} torr indicate a threshold voltage of approximately 20 V leading to an emission field in the range of 0.07–0.1 MV cm^{-1}. The inset of Fig. 6(b) demonstrates a typical Fowler–Nordheim (F–N) field emission behavior (I/V^2 – $1/V$ plot is a straight line). The current density measured at 0.2 MV cm^{-1} is approximately 0.1 A cm^{-2}, which is comparable to values reported in the literature. As compared to the switching voltage of several hundred volts used in the prototype diamond diode FED [7], a gate voltage in the range of 20–100 V was enough to control the field emission in our gated FED structure, as discussed in the next section.

B. FED Cell Testing

A glass plate coated with indium tin oxide (ITO) and ZnO : Zn phosphor was used as an anode to test the light emission behavior of the gated FED cells. A quartz spacer with a thickness of 0.15 or 1 mm was used between the anode plate and the wafer containing the FED cells. Using the grid and anode potentials of 100 and 500 V, respectively, and the setup shown in Fig. 7(a), a light emission pattern with a diameter of approximately 1 mm, as shown in Fig. 7(b), was observed at 10^{-6} torr in a vacuum chamber. An emission pattern of an array of 1×4 pixels is shown in Fig. 8. In contrast to the four holes shown in the schematics of Fig. 8(a), the actual number of holes in the Al grid for every pixel is 225. Although the gated diamond FED cells have been demonstrated successfully, the yield was below 5% and the grid current was equal to or larger than the anode current.

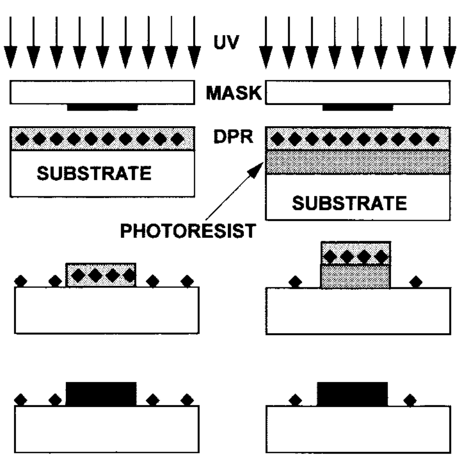


(a)



(b)

Fig. 3. SEM micrographs corresponding to Fig. 2(a) and (f).



(a) (b)

Fig. 4. Comparison of (a) conventional patterning method and (b) double-layer method. DPR stand for diamond-loaded photoresist.

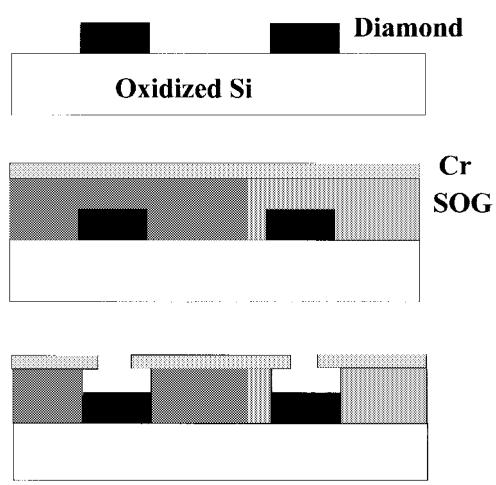


Fig. 5. Fabrication process for a self-aligned FED using SOG as the insulator.

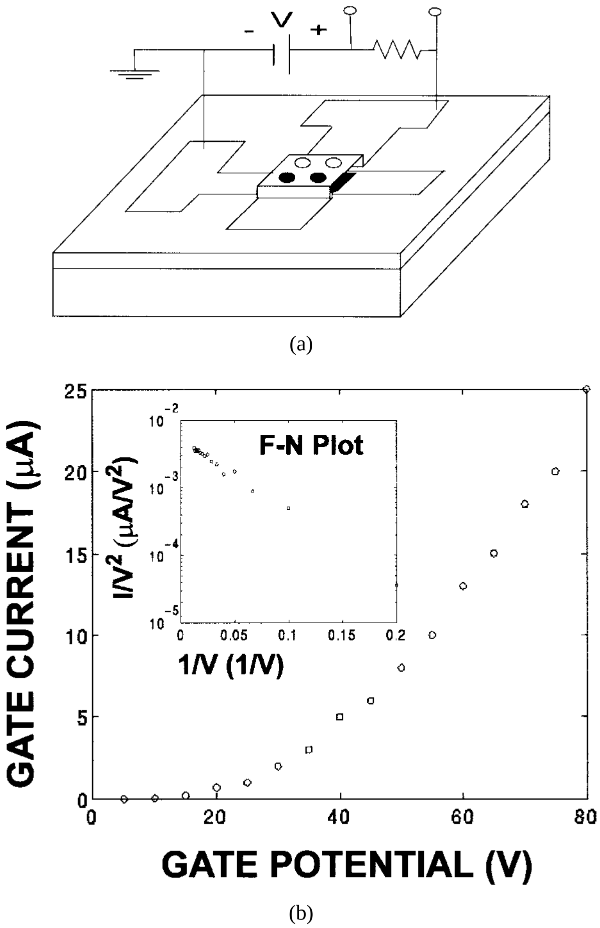
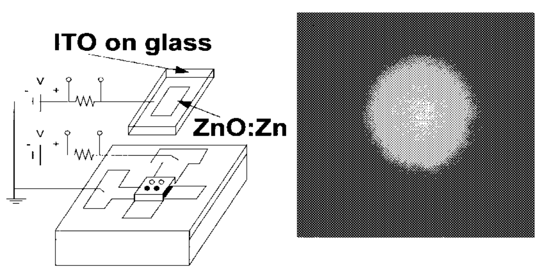


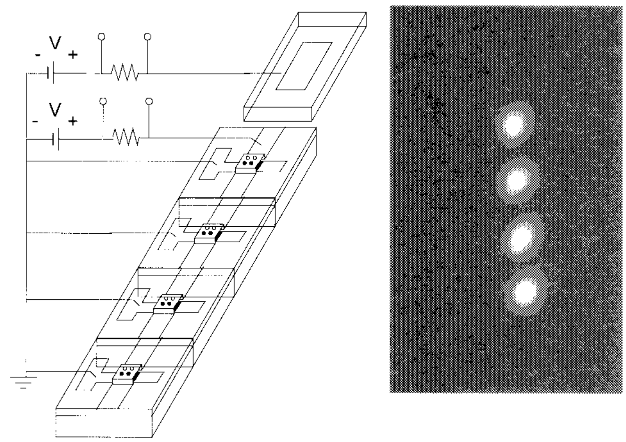
Fig. 6. (a) Experimental setup for $I-V$ measurement and (b) $I-V$ curve and F–N plot of a display cell when tested in a diode configuration.



(a) (b)

Fig. 7. (a) Setup for emission image from a triode display cell and (b) its corresponding image.

The structure shown in Fig. 5 and an anode, with an anode to grid separation of 50 μm, were used to measure the grid and anode currents at 10^{-6} torr. As obvious from Fig. 9, the grid current is an order of magnitude lower than the anode current. An anode to grid current ratio in the range of 0.1–10 has been recently reported [14]. Unfortunately, the yield could not be improved beyond 5% due the appearance of cracks in the SOG layer. Replacing the SOG by a film of low-temperature oxide is expected to improve the yield. The work currently in progress, which will use low-temperature oxide, involves the development of a new FED microchip containing prototype FED structures and will be the subject of a subsequent publication.



(a) (b)

Fig. 8. (a) Setup for measuring emission image from 1×4 pixel FED and (b) its corresponding image.

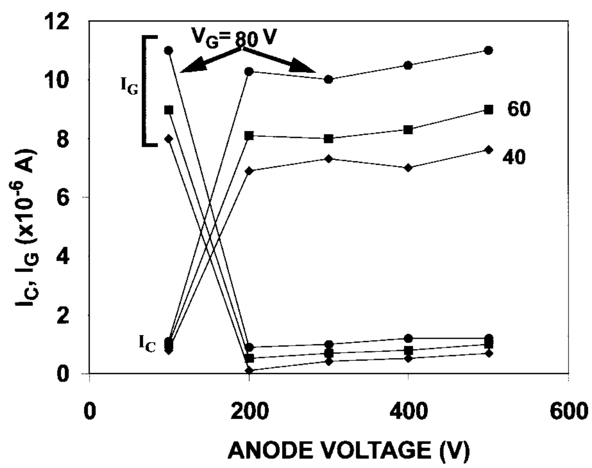


Fig. 9. Anode current I_a and gate current I_g as a function of anode voltage V_a for different gate voltages V_g.

IV. Conclusions

Diamond FED display cells are fabricated using an IC-compatible diamond film processing and are tested in diode and triode modes. The field emission current is initiated at 20 V at 10^{-6} torr resulting in a threshold of emission field in the range of 0.07–0.1 V cm^{-1}, and reaches a value of $\sim$20 μA at 80 V. The light emission pattern is recorded for a 1×4 pixel gated FED for the first time.

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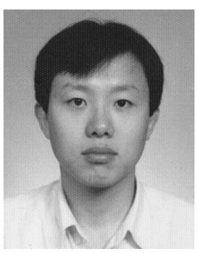

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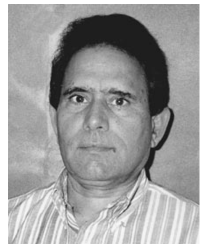

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