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Microfabricated Capacitive Electrodes for High Channel Count ECoG Recording

Heyu Yin, Ehsan Ashoori, *Student Member, IEEE*, Sina Parsnejad, Joseph W. Salatino, Erin K. Purcell, and Andrew J. Mason, *Senior Member, IEEE*

***Abstract*—Toward understanding brain functionality, high channel count ECoG arrays enable expanding the resolution and/or physical scope of neural recordings. For fully implanted ECoG arrays, one limiting factor to scaling channel count is the size of the front-end recording electronics, which is dominated by the coupling capacitor needed at every recording channel. This paper presents an ECoG array with coupling capacitors fabricated into the electrodes that significantly reduces the area required for recording electronics and thus enables scaling to higher channel counts. Two different fabrication procedures were explored to form 4x4 arrays of 8 pF capacitor-embedded electrodes utilizing a stack of Cu, Ta2O5, and Ti/Au on a flexible substrate. Several *in vivo* experiments were performed on an adult rat, and physiologically evoked activity was successfully observed for shoulder and hindlimb tapping as well as for whisker deflection.**

Keywords—ECoG, capacitive electrodes, high-channel-count neural recording, large scale brain activity monitoring

I. Introduction

Large scale brain monitoring with high resolution provides valuable insight into the brain functional structure and also could enable high performance BMIs to, for instance, restore natural limb movements [1]. Although noninvasive neural recording is the most preferable choice, noninvasive methods such as functional magnetic resonance imaging (fMRI) or electroencephalographic (EEG) do not provide high spatial or temporal resolution that enables advanced prosthetics or detailed studies of the brain. On the other hand, implantable neural recording microsystems have become a necessity in biological and clinical research with their potential to help understanding brain structure and function as well as enhancing the quality of life for people with certain neurological diseases [2]. Two main family of implantable neural recording families are penetrating probes which will be inserted into brain tissue and electrocorticography (ECoG) electrodes which only touch the brain surface. Although penetrating probes provide higher resolution, ECoG electrodes are far less invasive and more appropriate for large scale brain monitoring with high number of channels while provide higher resolution than noninvasive methods.

Size of the recording chip in implant applications is of high importance due to the limited space and discomfort of the patient. One limiting factor in implantable neural recording chip size is the coupling capacitor which is needed for every single recording site. This issue is more highlighted in high channel count recording systems. These capacitors are very important because electrodes that are in direct contact with living tissue generate a DC offset voltage as a result of electrochemical reaction at the interface [3]. The generated DC offset could potentially saturate the recording circuitry and stops the system to function properly. The most successful method to address this issue is the use of coupling capacitors to block the input DC offset [4, 5], as shown in Fig. 1. Noise and gain requirements dictate ~10 pF coupling capacitor value is needed for proper function which can occupy a large chip area especially when large number of channels are needed. For instance, implementing this big capacitor has occupied almost two third of the chip area in a 1.5 µm CMOS technology [4]. This proportional size issue gets more highlighted as in advanced CMOS technology capacitors do not shrink as much as active circuits.

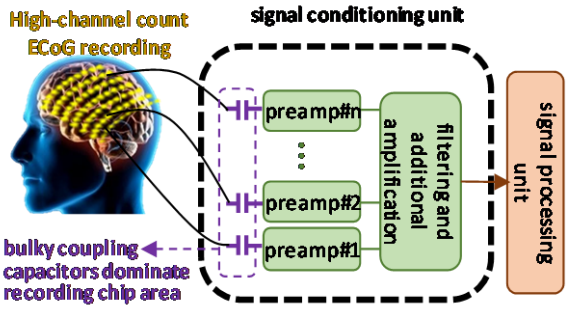

Fig. 1. Conventional ECoG recording system along with coupling capacitor design to block the input DC offset.

This paper presents a new capacitive ECoG array that significantly reduces the readout chip area to allow high channel count ECoG recording. The capacitive ECoG array utilizes the coupling capacitor structure for DC offset control but moves the coupling capacitors out of the CMOS recording circuitry and into the area occupied by ECoG electrodes. ECoG electrode, which typically has a diameter around 100 µm [6], provides the chance to embed coupling capacitors within the electrodes to relieve the size requirement of the recording chip for implementing on-chip coupling capacitors. Forming thin film of high dielectric materials on the same site of the electrodes enables implementing high enough capacitances without using silicon chip real estate while handling the input DC offset and hence decreasing the recording chip size significantly. ECoG electrode arrays were fabricated on polyimide substrate while each electrode was composed of a stack of copper (capacitor plate, CP), Ta_2O_5 (dielectric) and titanium-gold (electrode-capacitor plate, ECP). Fabrication methods with two different commercial available Kapton substrates were demonstrated, methods that help to solve the fabrication challenges were discussed. The new electrodes, integrated with the neural amplifier developed by our group [7], were used to perform

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Heyu Yin*, Ehsan Ashoori, Sina Parsnejad, Erin K. Purcell and Andrew J. Mason are with the Electrical and Computer Engineering Department, Michigan State University, East Lansing, MI 48823 USA (phone: 517-898-6253; fax: 517-353-1980; e-mail: yinheyu@msu.edu).

Joseph W. Salatino and Erin K. Purcell, are with the Biomedical Engineering Department and Institute for Quantitative health Science and Engineering, Michigan State University, East Lansing, MI, 48823.

in vivo experiments on an anesthetized adult rat to record stimulated neural activities.

II. METHOD

A. Capacitive DC Offset Rejection

For rejecting input DC offset voltage, capacitively coupled circuits show better performance than other approaches [7]. Utilizing the capacitively coupled structure, a schematic of the capacitive ECoG electrode coupled to neural amplifier is shown in Fig. 2. The coupling capacitor (C_1) along with a feedback capacitor (C_2) produce a gain factor which can be calculated as AV= C_1/C_2. A resistor (R_{bias}) parallel to the feedback capacitor not only biases the input of the OTA but also forms a high pass filter. As known, typical ECoG signal bandwidth is between 1-500 Hz. Therefore, the filter should be designed to have a very low 3-dB frequency at 1 Hz which requires that $C_2 \times R_{bias}$ has a large value. In addition, big coupling capacitor is needed so that the neural amplifier has sufficient voltage gain and good noise performance to handle weak neural signals [4]. Therefore, implementing a big coupling capacitor (C_1) is critical which in turn makes the size of C_1 an important factor for overall size of the amplifier. Furthermore, although further amplifying and processing blocks could be shared between different channels, a preamplifier is necessary for every single channel for signal conditioning. Consequently, the size of coupling capacitors is a crucial factor in the total area occupied by the ECoG recording circuit which limits the scalability toward high-channel-count large-scale brain activity monitoring.

To facilitate high channel count ECoG recording, as shown in Fig.2, we have introduced a new approach in which the large coupling capacitor (C_1) is transferred out of the silicon area and realized within the ECoG electrodes. Since ECoG electrode has large footprint, coupling capacitors could be realized in the same area by stacking the thin film dielectric material in conjunction with another layer of metal. This parallel plate capacitor is served as the coupling capacitor where the ECoG electrode works as one plate of the coupling capacitor. This approach will remain the electrode footprint as was before while significantly decreasing the amplifier silicon real estate by omitting the large coupling capacitor (C_1) for every ECoG channel. This approach allows the ECoG circuitry to be very compact and empowers expanding the recording system to higher channel-count and higher scale brain monitoring.

B. Fabrication of Capacitor-Embedded Electrodes

To implement the coupling capacitor embedded ECoG electrodes, two different fabrication methods were explored and discussed in this section. The microfabrication processes were performed on top of flexible polyimide film because the flexibility improves contact to brain tissue. In our design, a circular capacitor array structure with 200 µm diameter of each electrode and 575 µm pitch between electrodes was adopted. For the bottom metal layer named as capacitor plate (CP), copper was chosen for low cost consideration. For the dielectric layer, in order to form high capacitance devices, on the order of 10pF, within the 200 µm plates/electrodes, Ta_2O_5 was chosen as the dielectric material due to its outstanding dielectric constant [8]. Even the dielectric constant of Ta_2O_5

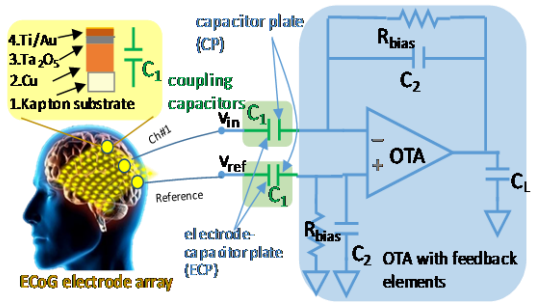

Fig. 2. Illustration of coupling capacitor embedded ECoG array with the schematic of the capacitively coupled neural amplifier.

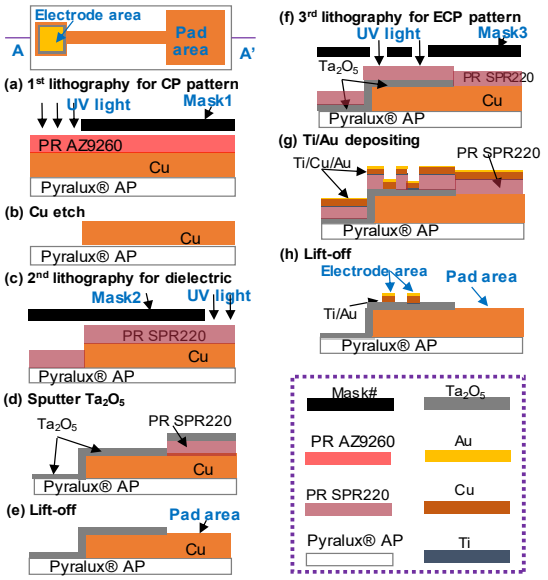

Fig. 3. Procedure I fabrication flow for the new ECoG array with capacitive electrodes.

may change according to fabrication method, we assume a minimum value of 15 to calculate the necessary Ta_2O_5 thickness. Considering possible misalignment and non-uniform layer deposition, the Ta_2O_5 thickness was calculated as ~100 nm for a 10 pF capacitance design. This breakdown voltage, which limits how thin the Ta_2O_5 can go, also depends on the thickness of the Ta_2O_5 as well as the fabrication method and conditions. According to literature, if the breakdown field for Ta_2O_5 is 100 mV/nm [8], the breakdown voltage for 100 nm Ta_2O_5 is about 10 V, which should be high enough in ECoG recording. For the second plate of the capacitor (ECP) which serve as the electrode to touch the surface of the brain, a 200 nm layer of gold was chosen for good conductivity, stability and biocompatibility. Two different fabrication procedures were developed for the capacitor-embedded electrode fabrication. One of them utilizes the etched commercially available thick copper layer as the CP layer, while other one utilizes the deposited thin film copper as the CP layer. Both fabrication methods have their own pros and cons, detailed fabrication steps together with the pros & cons analysis were discussed as follow.

1) Fabrication Procedure I

The detailed fabrication process flow for the new capacitor embedded ECoG array is shown in Fig. 3. A commercially available polyimide film (DuPontTM Pyralux® AP), which comes with a 9 µm thick bonded

copper foil, was chosen as a substrate. To easily handle the flexible substrate in lithography process, the Pyralux polyimide substrate was first affixed to a 3-inch quartz wafer using Crystal-bond (Crystal-bond 555HMP, 60 °C, SPI Supplies) as a temporary bonding material. The first step was to pattern the CP layer on top of the polyimide substrate. For better lithography performance, a stripping process was first performed to clean the substrate and then a thin layer of HMDS was deposited for better adhesion. Because the CP layer is 9um thick, AZ9260 photoresist was spin-coated with 8 µm thick receipt and patterned to expose everything except the electrode sites, interconnections and connecting pad sites. Since the crystal-bond is water soluble material, before copper etching, the polyimide substrate with pattern will be relived from the crystal wafer to expose the backside. Ferric chloride copper etchant (MG Chemicals, Ferric chloride copper etchant solution) was then used under 50 °C to etch away the unwanted copper and the copper on the backside.

After etching the copper, the polyimide sheet with copper pattern will be affixed with the crystal wafer again with Santovac (Santovac 5 Polyphenyl Ether Diffusion Pump Fluid) as a temporary bonding material. Compare to crystal-bond, Santovac have better performance regarding the degas issue, which is vital in the high vacuum environment of subsequent dielectric material and metal deposition steps. Then, a second lithography process was performed with SPR220 as photoresist to create the pattern for Ta_2O_5 dielectric material deposition. For better edge coverage, which is critical for capacitor fabrication, a sputtering process was chosen to achieve about 100 nm thick Ta_2O_5 layer. A lift-off process was then performed to expose the bottom copper layer in the pad area for connection to amplifiers. Then the third lithography, again with SPR220 as photoresist, was performed to pattern the top electrodes. Following the lithography, electron beam deposition was chosen for the top electrode layer (10nm Ti/ 200nm Au) deposition to simplify the lift-off process. 10nm thick titanium layer was good enough for better adhesion, and 200nm gold was chosen as the top layer for better conductivity and biocompatibility. Finishing the lift-off process, the capacitor embedded ECoG electrode arrays were formed on top of the flexible Pyralux substrate.

2) Fabrication Procedure II

In fabrication procedure I, although the thick CP layer will provide less resistivity, the 9um copper layer make the alignment and the device characterization difficult. For easier alignment and better device characterization purpose, the second fabrication procedure which utilizes a copper deposition process on top of bare polyimide film instead of copper etching was developed. This thin copper deposition process allows us to add interconnects for ECP layer which will make the device characterization more convenient. In fabrication procedure II, instead of choosing the Pyralux polyimide film, a bare Kapton film (DuPontTM Kapton® 300HPP-ST) was chosen as the substrate. As shown in Fig. 4, instead of copper etching, the first lithography with SPR 220 as photoresist is to create pattern for following copper deposition with electron beam evaporation. Because there is no need to release the backside during the fabrication process, we only need to use Crystal-bond to fix the Kapton substrate to the quartz wafer which also simplifies the fabrication process. Then, a lift-off process will be performed to create the CP layer. Then, steps (d-i) in Fig. 4 are almost the same as the steps (c-h) in Fig. 3 in fabrication procedure I. The only difference is that the mask used for the third lithography in fabrication procedure II has interconnections for the ECP layer also.

C. Comparative Analysis of Two Fabrication Procedures

Fabrication procedure I, with a thicker CP layer, will provide less resistivity resulting higher Q factor for the embedded capacitors. However, the 9um CP layer is not compatible with thin metal deposition methods which were chosen for the ECP layer deposition and will in turn make the alignment and the device characterization difficult. Compare to fabrication I, procedure II utilizing thin film deposition for the CP layer on top of bare polyimide substrate, not only simplifies the alignment to a great extent but also allows us to add interconnection for CPF layer for easier device characterization. On the other hand, because of the thinner CP layer which will increase the resistance of the interconnection, procedure II will sacrifice the capacitance performance of the ECoG electrode slightly due to the lower Q factor.

D. In Vivo Experiment Procedure

The ECoG array was tested via observation of sensory-evoked activity in the somatosensory cortex (S1) of an adult male Sprague-Dawley rat under isoflurane anesthesia

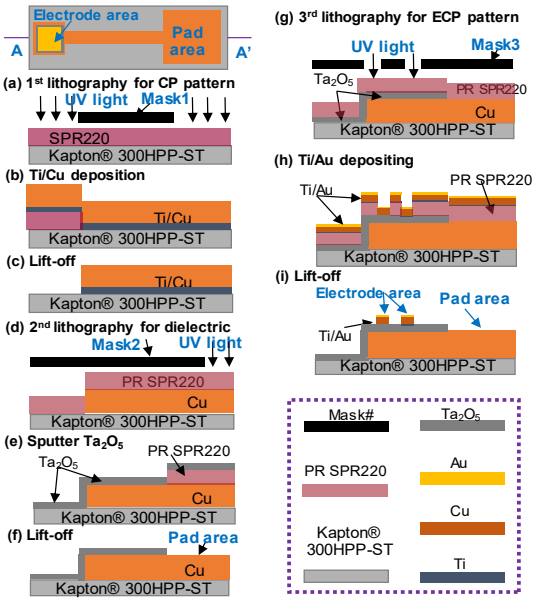

Fig. 4. Procedure II fabrication flow for coupling capacitor embedded ECoG electrodes.

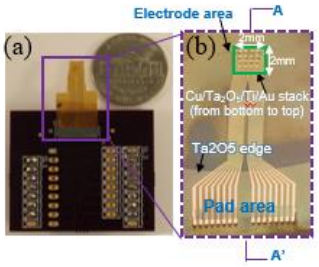

Fig. 5. (a) ECoG electrode in hands showing its flexibility; (b) Fabricated ECoG electrode.

(11wks, 300g, Charles River, Wilmington, MA). A hand drill and rongeurs were used to expose S1 (centered at 2.0mm posterior, 4.0 mm lateral from bregma) with a 4x4mm craniotomy in the left hemisphere. The ECoG array was positioned to span barrel field (S1BF) as well as hindlimb and shoulder representations [9]. Activity in S1BF was stimulated by manual deflection of the contralateral whisker set. Manual stimulation of the ipsilateral whisker set was performed to control for potential sources of noise associated with the experimental procedure. Replication of the entire procedure was used to confirm observations of stimulus-evoked activity. All surgical procedures were approved by the Michigan State University Animal Care and Use Committee.

III. Results

The microfabricated capacitive ECoG electrodes were first characterized with bench test, and then *in vivo* test were performed with an adult rat. For the readout in both on bench and *in vivo* tests, a recording circuit was designed and fabricated using off the shelf components to test the fabricated capacitive ECoG electrodes [7].

A. Bench Test Results

Multiple 4x4 ECoG electrode arrays with embedded capacitors, as shown in Fig. 5, were fabricated with both fabrication procedures. The ECoG electrode array was used in conjunction with the recording circuit in multiple frequency within the ECoG frequency band. The input AC signal was applied using a bath of 0.9% saline. The transfer function of the recording system was derived and based on the result, the fabricated coupling capacitors were characterized to approximately 8 pF of capacitance with breakdown voltage of more than 5 V.

B. In Vivo Experimental Results

The *in vivo* experimental test setup with the capacitor embedded ECoG electrode positioned on the cortical surface of an isoflurane-anesthetized adult rat is shown in Fig. 6. In contrast to the responses to ipsilateral stimulation, which are similar to the baseline (Fig. 7b), Fig. 7 reveals robust activity evoked from the contralateral hemisphere during whisker deflection (Fig. 7a). We validated the reproducibility of the results across multiple trials performed in the same subject. In addition, similar results were observed following manual tapping of the shoulder and hindlimb areas (data not shown). The *in vivo* test results validate that the novel ECoG arrays are able to collect physiologically-evoked activity, where signal modulation was detected exclusively from the side of the body responsible for delivering the appropriate input.

IV. Conclusion

To decrease the size of ECoG amplifiers for high channel count applications, this paper presented a new electrode array where the bulky coupling capacitors were moved from the silicon chip and embedded within the electrode array. Utilizing two fabrication procedures, 4x4 arrays of capacitor embedded electrodes were fabricated on flexible substrates. A custom PCB amplifier was designed as the recording circuit and both bench test and in vivo experiments of the capacitor-embedded ECoG electrode array were performed to verify the functionality. Results show that the new capacitor-embedded ECoG electrodes effectively detected physiologically-evoked activity.

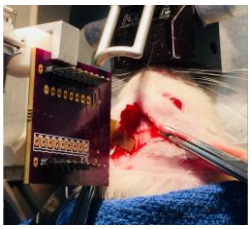

Fig. 6. *In vivo* experimental test setup with an adult male rat.

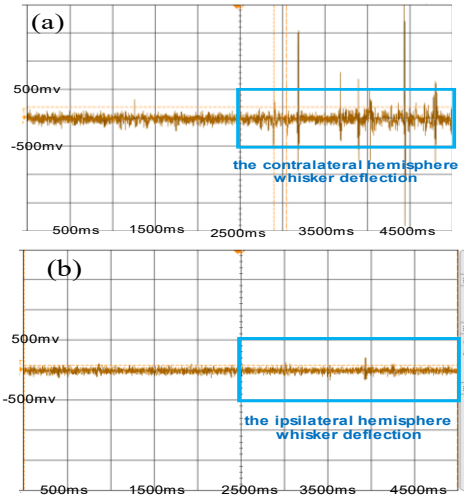

Fig. 7. *In vivo* experimental results for manual whisker deflection in (a) contralateral hemisphere and (b) ipsilateral hemisphere.

Acknowledgment

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References

[1] D. A. Schwarz *et al.*, "Chronic, Wireless Recordings of Large-Scale Brain Activity in Freely Moving Rhesus Monkeys," *Nat. Methods*, vol. 11, no. 6, pp. 670–6, 2014.

[2] B. Rubehn, C. Bosman, R. Oostenveld, P. Fries, and T. Stieglitz, "A MEMS-based flexible multichannel ECoG-electrode array," *J. Neural Eng.*, vol. 6, no. 3, 2009.

[3] C. D. Ferris, *Introduction to bioinstrumentation*. Humana Press, 1978.

[4] R. R. Harrison and C. Charles, "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, 2003.

[5] E. Ashoori, S. Dávila-montero, and A. J. Mason, "Compact and low power analog front end with in-situ data decimator for high-channel-count ECoG recording," in *Circuits and Systems (ISCAS), 2018 IEEE International Symposium on*, 2018, pp. 1–4.

[6] X. Wang *et al.*, "Mapping the fine structure of cortical activity with different micro-ECoG electrode array geometries," *J. Neural Eng.*, vol. 14, no. 5, 2017.

[7] E. Ashoori, H. Yin, S. Parsnejad, J. W. Salatino, E. K. Purcell, and A. J. Mason, "ECoG Electrode Array with Embedded Coupling Capacitors for Area Efficient Neural Recording," in *BioCAS*, 2018, pp. 419–422.

[8] S. Ezhilvalavan and T. Y. Tseng, "Preparation and properties of tantalum pentoxide (Ta2O5) thin films for ultra large scale integrated circuits (ULSIs) application - a review," *J. Mater. Sci. Mater. Electron.*, vol. 10, no. 1, pp. 9–31, 1999.

[9] G. Paxinos and C. Watson, "The rat atlas in stereotaxic coordinates". New York: Academic, 1998.