Screen-printed Planar Metallization for Lab-on-CMOS with Epoxy Carrier

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***Abstract*—The integration of biosensors, microfluidics and CMOS instrumentation provides a compact lab-on-CMOS microsystem well suited for high throughput measurement. This paper describes a screen-printed planar metallization technique for lab-on-CMOS that overcomes challenges associated with traditional thin film metallization. Utilizing a chip-in-carrier packaging approach with an epoxy carrier, screen-printed electrical interconnects are shown to reliably resolve up to 10µm step height differences between the CMOS chip and the surrounding carrier that supports microfluidics. The metallization process presented in this paper is also shown to be compatible with subsequent microfluidic integration to complete the lab-on-CMOS device platform.**

Keywords – lab-on-CMOS, chip-in-carrier, planar metallization, CMOS biosensor, screen-printing

I. Introduction

Identifying and quantitatively measuring analyte concentrations is one of the key objectives in chemical, biological and medical applications, such as bio-sensing, environmental monitoring, drug discovery and clinical diagnosis [1-3]. In particular, biosensors provide great diversity, sensitivity and specificity through hybridization, binding, transfer and other interactions with target analytes using antibody, antigen, peptide, DNA and other interfaces. To measure analyte concentration in solutions, many biosensors techniques have been developed, such as electrochemical methods, optical imaging, thermal detection, and spectrometry [4]. Electrochemical methods are very useful because they can readily be adapted to CMOS technology, and they offer label-free detection which eliminates external labels or indicators and greatly shortens assay time. CMOS instrumentation offers the opportunity to replace bulky lab bench top measurement equipment and permits further miniaturization and integration of a biosensor. Such miniaturization and integration enable portable and embeddable biosensors with performance benefits including array formation, better sensitivity, lower power consumption and lower cost. Further integration of on-CMOS biosensors with microfluidics allows controlled introduction of fluids and maintenance of a biocompatible environment. The resulting lab-on-CMOS platform is suitable for high throughput bio-analysis [5,6].

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While the integration of microfluidic-based biosensor interfaces and CMOS detection circuitry has many benefits, an obvious obstacle exists within the mismatch of device footprints [7]. Microfluidic devices usually have dimensions in centimeters while CMOS die have dimensions in millimeters. Furthermore, creating reliable electrical connections in the presence of fluids further constrains design efforts. A chip-in-carrier method has been developed to address these challenges [8]. Die-level photolithography process can fabricate stable electrodes on the surface of CMOS chips, and the carrier allows more area for microchannel fabrication without adding area and associated cost to CMOS fabrication. However, due to the inherent difference in the heights of the chip and the carrier, traditional PVD thin film metal deposition is not an effective solution for the planar metallization required in such lab-on-CMOS integration platforms.

This paper introduces a screen-printing metallization process to form planar electrical interconnects for lab-on-CMOS integrated devices. The metallization process provides robust electric interconnection using simple techniques that help to minimize fabrication costs. The screen printed interconnects are thick enough to overcome step heights across the device, yet the process still enables microfluidic devices to be integrated without any observed leakage between channels.

II. Lab-on-CMOS Metallization Challenges

To combine CMOS chips and microfluidics, several challenges must be addressed, including: 1) identifying reliable and simple methods to seal microfluidics on top of CMOS chip or carrier, because any leakage will ruin the whole system; 2) protecting the integrated circuits from the aqueous sample; 3) making electrical interconnection between the on-CMOS electrodes and readout circuit bond pads while also isolating the fluids from the metallization layer [7]. Furthermore, any packaging methods must be compatible with the integrated circuit process. This means no anodic bonding or high temperature process is allowed during the whole packaging process. Early packaging methods typically deposited layers of polymer directly on a

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chip or remove sacrificial layers using deep-RIE to create microchannels [9]. Such methods require extensive post-CMOS fabrication of chips or complicated machining of a package used to hold the CMOS chip. To form sensor electrodes on CMOS and support integration with microfluidics, our group has previously reported designs based on a chip-in-carrier approach [5,8]. This paper builds on these efforts with a focus on improving the planar metallization process.

The main techniques used to form interconnections with CMOS chips tape automated bonding (TAB), wire bonding, and flip chip. TAB is a high-density interconnection technology based on bonding bare die onto a polyimide film with copper leads through bumps using thermocompression bonding [10]. TAB can provide assembly package process, however, for lab-on-CMOS application, TAB is not ideal because of temperature restrictions and incompatibility with integration of microfluidic channels. Wire bonding is the most general way of forming interconnections because of its high yield and high interconnection density. Several groups have reported lab-on-CMOS work based on the wire bonding interconnection [11-12]. An integrated biological cell manipulation system has been reported in which CMOS and microfluidic devices were integrated in a hybrid fashion using conventional wire-bonding process for electrical interconnects [11]. However, one apparent shortcoming of the wire bonding method is that the metal bond wires eliminate many standard microfabrication operations which could be used to protect the bonding wires from the chemical corrosion and electrical failure. Moreover, lab-on-CMOS demands a large area for multi-channel microfluidic implementation, and bonding wires simply limit the available area for microfluidics. In the flip-chip method, a chip is placed on a substrate with its active surface facing the substrate, and interconnection between the I/O pad on CMOS chip and the pin on the package is created by solder bumps through thermal heating or thermosonic bindings. Hybrid integration of an active pixel sensor and microfluidics for cytometry on a chip has been reported [13]. A flip-chip bonded system for a broad range of electronic detection has been reported [14]. Seamless integration of CMOS and microfluidics using flip chip bonding and permanent bonding of PDMS to a flexible polyimide PCB has also been reported [15]. Using flip-chip methods, large surface area for multichannel design can be achieved. However, flip-chip methods require pre-determined design and various extra materials and processes including underfill epoxy, substrate metallization, substrate solder mask and chip passivation. Furthermore, on-CMOS sensor electrodes, which are critical to achieving a high measurement resolution, are inherently challenged by flip-chip methods that hide the surface of the CMOS chip against a packaging substrate.

III. Screen-Printing Method for Planar Metallization

In order to realize high throughput biosensor analysis in a lab-on-CMOS platform, a chip-in-carrier approach is well suited because of the extended surface area for microfluidics provided by the carrier [5]. Instead of using a traditional wire-bonding process, signals are routed off the CMOS chip and onto the carrier using planar metallization across the surface of the integrated platform. The planar metallization allows for subsequent formation of complex microfluidics directly on top of the CMOS chip and surrounding carrier without interference of bondwires, as illustrated in Fig. 1a. One method to produce the carrier is to form an epoxy layer surrounding the CMOS chip [16]. This method is simple and cost effective, but during the epoxy carrier formation process, a height difference of up to 10μm can be created between the carrier and the chip. The planar metallization must overcome this height difference. Because the thickness of PVD metal is limited to the order of 1μm, an alternative way to form interconnects that can improve yield while keeping cost and complexity low is highly desired.

The screen-printing method of metallization is a well-developed technology in which print ink or resin is deposited over a substrate through a predefined mask or screen. Screen-printed planar metallization can deposit layers thick enough to overcome uneven surface profile steps. Additionally, compared to PVD, screen-printing offers a wide material selection and low material cost.

The screen-printing metallization process described by Fig. 1b was developed for lab-on-CMOS applications using readily available materials and methods. Dielectric coated silicon die were cut to mimic CMOS chips and gold was deposited onto the chip surface using PVD to form sensor electrodes and chip bond pads. The chip was mounted on a glass holder and the epoxy carrier was formed around the chip using the process defined in [16]. A first parylene layer ($parylene_1$ in Fig. 1b.2) was then applied to the entire chip-in-epoxy-carrier assembly and patterned to cover the chip-carrier boundary and the carrier, leaving everything inside the chip bond pads exposed.

To start the metallization process, AZ4620 was spin-coated over the assembly and then it was exposed and developed to form a screen-printing mask for planar interconnects that route signals from the chip to the outer edge of the carrier. Silver (Ag) ink, PG-007 (Paru Co), was the screen printed through the AZ4620 mask following a standard process [17]. Afterward, a squeegee was used to flatten the film, and then the whole device was heated at 90ºC for 1 hour using a hotplate to cure the silver ink. This process provides an approximately 10μm planar

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metallization layer, which is thick enough to overcome the height difference between the CMOS die and the carrier. After curing, acetone was used to remove the AZ4620 screen mask and reveal the interconnect pattern. In order to insulate the interconnects from the aqueous environment, a second parylene layer (parylene$_2$ in Fig. 1b.3) was then deposited and patterned to form a protection and insulation layer, leaving only the on-chip biosensing electrodes exposed.

IV. Results

A. Resistance test

A 5mm×5mm silicon chip was used to demonstrate the chip-in-carrier packaging. A gold electrode array was fabricated on the silicon chip via deposition of 50Å/1000Å Ti/Au thin film metal, photolithography and patterning. Optical images of the fabricated device after screen-printed planar metallization are shown in Fig. 2. The silver interconnects run on top of the parylene$_1$ layer, from the carrier to the chip surface to make electrical contact. The silver interconnect is insulated by parylene$_2$ layer from contact with fluids. No distinguishable defects in the interconnects were observed from optical inspection and interconnects were found to be continuous when crossing the chip-carrier boundary.

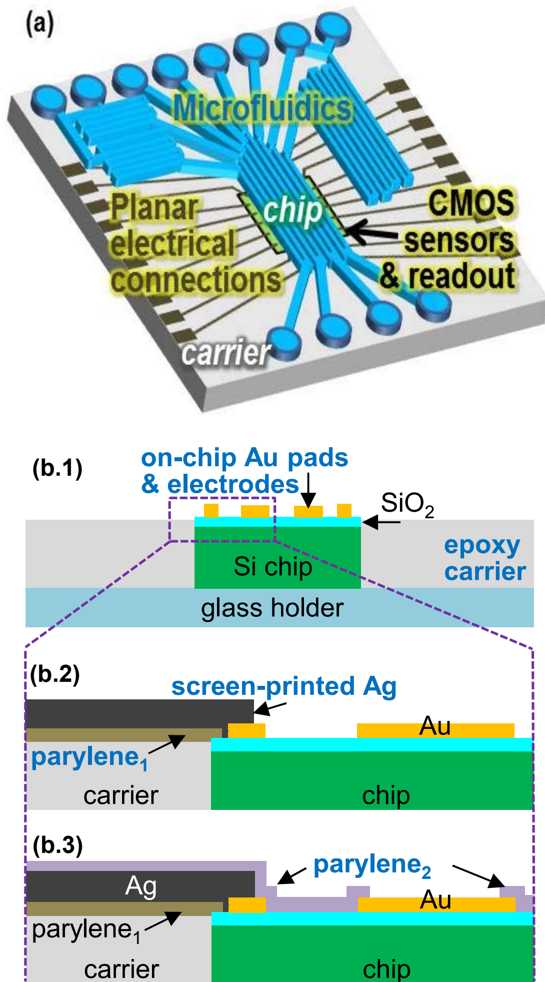

Fig. 1. a) Conceptual view of an integrated lab-on-CMOS sensor array; b) Post-CMOS process flow for chip-in-carrier approach with screen printed planar interconnects: b.1) device after epoxy chip-in-carrier process [16] using a dummy dielectric-coated Si die to mimic a CMOS chip; b.2) first parylene coating to cover die edge followed by Ag planar electrical interconnects screen-printed on surface of the chip-in-carrier assembly; b.3) second parylene layer to insulation all but sensor electrodes from the aqueous chemical environment. Following these steps, a microfluidics layer can be attached to the surface.

To verify functionality of the electrical interconnects between the on-chip Au electrodes and the connection pads on the carrier, resistance of all metal interconnects was tested using a probe station and a digital voltage meter. Most of the traces showed electric resistance around 10Ω, including the wire resistance, which demonstrates that the screen printing planar metallization process is a reliable method to form electrical interconnects for lab-on-CMOS platforms.

B. Microfluidic leakage test

Microfluidic experiments were carried out using a test device composed of the screen-printing metalized chip-in-carrier shown in Fig. 2, with an additional PDMS microfluidic device attached to the surface. As shown in Fig. 3, fluid with blue dye was flowed through the microchannel to test if the thick metallization layer created leakage in the fluidics. Fig. 3(a) shows that the device allows fluid to flow across a series of screen-printed metal traces on the carrier, and Fig. 4(b) shows that the device allows fluid to flow from carrier, onto chip, and back onto carrier. No leakage

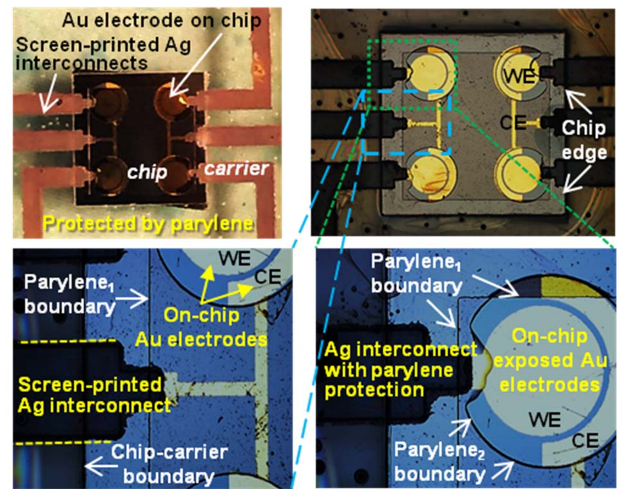

Fig. 2. Optical inspection of the screen-printed planar metallization layer. Screen-printed Ag interconnects were observed to be continuous even when crossing the chip-carrier boundary.

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was observed during any of these experiments, thus the microfluidic assembly is capable of low pressure microfluidic operation.

C. Electrochemical results

To verify the sensor functionality of the device, cyclic voltammetry (CV) was performed between 0 - 0.5V for Vwe with 100mV/s scan rate for $K_4[Fe(CN)_6]$ (potassium ferrocyanide) in KCl (potassium chloride) buffer using a commercial electrochemical instrument (CH instruments, Inc). An on-chip working electrode (WE) was used with off chip Ag/AgCl reference electrode (RE) and platinum wire counter electrode (CE). As the $K_4[Fe(CN)_6]$ concentration changes, different reduction and oxidation peak currents were collected as shown in Fig. 4. This experiment demonstrates the electrochemical functionality of the device and the cleanliness of the gold electrodes after going through several fabricatino steps. These results further validate the quality of the electrical interconnects and parylene insulation layer.

V. Conclusion

This paper introduced a screen-printing process to for planar metallization with a chip-in-carrier approach to lab-on-CMOS. A simple and low cost process flow was described. Test results confirmed that the screen printed interconnects are reliable and compatible with both integrated circuit chips, on-chip sensing electrodes and PDMS microfluidic channels.

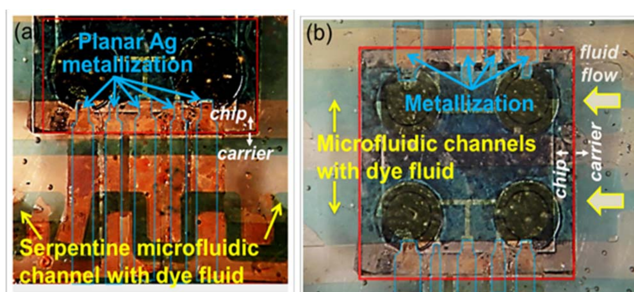

Fig. 3. No-leakage test: After the integration with PDMS microchannel, the system was tested with dyed DI water driven by syringe pump. (a) the fluid passes over multiple planar metallization traces; (b) the fluid flows across the chip-carrier boundary and over Au electrodes on the silicon chip.

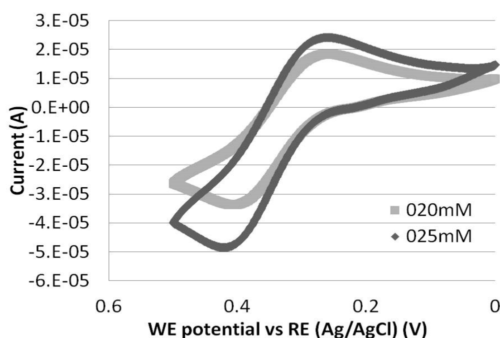

Fig. 4. Cyclic voltammetry test using the chip-in-carrier device. Fluid was pumped in through a PDMS channel, and on-chip WE and off chip RE and CE were used to test $K_4[Fe(CN)_6]$ concentration. Different redox peaks were collected for 20mM and 25 mM $K_4[Fe(CN)_6]$ solutions.

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