Module 16:
Printed Circuit Boards
16.0 Introduction

Electromagnetic compatibility has only recently become a concern for the designers of digital systems. Digital devices have become smaller and faster, and also are being used for a wider range of applications. As a result, the designers of digital circuits (who are typically not well versed in electromagnetic theory, or RF design) can no longer avoid electromagnetic compatibility issues. In this section basic PCB board design techniques used to avoid electromagnetic noise and interference will be examined.

16.1 Digital circuits

- Digital design is usually a purely mathematical process divorced from concerns about electromagnetic compatibility and noise effects.

- Even if the logic aspects of a digital circuit are correct, the circuit may fail to function properly in a particular environment, or may fail to meet legal emission limits.

- Many differences exist in design techniques for analog and digital circuits, such as methods of grounding, power distribution, and interconnection.
Although digital logic gates are typically small, and draw only a few milliamperes of current, the extremely fast switching speeds of these devices make them a major source of noise.

The voltage across an inductor is given by

\[ V = L \frac{di}{dt} \]

where \( L \) is inductance. Assume that a logic gate draws 5mA from a dc power supply in the “on” state and 1mA in the “off” state. Thus the total change in current is 4mA. If the change in current occurs in 2 nanoseconds and the power supply wiring has an inductance of 500 nH, then the noise voltage which is generated across the power supply wiring when the gate switches is

\[ V = 500 \times 10^{-9} \times \frac{4 \times 10^{-3} \text{A}}{2 \times 10^{-9} \text{s}} = 1 \text{V}. \]

If the power supply voltage is only 3.3 V, then the voltage calculated above may be a major source of noise which may make its way onto ground, power, or signal conductors associated with the digital circuitry.
As discussed in Chapter 3, a digital clock signal may be modeled as a trapezoidal waveform having a rise time $T_r$. It was seen in this chapter that the trapezoidal waveform with rise time $T_r$ has significant spectral content out to a frequency of about

$$f = \frac{1}{\pi T_r}.$$ 

It is at this breakpoint that the frequency envelope associated with the trapezoidal waveform begins to decrease at 40 dB/decade. This frequency is often referred to as the “bandwidth” of a digital logic circuit.

Digital circuits are inherently less susceptible to external noise sources than analog circuits.

16.2 Digital logic noise

Internally generated noise is a concern in the design and operation of digital circuits. This internal noise results from

- ground bus noise
- power bus noise
- transmission line reflections
Noise problems in digital circuits usually result in degraded performance.

Due to the incredible complexity of modern digital systems, such as computer processors, comprehensive laboratory testing of pre-production units is usually not possible. As a result proper design techniques applied at the earliest stages of development are critical to product success.

Although consumers are rather forgiving in regard to software shortcomings, hardware deficiencies are usually not tolerated.

* Internal noise sources

A simplified digital logic circuit is shown below.

Figure 1. Simplified digital logic circuit.
Assume that the output of gate 1 switches from high to low.

- Before gate 1 switches, the output is high and \text{C}_{\text{man}}\ is charged to the supply voltage.

- When the output of gate 1 switches to low, the \text{C}_{\text{man}}\ must discharge before the low signal is transmitted to gate 3.

- A large transient current flows through the ground system to discharge \text{C}_{\text{man}}\.

- Due to inductance associated with the ground connection, the discharge current produces a noise voltage pulse at the ground terminals of gates 1 and 2.

- If the output of gate 2 is low, the noise pulse will be interpreted by gate 4 as a switching signal from gate 2, which in turn may cause gate 4 to switch.

- The only practical way to reduce this noise voltage is to reduce the inductance associated with ground connections.
In addition to generating a noise voltage pulse, the discharge path through the ground connections forms a series resonant circuit that may oscillate.

![Diagram of a series resonant circuit](image)

**Figure 2. Digital logic gate output waveform.**

The $Q$ of a series resonant circuit is given by

$$Q = \frac{1}{12} \sqrt{\frac{1}{C}}.$$

The $Q$ associated with the discharge path can be decreased by placing a resistor at the output of the logical gate.

![Diagram of a digital logic gate with a damping resistor](image)

**Figure 3. Digital logic gate output with damping resistor.**

-DC-
- The damping resistor placed at the output of gate 1 will reduce the amount of ringing.

Another source of noise is illustrated in the figure below.

![Transistor-transistor logic schematic](image)

**Figure 1.** Transistor-transistor logic schematic.

- When the input is grounded, Q1 turns on, which turns on Q2 and turns off Q4. Transistor Q3 is then driven on by current flowing through R2. Q3 amplifies this current.

- When the output is high, Q3 is on, and Q4 is off. When the output is low Q3 is off and Q4 is on. In each case the impedance between the source and ground is high.
- While the gate is in the process of switching, for a brief time both Q3 and Q4 are on. This provides a low impedance path from the source to ground, causing a large current spike.

- The large current transient drawn from the source flows through the power and ground conductors, causing a large transient drop in the supply voltage.

- This effect can be minimized by placing a capacitor near each gate which supplies the transient current instead of drawing it through the power and ground connections. This will be discussed later in this chapter.

- **Digital circuit ground noise.**

  In digital circuit design, ground noise tends to be more of a problem than power supply noise.

- Power supply transients can be controlled with decoupling capacitors. Signal currents in the ground system cannot be bypassed or decoupled.

- Transient currents in the ground system are a major source of intrasystem noise as well as both conducted and radiated emissions.
Noise voltages arising from transient currents in the ground system can be controlled by minimizing the impedance of ground connections and current return paths.

At the frequencies at which digital circuits are commonly operated, the inductive component of the ground system impedance is dominant. Thus noise voltages are controlled by minimizing the inductance of ground connections and current return paths.

**minimizing inductance**

In previous chapters it was seen that several types of inductance exist:

1. Internal self-inductance is proportional to the length of a conductor, and also depends on cross-sectional geometry.

2. External self-inductance depends on circuit geometry.

3. Mutual inductance depends on circuit geometry, proximity to other circuits, and the geometry of those circuits.

Internal self-inductance is controlled primarily by minimizing the length of critical leads which carry large transient currents (clock leads, and line or bus drivers).
- Because high frequency currents flow very close to the surface of a conductor, a large change in conductor cross-sectional dimension may only lead to a small change in internal self inductance.

- At most frequencies of interest, mutual inductance and external self inductance are greater in magnitude than internal self inductance.

- Mutual inductance can be limited by increasing the spacing between conductors. Mutual inductance may also be reduced by changing the orientation of closed circuits, or current loops to one another.

- Inductance (both mutual inductance and external self inductance) can be reduced by minimizing the area of the loop enclosed by current flow. This is most easily accomplished by placing signal or clock current paths close to the corresponding current return paths.

- Digital circuit grounding

- A high-speed digital circuit ground system must provide a low inductance connection between various components that must communicate with each other.
This is best accomplished by providing many parallel current return paths.

i. One approach is to use a solid ground plane.

ii. An equally effective method is to use a gridded ground system.

Figure 5. Gridded ground system.

Typically vertical ground traces are printed on one side of the board, and horizontal ground traces are printed on the other (for a single layer board). The traces are then connected with plated through holes. This leaves room for signal connections.
- Usually the ground grid is arranged on the board before signal paths are laid out. Layout of the ground grid is more difficult if done after signal conductors are arranged.

- If the ground system is poorly little can be done to remedy the situation, short of starting over with a better ground layout.

- Power distribution on printed circuit boards

  Ideally, the power distribution layout should mirror the ground system layout. Power conductors should run parallel to current return paths, and the two should be spaced as closely as possible.

- Noise generated by the power supply can be controlled using decoupling capacitors, therefore the layout of the power distribution network is not as critical as a proper ground system. Ground system layout should take priority over the power distribution layout.

As mentioned previously, when a logic gate changes state, large transient currents may be drawn from the power supply, through the ground system.

- Even if the ground system inductance has been minimized,
A significant voltage drop may occur across the inductance associated with power supply leads.

Figure 6. Large transient current drawn when logic gate switches.

- The magnitude of the transient voltage on the power supply line can be reduced by decreasing the inductance associated with the power leads. A power plane or grid (similar to the ground plane/grid) may be used for this.

- The power supply voltage transient can be minimized by incorporating a source, other than the power supply, from which the transient switching current may be drawn.

Figure 7. Transient current drawn through decoupling capacitor.
- A decoupling capacitor may be placed across the logic gate. The noise voltage across the gate is then a function of the decoupling capacitor and the connection between it and the gate.

- Decoupling capacitors are also used to control radiated emissions. This will be discussed in a later section.

- The type, value, and placement of decoupling capacitors are all dependent on the type of IC's used.

- Individual decoupling capacitors are placed close to the IC's that they serve. These individual capacitors are recharged using a larger bulk decoupling capacitor, which is located near where power is supplied to the entire board.

- Capacitors used for decoupling must have low inductance, and must operate at high-frequency. The minimum value of capacitance required is determined from

\[ C = \frac{\Delta I \Delta t}{\Delta V} \]

\[ \Delta V = \text{transient voltage drop in supply voltage due to } \Delta I \]
\[ \Delta I = \text{current transient drawn when logic gate switches} \]
\[ \Delta t = \text{time interval over which transients occur} \]
Example: For an IC that draws a transient current of 50mA for 2ns, if the designer requires that the voltage transient be limited to 0.1V, a capacitor with

\[ C = \frac{50 \times 10^{-3} A \times (2 \times 10^{-9} s)}{0.1V} = 0.001 \mu F \]

is required.

- A decoupling capacitor which is too small will not store sufficient charge to supply the transient current needed by the IC. A decoupling capacitor which is too large will have a self-resonant frequency that is too low, and will not provide a low impedance bypass path for the transient current drawn when the IC switches. It is remembered that a capacitor has a self-resonant frequency, given by

\[ f = \frac{1}{2\pi \sqrt{LC}} \]

at which its impedance is a minimum. Thus the smallest capacitor which is sufficient to provide decoupling is the best choice.

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• Decoupling capacitor placement

Placement of decoupling capacitors is critical to their successful operation.

- Decoupling capacitors should be placed as close to the ICs they serve as possible so as to minimize inductance between the IC and the capacitor.

- Leads connecting the capacitor and the IC should be as short as possible and placed close together to minimize loop area. One capacitor may also supply more than one IC.

Figure 8. Placement of decoupling capacitors
- **Unused Inputs**

  - To prevent unwanted switching, all unused inputs must be connected somewhere. A noise signal may couple to a floating input, causing a gate to switch. Unused inputs are normally connected to the voltage supply through a series resistor, or to ground.

### 16.3 Digital Circuit Radiation

Two types of radiation can occur from digital circuits: common-mode radiation and differential-mode radiation.

- **Differential-mode radiation** is caused by current flowing around loops formed by conductors in the circuit. These loops act as antennas which produce magnetic fields.

- **Common-mode radiation results from undesired voltage drops in the circuit**, which cause some parts of the circuit to be at a common-mode potential above true ground. Often this is the result of voltage drops in the ground system. External cables connected to the PCB board which are driven at the common-mode potential may act as antennae.

- **Common-mode radiation is generally more difficult to**
Control than differential-mode radiation.

- **differential mode radiation**

  Differential-mode radiation is modeled as radiation from a small loop antenna. Radiation from a loop is controlled by reducing the magnitude of the current flowing through the loop, reducing the frequency of the current, or reducing the area enclosed by the loop.

  The control of differential-mode radiation should be addressed in the initial design of PC boards.

  - Loop areas formed by clock and signal currents should be minimized.

  - The most critical loops are those that carry clock signals. Emissions from clock signals usually exceed other types of emissions.

  - To minimize loop area, leads carrying clock signals should be routed near ground returns.

  - Clock leads should not run parallel to data bus or signal leads for long distances.

  - Address buses, data buses, and other signal conductors may carry high currents, however the random nature of
These signals usually result in less radiation. Loop areas associated with these conductors should also be minimized by providing a current return for groups of data or address leads.

- Transient power supply currents are also a source of radiated emissions. Loop areas associated with these transient currents can be reduced by using decoupling capacitors near ICs. Decoupling capacitors also keep power supply currents off of the board backplane and interconnecting cables.

- Interboard cabling can be a source of differential mode radiation. As discussed in previous chapters, to minimize the loop area on a cable, the current return should be routed near the signal conductor. Various types of cables were discussed in a previous chapter.

• Common-mode radiation

Common-mode radiation is usually more difficult to prevent than differential-mode radiation. Common-mode radiation is emitted by cables or long conductors in the digital system. Common-mode emissions are modeled as those from a short monopole (a cable or conductor) driven by a voltage source (the ground plane). Common-mode radiation is limited by limiting common-mode current.

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Common mode current can be limited by

1. Minimizing the source voltage (normally the ground potential)
2. Placing a large common-mode impedance (choke) in series with the emitting cable or conductor
3. Shunting the common mode current to ground
4. Shielding the emitting cable.

Common-mode radiation is controlled by limiting the common-mode voltage that drives the radiating system.

- Most methods of minimizing differential mode radiation also minimize common-mode voltage (use of a ground plane or grid reduces voltage drop in the ground system).

- External ground connections should be located near external interface cables. The farther the external ground is from interface cables, the more likely that a large noise voltage exists between these points.

- Cable decoupling (shunting currents to ground) and shielding require "clean" grounds (ground connections not contaminated by digital logic noise).

- All I/O leads should be connected to a separate low inductance I/O ground that connects to the digital logic ground at
only one point. This prevents noise from the digital logic gates from being coupled to external cables which may act as antennas.

Figure 9. "Clean" I/O ground for external cables.

Common-mode emissions from cables may be limited using common-mode chokes. A pair of wires are wound around a ferromagnetic core.

Figure 10. Common mode choke
- A common-mode choke has no effect on differential mode currents, but presents an inductance to common-mode currents.

- Wires are wound around the core in such a way that magnetic fluxes arising from differential mode currents subtract in the core, while fluxes arising from common-mode currents add in the core.

![Diagram](image)

**Figure 11. Effect of common-mode choke on differential- and common-mode currents.**

In this way common-mode currents are presented with a large mutual inductance in addition to the self inductance of the conductor windings.

16.4 More about component placement

This chapter concludes with a further discussion of component placement to reduce conducted and radiated emissions from PC boards.
Connections between oscillators and the ICs they serve should be made as short as possible. In order to minimize loop area, signal and return paths of the clock signal should be parallel and close together.

Address, data, and I/O connections should be made as short as possible, with signal and return paths as close together as possible to minimize loop area.

![Diagram showing component placement]

Poor component placement

![Diagram showing improved component placement]

Better component placement

Figure 12. PCB board component configurations.
- The fastest components should be placed on a section of the board which is furthest from external connectors. This takes advantage of natural loss on the board material, which attenuates noise signals.

![Diagram of component placement]

**Figure 13. Placement of various-speed components on PC board.**

References
