ANALOG DEVICES

Low Noise, Precision, High Speed Operational Amplifier ($A_{VCL} \geq 5$)

OP37

FEATURES

Low Noise, 80 nV p-p (0.1 Hz to 10 Hz)
3 nV/√Hz @ 1 kHz
Low Drift, 0.2 μV/°C
High Speed, 17 V/μs Slew Rate
63 MHz Gain Bandwidth
Low Input Offset Voltage, 10 μV
Excellent CMRR, 126 dB (Common-Voltage @ 11 V)
High Open-Loop Gain, 1.8 Million
Replaces 725, OP-07, SE5534 In Gains > 5
Available in Die Form

GENERAL DESCRIPTION

The OP37 provides the same high performance as the OP27, but the design is optimized for circuits with gains greater than five. This design change increases slew rate to 17 V/μs and gain-bandwidth product to 63 MHz.

The OP37 provides the low offset and drift of the OP07 plus higher speed and lower noise. Offsets down to 25 μV and a maximum drift of 0.6 μV/°C make the OP37 ideal for precision instrumentation applications. Exceptionally low noise (e_n= 3.5 nV/ @ 10 Hz), a low 1/f noise corner frequency of 2.7 Hz, and the high gain of 1.8 million, allow accurate high-gain amplification of low-level signals.

The low input bias current of 10 nA and offset current of 7 nA are achieved by using a bias-current cancellation circuit. Over the military temperature range this typically holds I_B and I_{OS} to 20 nA and 15 nA respectively.

The output stage has good load driving capability. A guaranteed swing of 10 V into 600 Ω and low output distortion make the OP37 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120 dB. These characteristics, coupled with long-term drift of 0.2 μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low-cost, high-volume production of the OP37 is achieved by using on-chip zener-zap trimming. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

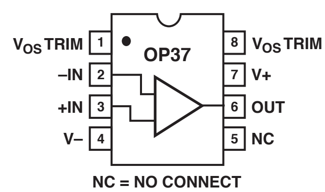
The OP37 brings low-noise instrumentation-type performance to such diverse applications as microphone, tapehead, and RIAA phono preamplifiers, high-speed signal conditioning for data acquisition systems, and wide-bandwidth instrumentation.

PIN CONNECTIONS

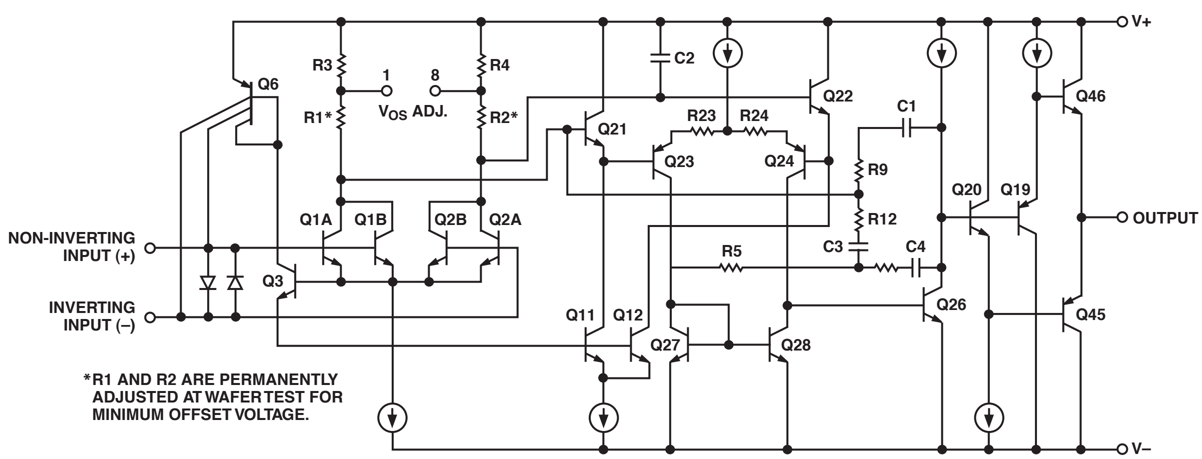
8-Lead Hermetic DIP (Z Suffix)

Epoxy Mini-DIP (P Suffix)

8-Lead SO (S Suffix)



SIMPLIFIED SCHEMATIC



REV. B

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ABSOLUTE MAXIMUM RATINGS[4]

Supply Voltage . . . . 22 V
Internal Voltage (Note 1) . . . . 22 V
Output Short-Circuit Duration . . . . Indefinite
Differential Input Voltage (Note2) . . . . 0.7 V
Differential Input Current (Note 2) . . . . 25 mA
Storage Temperature Range . . . . –65°C to +150°C
Operating Temperature Range
  OP37A . . . . –55°C to +125°C
  OP37E (Z) . . . . –25°C to +85°C
  OP37E, OP-37F (P) . . . . 0°C to 70°C
  OP37G (P, S, Z) . . . . –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) . . . . 300°C
Junction Temperature . . . . –45°C to +150°C

Package Type	θ_{JA}[3]	θ_{JC}	Unit
8-Lead Hermetic DIP (Z)	148	16	°C/W
8-Lead Plastic DIP (P)	103	43	°C/W
8-Lead SO (S)	158	43	°C/W

NOTES
[1]For supply voltages less than 22 V, the absolute maximum input voltage is equal to the supply voltage.
[2]The OP37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds 0.7 V, the input Current should be limited to 25 mA.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.
[4]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ORDERING GUIDE

T_A = 25°C V_{OS} MAX (μV)	CerDIP 8-Lead	Plastic 8-Lead	Operating Temperature Range
25	OP37AZ*		MIL
25	OP37EZ	OP37EP	IND/COM
60		OP37FP*	IND/COM
100		OP37GP	XIND
100	OP37GZ	OP37GS	XIND

*Not for new design, obsolete, April 2002.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP37 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

SPECIFICATIONS (V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP37A/E			OP37F			OP37G			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{OS}	Note 1		10	25		20	60		30	100	µV
Long-Term Stability	V_{OS}/Time	Notes 2, 3		0.2	1.0		0.3	1.5		0.4	2.0	µV/Mo
Input Offset Current	I_{OS}			7	35		9	50		12	75	nA
Input Bias Current	I_B			±10	±40		±12	±55		±15	±80	nA
Input Noise Voltage	e_{np-p}	1 Hz to 10 Hz[3, 5]		0.08	0.18		0.08	0.18		0.09	0.25	µV p-p
Input Noise Voltage Density	e_n	f_O = 10 Hz[3]		3.5	5.5		3.5	5.5		3.8	8.0	
		f_O = 30 Hz[3]		3.1	4.5		3.1	4.5		3.3	5.6	nV/√Hz
		f_O = 1000 Hz[3]		3.0	3.8		3.0	3.8		3.2	4.5	
Input Noise Current Density	i_N	f_O = 10 Hz[3, 6]		1.7	4.0		1.7	4.0		1.7		
		f_O = 30 Hz[3, 6]		1.0	2.3		1.0	2.3		1.0		pA/√Hz
		f_O = 1000 Hz[3, 6]		0.4	0.6		0.4	0.6		0.4	0.6	
Input Resistance Differential Mode	R_{IN}	Note 7	1.3	6		0.9	4 5		0.7	4		MΩ
Input Resistance Common Mode	R_{INCM}			3			2.5			2		GΩ
Input Voltage Range	IVR		±11	±12.3		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±11 V	114	126		106	123		100	120		dB
Power Supply Rejection Ratio	PSSR	V_S = ±4 V to ±18 V		1	10		1	10		2	20	µV/ V
Large Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	1000	1800		1000	1800		700	1500		V/mV
		R_L ≥ 1 kΩ, Vo = ±10 V	800	1500		800	1500		400	1500		V/mV
		R_L ≥ 600 Ω, V_O = ±1 V, V_S ±4[4]	250	700		250	700		200	500		V/mV
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12.0	±13.8		±12.0	±13.8		±11.5	±13.5		V
		R_L ≥ 600 Ω	±10	±11.5		±10	±11.5		±10	±11.5		V
Slew Rate	SR	R_L ≥ 2k Ω[4]	11	17		11	17		11	17		V/µs
Gain Bandwidth Product	GBW	f_O = 10 kHz[4]	45	63		45	63		45	63		MHz
		f_O = 1 MHz		40			40			40		MHz
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0		70			70			70		Ω
Power Consumption	P_d	V_O = 0		90	140		90	140		100	170	mW
Offset Adjustment Range		R_P = 10 kΩ		±4			±4			±4		mV

NOTES

[1]Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.

[2]Long term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5 µV—refer to typical performance curve.

[3]Sample tested.

[4]Guaranteed by design.

[5]See test circuit and frequency response curve for 0.1 Hz to 10 Hz tester.

[6]See test circuit for current noise measurement.

[7]Guaranteed by input bias current.

OP37–SPECIFICATIONS

Electrical Characteristics (V_S = ±15 V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.)

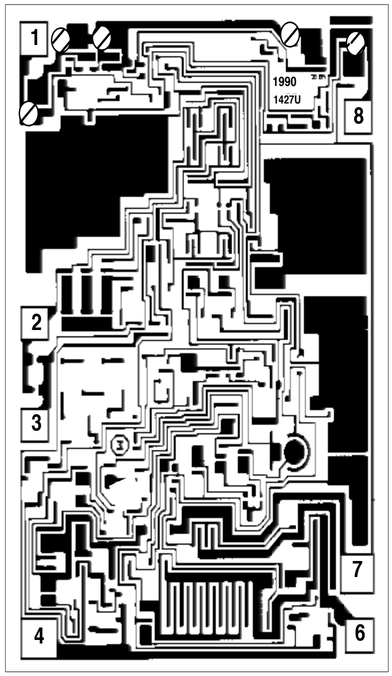
Parameter	Symbol	Conditions	OP37A Min	OP37A Typ	OP37A Max	OP37C Min	OP37C Typ	OP37C Max	Unit
Input Offset Voltage	V_{OS}	Note 1		10	25		30	100	µV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	Note 2 Note 3		0.2	0.6		0.4	1.8	µV/°C
Input Offset Current	I_{OS}			15	50		30	135	nA
Input Bias Current	I_B			±20	±60		±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5		±10.2	±11.5		V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±10 V	108	122		94	116		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		2	16		4	51	µV/ V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	600	1200		300	800		V/mV
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±11.5	±13.5		±10.5	±13.0		V

Electrical Characteristics (V_S = ±15 V, –25°C ≤ T_A ≤ +85°C for OP37EZ/FZ, 0°C ≤ T_A ≤ 70°C for OP37EP/FP, and –40°C ≤ T_A ≤ +85°C for OP37GP/GS/GZ, unless otherwise noted.)

Parameter	Symbol	Conditions	OP37E Min	OP37E Typ	OP37E Max	OP37F Min	OP37F Typ	OP37F Max	OP37C Min	OP37C Typ	OP37C Max	Unit
Input Offset Voltage	V_{OS}			20	50		40	140		55	220	µV
Average Input Offset Drift	TCV_{OS} TCV_{OSN}	Note 2 Note 3		0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Input Offset Current	I_{OS}			10	50		14	85		20	135	nA
Input Bias Current	I_B			±14	±60		±18	±95		±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8		V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±10 V	108	122		100	119		94	116		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		2	15		2	16		4	32	µV/ V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, $_{VO}$ = ±10 V	750	1500		700	1300		450	1000		V/mV
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±11.7	±13.6		±11.4	±13.5		±11	±13.3		V

NOTES
[1]Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
[2]The TC $_{VOS}$ performance is within the specifications unnulled or when nulled withR_P = 8 kΩ to 20 kΩ. TC $_{VOS}$ is 100% tested for A/E grades, sample tested for F/G grades.
[3]Guaranteed by design.

BINDING DIAGRAM



Wafer Test Limits

(V_S = ±15 V, T_A = 25°C for OP37N, OP37G, and OP37GR devices; T_A = 125°C for OP37NT and OP37GT devices, unless otherwise noted.)

Parameter	Symbol	Conditions	OP37NT Limit	OP37N Limit	OP37GT Limit	OP37G Limit	OP37GR Limit	Unit
Input Offset Voltage	V_{OS}	Note 1	60	35	200	60	100	μV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		±60	±40	±95	±55	±80	nA MAX
Input Voltage Range	IVR		±10.3	±11	±10.3	±11	±11	V MIN
Common Mode Rejection Ratio	CMRR	V_{CM} = ±11 V	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	T_A = 25°C, V_S = ±4 V to ±18 V	10	10	10	10	20	μV/V MAX
		T_A = 125°C, V_S = ±4.5 V to ±18 V	16		20			μV/V MAX
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	600	1000	500	1000	700	V/mV MIN
		R_L ≥ 1 kΩ, V_O = ±10 V		800		800		V/mV MIN
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±11.5	±12	±11	±12	±11.5	V MIN
		R_L ≥ 600 kΩ		±10		±10	±10	V MIN
Power Consumption	P_d	V_O = 0		140		140	170	mW MAX

NOTES
For 25°C characterlstics of OP37NT and OP37GT devices, see OP37N and OP37G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.