**General Description**

The LF198/LF298/LF398 are monolithic sample-and-hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having instability problems. Input impedance of $10^{10} \Omega$ allows high source impedances to be used without degrading accuracy. P-channel junction FET’s are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 µF hold capacitor. The JFET’s have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

**Features**

- Operates from ±5V to ±18V supplies
- Less than 10 µs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at $C_h = 0.01 \, \mu F$
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth
- Space qualified, JM38510

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies.

An “A” version is available with tightened electrical specifications.

**Typical Connection and Performance Curve**

![Typical Connection and Performance Curve](attachment:image.png)

**Functional Diagram**

![Functional Diagram](attachment:image.png)
Absolute Maximum Ratings (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ±18V
Power Dissipation (Package Limitation) (Note 2) 500 mW
Operating Ambient Temperature Range
LF198/LF198A −55˚C to +125˚C
LF298 −25˚C to +85˚C
LF398/LF398A 0˚C to +70˚C
Storage Temperature Range −65˚C to +150˚C
Input Voltage Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (Note 3) +7V, −30V
Output Short Circuit Duration Indefinite
Hold Capacitor Short Circuit Duration 10 sec
Lead Temperature (Note 4)
H package (Soldering, 10 sec.) 260˚C
N package (Soldering, 10 sec.) 260˚C
M package:
Vapor Phase (60 sec.) 215˚C
Infrared (15 sec.) 220˚C
Thermal Resistance (θJA) (typicals)
H package 215˚C/W (Board mount in still air)
85˚C/W (Board mount in 400LF/min air flow)
N package 115˚C/W
M package 106˚C/W
θJC (H package, typical) 20˚C/W

Electrical Characteristics
The following specifications apply for −V S + 3.5V ≤ V IN ≤ +V S − 3.5V, +V S = +15V, −V S = −15V, T A = T j = 25˚C, C h = 0.01 µF, R L = 10kΩ, LOGIC REFERENCE = 0V, LOGIC HIGH = 2.5V, LOGIC LOW = 0V unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LF198/LF298</th>
<th>LF398</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Offset Voltage, (Note 5)</td>
<td>T j = 25˚C, Full Temperature Range</td>
<td>1</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Input Bias Current, (Note 5)</td>
<td>T j = 25˚C, Full Temperature Range</td>
<td>5</td>
<td>25</td>
<td>10</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>T j = 25˚C</td>
<td>10</td>
<td>10</td>
<td>0.002</td>
</tr>
<tr>
<td>Gain Error</td>
<td>T j = 25˚C, R L = 10kΩ</td>
<td>0.002</td>
<td>0.005</td>
<td>0.004</td>
</tr>
<tr>
<td>Feedthrough Attenuation Ratio at 1 kHz</td>
<td>T j = 25˚C, C h = 0.01 µF</td>
<td>86</td>
<td>96</td>
<td>80</td>
</tr>
<tr>
<td>Output Impedance</td>
<td>T j = 25˚C, “HOLD” mode, Full Temperature Range</td>
<td>0.5</td>
<td>2</td>
<td>0.5</td>
</tr>
<tr>
<td>“HOLD” Step, (Note 6)</td>
<td>T j = 25˚C, C h = 0.01 µF, V OUT = 0</td>
<td>0.5</td>
<td>2</td>
<td>1.0</td>
</tr>
<tr>
<td>Supply Current, (Note 5)</td>
<td>T j ≥ 25˚C</td>
<td>4.5</td>
<td>5.5</td>
<td>4.5</td>
</tr>
<tr>
<td>Logic and Logic Reference Input Current</td>
<td>T j = 25˚C</td>
<td>2</td>
<td>10</td>
<td>2</td>
</tr>
<tr>
<td>Leakage Current into Hold Capacitor (Note 5)</td>
<td>T j = 25˚C, Hold Mode</td>
<td>30</td>
<td>100</td>
<td>30</td>
</tr>
<tr>
<td>Acquisition Time to 0.1%</td>
<td>ΔV OUT = 10V, C h = 1000 pF</td>
<td>4</td>
<td>20</td>
<td>4</td>
</tr>
<tr>
<td>Hold Capacitor Charging Current</td>
<td>V IN − V OUT = 2V</td>
<td>5</td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>Supply Voltage Rejection Ratio</td>
<td>V OUT = 0</td>
<td>80</td>
<td>110</td>
<td>80</td>
</tr>
<tr>
<td>Differential Logic Threshold</td>
<td>T j = 25˚C</td>
<td>0.8</td>
<td>1.4</td>
<td>2.4</td>
</tr>
<tr>
<td>Input Offset Voltage, (Note 5)</td>
<td>T j = 25˚C, Full Temperature Range</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Input Bias Current, (Note 5)</td>
<td>T j = 25˚C, Full Temperature Range</td>
<td>5</td>
<td>25</td>
<td>10</td>
</tr>
</tbody>
</table>
Electrical Characteristics

The following specifications apply for \(-V_S + 3.5V \leq V_{IN} \leq +V_S - 3.5V, +V_S = +15V, -V_S = -15V, T_A = T_J = 25^\circ C, C_h = 0.01 \mu F, R_L = 10 \, k\Omega, LOGIC\, REFERENCE = 0V, LOGIC\, HIGH = 2.5V, LOGIC\, LOW = 0V\) unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LF198A</th>
<th>LF398A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Impedance</td>
<td>(T_J = 25^\circ C)</td>
<td>10 (^{10})</td>
<td>10 (^{10})</td>
</tr>
<tr>
<td>Gain Error</td>
<td>(T_J = 25^\circ C, R_L = 10k)</td>
<td>0.002</td>
<td>0.005</td>
</tr>
<tr>
<td>Feedthrough Attenuation Ratio at 1 kHz</td>
<td>(T_J = 25^\circ C, C_h = 0.01 \mu F)</td>
<td>86</td>
<td>96</td>
</tr>
<tr>
<td>Output Impedance</td>
<td>(T_J = 25^\circ C, &quot;HOLD&quot;) mode</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>&quot;HOLD&quot; Step, (Note 6)</td>
<td>(T_J = 25^\circ C, C_h = 0.01 \mu F, V_{OUT} = 0)</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>Supply Current, (Note 5)</td>
<td>(T_J \geq 25^\circ C)</td>
<td>4.5</td>
<td>5.5</td>
</tr>
<tr>
<td>Logic and Logic Reference Input Current</td>
<td>(T_J = 25^\circ C)</td>
<td>2</td>
<td>10</td>
</tr>
<tr>
<td>Leakage Current into Hold Capacitor (Note 5)</td>
<td>(T_J = 25^\circ C)</td>
<td>30</td>
<td>100</td>
</tr>
<tr>
<td>Acquisition Time to 0.1%</td>
<td>(\Delta V_{OUT} = 10V, C_h = 1000 , \mu F)</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>Hold Capacitor Charging Current</td>
<td>(V_{IN} - V_{OUT} = 2V)</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>Supply Voltage Rejection Ratio</td>
<td>(V_{OUT} = 0)</td>
<td>90</td>
<td>110</td>
</tr>
<tr>
<td>Differential Logic Threshold</td>
<td>(T_J = 25^\circ C)</td>
<td>0.8</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by \(T_{JMAX} = \frac{P_D}{R_{JA}}\), and the ambient temperature, \(T_A\). The maximum allowable power dissipation at any temperature is \(P_D = \frac{T_{JMAX} - T_A}{R_{JA}}\) or the number given in the Absolute Maximum Ratings, whichever is lower. The maximum junction temperature, \(T_{JMAX}\), for the LF198/LF198A is 150\(^\circ\)C; for the LF298, 115\(^\circ\)C; and for the LF398/LF398A, 100\(^\circ\)C.

Note 3: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 4: See AN-450 “Surface Mounting Methods and their effects on Product Reliability” for other methods of soldering surface mount devices.

Note 5: These parameters guaranteed over a supply voltage range of \(\pm 5\) to \(\pm 18V\), and an input range of \(-V_S + 3.5V \leq V_{IN} \leq +V_S - 3.5V\).

Note 6: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01\(\mu F\) hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 7: Leakage current is measured at a junction temperature of 25\(^\circ\)C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25\(^\circ\)C value for each 11\(^\circ\)C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 8: A military RETS electrical test specification is available on request. The LF198 may also be procured to Standard Military Drawing #5962-8760801GA or to MIL-STD-38510 part ID JM38510/12501SGA.

Typical Performance Characteristics

<table>
<thead>
<tr>
<th>Aperture Time (Note 9)</th>
<th>Dielectric Absorption Error in Hold Capacitor</th>
<th>Dynamic Sampling Error</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="DS005692-17" alt="Aperture Time Graph" /></td>
<td><img src="DS005692-18" alt="Dielectric Absorption Error in Hold Capacitor Graph" /></td>
<td><img src="DS005692-19" alt="Dynamic Sampling Error Graph" /></td>
</tr>
</tbody>
</table>

Note 9: See Definition of Terms
Typical Performance Characteristics (Continued)

Output Droop Rate

Hold Step

“Hold” Settling Time
(Note 10)

Leakage Current into Hold Capacitor

Phase and Gain (Input to Output, Small Signal)

Gain Error

Power Supply Rejection

Output Short Circuit Current

Output Noise

Note 10: See Definition
Typical Performance Characteristics (Continued)

Input Bias Current

Feedthrough Rejection Ratio (Hold Mode)

Hold Step vs Input Voltage

Output Transient at Start of Sample Mode

Output Transient at Start of Hold Mode

Logic Input Configurations

TTL & CMOS

3V ≤ V_{LOGIC} (Hi State) ≤ 7V

Threshold = 1.4V

*Select for 2.8V at pin 8
Application Hints

Hold Capacitor

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may “sag back” up to 0.2% after a quick change in voltage. A long sample time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85˚C to 100˚C. Most ceramic capacitors are unusable with > 1% hysteresis. Ceramic “NPO” or “COG” capacitors are now available for 125˚C operation and also have low dielectric absorption. For more exact data, see the curve Dielectric Absorption Error.

The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10—50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

DC and AC Zeroing

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V+ and the other end tied through a resistor to ground. The resistor should be selected to give ≈0.6 mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01 µF hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

Logic Rise Time

For proper operation, logic signals into the LF198 must have a minimum dV/dt of 1.0 V/µs. Slower signals will cause excessive hold step. If a R/C network is used in front of the
Application Hints (Continued)

logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 1.0 V/µs.

Sampling Dynamic Signals

Sample error to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the “hold” command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/µs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1 µs) (0.6V/µs) = 60 mV error if the “hold” signal arrived near maximum dV/dt of the input. A positive-going input would give a +60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16 µs) (0.6 V/µs) = −96 mV. Total output error is +60 mV (digital) −96 mV (analog) for a total of −36 mV. To add to the confusion, analog delay is proportioned to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

A curve labeled Aperture Time has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the “hold” command. This curve is based on a 1 mV error fed into the output.

A second curve, Hold Settling Time indicates the time required for the output to settle to 1 mV after the “hold” command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input and the Cn pin. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.
Typical Applications

**X1000 Sample & Hold**

*For lower gains, the LM108 must be frequency compensated*

\[
\text{Use } C = \frac{100}{A_V} \text{ pF from comp 2 to ground}
\]

**Sample and Difference Circuit**

(Output Follows Input in *Hold Mode*)

\[
V_{OUT} = V_B + V_{IN}(\text{HOLD MODE})
\]

**Ramp Generator with Variable Reset Level**

\[
\Delta V = \frac{1.2V}{R_2} \cdot \frac{1}{C_m}
\]

*Select for ramp rate

\[
R_2 \geq 10k
\]

**Integrator with Programmable Reset Level**

\[
V_{OUT} (\text{Hold Mode}) = \frac{1}{(R_1)(C_m)} \int_{0}^{t} V_{IN} \, dt + V_R
\]
Typical Applications (Continued)

Output Holds at Average of Sampled Input

\[ \text{Select } (R_h) (C_n) \geq \frac{1}{2\pi f_h (\text{Min})} \]

Reset Stabilized Amplifier (Gain of 1000)

\[ V_{OS} \leq 20 \mu V \text{ (No trim)} \]
\[ Z_{IN} \approx 1 \text{ M}\Omega \]
\[ \frac{\Delta V_{OS}}{\Delta t} = 30 \mu V/\text{sec} \]
\[ \frac{\Delta V_{OS}}{\Delta T} = 0.1 \mu V/\text{C} \]
**Synchronous Correlator for Recovering Signals Below Noise Level**

*Select C1 to filter lowest frequency component of input noise

**Select C2 \( \approx 5 \times 10^{-6} / f_N \)**

**2-Channel Switch**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>1 ± 0.02%</td>
</tr>
<tr>
<td>( Z_{IN} )</td>
<td>( 10^{10} \Omega )</td>
</tr>
<tr>
<td>BW</td>
<td>1 MHz</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>−90 dB</td>
</tr>
<tr>
<td>@ 1 kHz</td>
<td></td>
</tr>
<tr>
<td>Offset</td>
<td>( \leq 6 \text{ mV} )</td>
</tr>
</tbody>
</table>

**DC & AC Zeroing**

*Select for step height

50k \( \rightarrow \) 1V Step

**Staircase Generator**

www.national.com 10
**Typical Applications** (Continued)

### Definition of Terms

**Hold Step:** The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

**Acquisition Time:** The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

**Gain Error:** The ratio of output voltage swing to input voltage swing in the sample mode expressed as a per cent difference.

**Hold Settling Time:** The time required for the output to settle within 1 mV of final value after the “hold” logic command.

**Dynamic Sampling Error:** The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

**Aperture Time:** The delay required between “Hold” command and an input analog transition, so that the transition does not affect the held output.

### Connection Diagrams

#### Dual-In-Line Package

Order Number LF398N or LF398AN
See NS Package Number N08E

#### Small-Outline Package

Order Number LF298M or LF398M
See NS Package Number M14A

#### Metal Can Package

Order Number LF198H, LF198H/883, LF298H, LF398H, LF198AH or LF398AH
See NS Package Number H08C
(Note 8)
Physical Dimensions inches (millimeters) unless otherwise noted

Metal Can Package (H)
Order Number LF198H, LF298H, LF398H, LF198AH or LF398AH
NS Package Number H08C

Molded Small-Outline Package (M)
Order Number LF298M or LF398M
NS Package Number M14A
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