DS75451/2/3
Series Dual Peripheral Drivers

General Description
The DS7545X series of dual peripheral drivers is a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.
The DS75451, DS75452 and DS75453 are dual peripheral AND, NAND and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

Features
- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI “A” and “B” series

Connection Diagrams (Dual-In-Line and Metal Can Packages)

*See (Note 5) and Appendix E regarding S.O. package power dissipation constraints.
### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

- Supply Voltage, \( (V_{CC}) \) (Note 2): 7.0V
- Input Voltage: 5.5V
- Inter-Emitter Voltage (Note 3): 5.5V
- Output Voltage (Note 4): 30V
- Output Current (Note 5): 300 mA
- Maximum Power (Note 5) Dissipation at 25˚C
  - Molded DIP Package: 957 mW
  - SO Package: 632 mW
- Storage Temperature Range: −65˚C to +150˚C
- Lead Temperature (Soldering, 4 sec.): 260˚C

### Operating Conditions

- Supply Voltage, \( (V_{CC}) \): 4.75 to 5.25 V
- Temperature, \( (T_A) \): 0 to +70˚C

<table>
<thead>
<tr>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{CC}</td>
<td>4.75</td>
<td>5.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Temperature, (T_A)</td>
<td>0</td>
<td>+70</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

†Derate molded package 7.7 mW/˚C above 25˚C, derate SO package 7.56 mW/˚C above 25˚C.

### Electrical Characteristics

(Notes 6, 7)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IH}</td>
<td>High-Level Input Voltage</td>
<td>((Figure 7))</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{IL}</td>
<td>Low-Level Input Voltage</td>
<td>(V_{CC} = \text{Min}, \ I_I = -12 \text{ mA})</td>
<td>0.8</td>
<td></td>
<td>-1.5</td>
<td>V</td>
</tr>
<tr>
<td>V_I</td>
<td>Input Clamp Voltage</td>
<td>(V_{CC} = \text{Min}, \ I_I = -12 \text{ mA})</td>
<td>1.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Low-Level Output Voltage</td>
<td>(V_{CC} = \text{Min}, \ (Figure 7))</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I_{OH}</td>
<td>High-Level Output Current</td>
<td>(V_{CC} = \text{Min}, \ (Figure 7))</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I_I</td>
<td>Input Current at Maximum Input Voltage</td>
<td>(V_{CC} = \text{Max}, \ V_I = 5.5V, \ (Figure 9))</td>
<td>1</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I_{IH}</td>
<td>High-Level Input Current</td>
<td>(V_{CC} = \text{Max}, \ V_I = 2.4V, \ (Figure 9))</td>
<td>40</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I_{IL}</td>
<td>Low-Level Input Current</td>
<td>(V_{CC} = \text{Max}, \ (Figure 8))</td>
<td>-1</td>
<td></td>
<td>-1.6</td>
<td>mA</td>
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<tr>
<td>I_{CCH}</td>
<td>Supply Current, Outputs High</td>
<td>(V_{CC} = \text{Max}, \ (Figure 10))</td>
<td>7</td>
<td>11</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I_{CCL}</td>
<td>Supply Current, Outputs Low</td>
<td>(V_{CC} = \text{Max}, \ (Figure 10))</td>
<td>8</td>
<td>11</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

### Switching Characteristics

\((V_{CC} = 5V, \ T_A = 25˚C)\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<tbody>
<tr>
<td>t_{PLH}</td>
<td>Propagation Delay Time, Low-to-High Level Output</td>
<td>(C_L = 15 \text{ pF}, \ R_L = 50\Omega, \ I_O = 200 \text{ mA}, \ (Figure 14))</td>
<td>DS75451</td>
<td>DS75452</td>
<td>DS75453</td>
<td>18</td>
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<td>t_{PHL}</td>
<td>Propagation Delay Time, High-to-Low Level Output</td>
<td>(C_L = 15 \text{ pF}, \ R_L = 50\Omega, \ I_O = 200 \text{ mA}, \ (Figure 14))</td>
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<td>DS75452</td>
<td>DS75453</td>
<td>18</td>
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<td>t_{TLH}</td>
<td>Transition Time, Low-to-High Level Output</td>
<td>(C_L = 15 \text{ pF}, \ R_L = 50\Omega, \ I_O = 200 \text{ mA}, \ (Figure 14))</td>
<td>DS75451</td>
<td>DS75452</td>
<td>DS75453</td>
<td>16</td>
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<td>t_{THL}</td>
<td>Transition Time, High-to-Low Level Output</td>
<td>(C_L = 15 \text{ pF}, \ R_L = 50\Omega, \ I_O = 200 \text{ mA}, \ (Figure 14))</td>
<td>DS75451</td>
<td>DS75452</td>
<td>DS75453</td>
<td>24</td>
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<td>V_{OH}</td>
<td>High-Level Output Voltage after Switching</td>
<td>(V_S = 20V, \ I_O = 300 \text{ mA}, \ (Figure 15))</td>
<td>0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_S</td>
<td>6.5</td>
<td>mV</td>
<td></td>
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</table>
Switching Characteristics (Continued)

Note 1: “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: The voltage between two emitters of a multiple-emitter transistor.

Note 4: The maximum voltage which should be applied to any output when it is in the “OFF” state.

Note 5: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 6: Unless otherwise specified min/max limits apply across 0˚C to +70˚C range. All typicals are given for VCC = +5V and TA = 25˚C.

Note 7: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Truth Tables (H = high level, L = low level)

DS75451

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<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
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<tr>
<td>L</td>
<td>L</td>
<td>L (ON State)</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L (ON State)</td>
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<td>H</td>
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<td>L (ON State)</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H (OFF State)</td>
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DS75452

<table>
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<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
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<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H (OFF State)</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H (OFF State)</td>
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<tr>
<td>H</td>
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DS75453

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<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>L (ON State)</td>
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<tr>
<td>L</td>
<td>H</td>
<td>H (OFF State)</td>
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<td>H</td>
<td>L</td>
<td>H (OFF State)</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H (OFF State)</td>
</tr>
</tbody>
</table>
Schematic Diagrams

Resistor values shown are nominal.

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Both inputs is tested simultaneously.

FIGURE 1. $V_{IH}, V_{OL}$

Each input is tested separately.

FIGURE 2. $V_{IL}, V_{OH}$

Each input is tested separately.

FIGURE 3. $V_{p}, I_{IL}$

Each input is tested separately.

FIGURE 4. $I_{P}, I_{IH}$

Each input is tested separately.

FIGURE 5. $I_{OS}$

Both gates are tested simultaneously.

FIGURE 6. $I_{CCH}, I_{CCL}$
DC Test Circuits (Continued)

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Input Under Test</th>
<th>Other Input</th>
<th>Output</th>
<th>Apply</th>
<th>Measure</th>
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<tr>
<td>DS75451</td>
<td>$V_{IH}$</td>
<td>$V_{IH}$</td>
<td>$V_{CH}$</td>
<td>$I_{OL}$</td>
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<tr>
<td></td>
<td>$V_{IL}$</td>
<td>$V_{CC}$</td>
<td>$I_{OL}$</td>
<td>$V_{OL}$</td>
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<tr>
<td>DS75452</td>
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<td>$I_{OL}$</td>
<td>$V_{OL}$</td>
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<td>$V_{IL}$</td>
<td>$V_{CC}$</td>
<td>$V_{OH}$</td>
<td>$I_{OH}$</td>
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<td>DS75453</td>
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<td>Gnd</td>
<td>$V_{CH}$</td>
<td>$I_{OH}$</td>
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<td>$V_{IL}$</td>
<td>$V_{IL}$</td>
<td>$I_{OL}$</td>
<td>$V_{OL}$</td>
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</tr>
</tbody>
</table>

FIGURE 7. $V_{IH}$, $V_{IL}$, $I_{OH}$, $V_{OL}$

Note A: Each input is tested separately.
Note B: When testing DS75453 input not under test is grounded.
For all other circuits it is at 4.5V.

FIGURE 8. $V_{I}$, $V_{IL}$

FIGURE 9. $I_{I}$, $I_{IH}$

Both gates are tested simultaneously.

FIGURE 10. $I_{CCH}$, $I_{CCL}$ for AND, NAND Circuits

Both gates are tested simultaneously.

FIGURE 11. $I_{CCH}$, $I_{CCL}$ for OR, NOR Circuits
AC Test Circuits and Switching Time Waveforms

Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.

Note 2: $C_L$ includes probe and jig capacitance.

FIGURE 12. Propagation Delay Times, Each Gate

Note 1: The pulse generator has the following characteristics: duty cycle $\leq 1\%$, $Z_{OUT} = 50\Omega$.

Note 2: $C_L$ includes probe and jig capacitance.

FIGURE 13. Switching Times, Each Transistor
Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{\text{OUT}} \approx 50\, \Omega$.

Note 2: $C_L$ includes probe and jig capacitance.

FIGURE 14. Switching Times of Complete Drivers
AC Test Circuits and Switching Time Waveforms (Continued)

Typical Performance Characteristics

Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{OUT} ≈ 50 Ω.

Note 2: C_{c} includes probe and jig capacitance.

FIGURE 15. Latch-UP Test of Complete Drivers

FIGURE 16. Transistor Collector-Emitter Saturation Voltage vs Collector Current
Typical Applications

*Optional keep-alive resistors maintain off-state lamp current at ≈ 10% to reduce surge current.

FIGURE 17. Dual Lamp or Relay Driver

FIGURE 18. Complementary Driver

FIGURE 19. TTL or DTL Positive Logic-Level Detector
*The two input resistors must be adjusted for the level of MOS input.

**FIGURE 20. MOS Negative Logic-Level Detector**
Typical Applications (Continued)

*If inputs are unused, they should be connected to +5V through a 1k resistor.

Low output occurs only when inputs are low simultaneously.

**FIGURE 21. Logic Signal Comparator**

**FIGURE 22. In-Phase Detector**
Physical Dimensions inches (millimeters) unless otherwise noted

SO Package (M)
Order Number DS75451M, DS75452M, DS75453M
NS Package Number M08A

Molded Dual-In-Line Package (N)
Order Number DS75451N, DS75452N, DS75453N
NS Package Number N08E
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