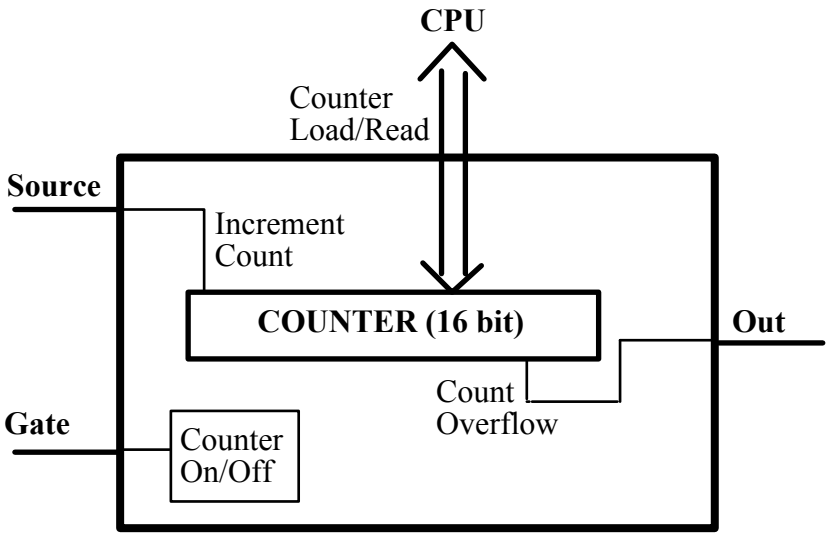
Digital Counter/Timers and How They Work

Counter/Timer Logic can be represented schematically as shown below,



Clock Timers use a *Source* to increment a *Counter* . Whenever the counter increments past its maximum value, an Overflow is generated which pulses the counter *Out.* The *Gate* is used to enable or disable the clock function.

Clock Timers can be used for many types of time keeping and/or event counting functions.

To Count Events:
a) Disable Gate to turn off Counter.
b) Connect Event signal to Source
c) Load Counter with Zero.
d) Enable Gate to turn on counter.
e) Read event count from Counter

To Time Events:
a)Connect a known frequency pulse train to the Source to increment the counter.
b)Disable the Gate to stop the Counter.
c)Load the Counter with zero.
d)Enable the gate when the event starts and Disable the gate at the end of the event.
e) Read the Counter contents. Event time = Count/Timebase.

LabVIEW “Easy I/O” Counter-Timer VI’s

