

ECE 480

Pre-Proposal

Ethernet Integrity Analyzer

Sponsored By Texas Instruments

Design Team 7:

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Executive Summary

Due to the expanding use of Ethernet technology, the need for a troubleshooting device is becoming more of a necessity. To fulfill this need, we intend to put Texas Instruments at the forefront of this industry by creating an Ethernet Integrity Analyzer. This handheld device will have the capabilities of performing a series of cable diagnostics over an Ethernet line. These diagnostics will detect and locate faults such as, cable damage, water ingress, and manufacturing flaws. In addition, the device supports the new technology of Power-over-Ethernet which will decrease power consumption and lower cost of operation.

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Introduction

Ethernet has become one of the most popular and most widely deployed network technologies in the world. In today's increasingly complex internet and client-server environments, the need for Ethernet Analyzers is more essential. There are many sophisticated features and modern technologies that Ethernet Analyzers poses. ECE 480 Design Team 7 will design and develop a handheld analyzer for Ethernet networks. Our Ethernet Integrity Analyzer (EIA) will automatically execute a diagnostic suite, and perform integrity checks when plugged into a standard RJ-45 Ethernet port. The EIA will display the results of the tests by its on-board color touch-screen display and can optionally tag and store the results in a data log to be later uploaded to a host PC for off-line analysis. The EIA is powered from one of three sources; the PoE port of power if detected on the link; a DC input supply or, if neither of the line sources are detected, batteries.

Background

Currently, there is a limited amount of diagnostic tools for Ethernet Networks. Many of the current tools require significant knowledge of networks and can take a significant amount of time to accurately diagnose. TI has a number of existing technologies that we will incorporate to create a new network analyzing tool. The most significant is the TLK100 Ethernet PHY, a physical layer device that offers three capabilities Time Domain Reflectometry

(TDR), Active Link Cable Diagnostic (ALCD) and Digital Spectrum Analyzer (DSA). A new technology being used is Power-over-Ethernet which will be incorporated through the TPS2376 PoE PD Controller. Another highlighted hardware technology is the ARM Cortex M3 MCU. The software will be developed using StellarisWare which is used to program the microcontroller in C++. The software will also be written using IAR embedded workbench which is a development environment for programming ARM-based embedded applications.

Objectives and Design Descriptions

Our design will diagnose a RJ-45 Ethernet line to determine its integrity. The Stellaris® LM3S9B96 Development Board (shown in Figure 1) presents a platform for developing systems around the advanced capabilities of the LM3S9B96 ARM® Cortex™-M3 based microcontroller. The LM3S9B96 is a member of the Stellaris Tempest-Class microcontroller family which contains capabilities such as 80MHz clock speeds, an External Peripheral Interface (EPI) and Audio I²C interfaces. To support these features, the DK-LM3S9B96 includes a rich set of peripherals found on other Stellaris boards. This development kit will lead us to design and test the implementation of our Ethernet Integrity Analyzer. The kit also provides some features such as, Controller Area Network (CAN), 10/100 BaseT Ethernet, 1MB flash memory and LCD monitor.

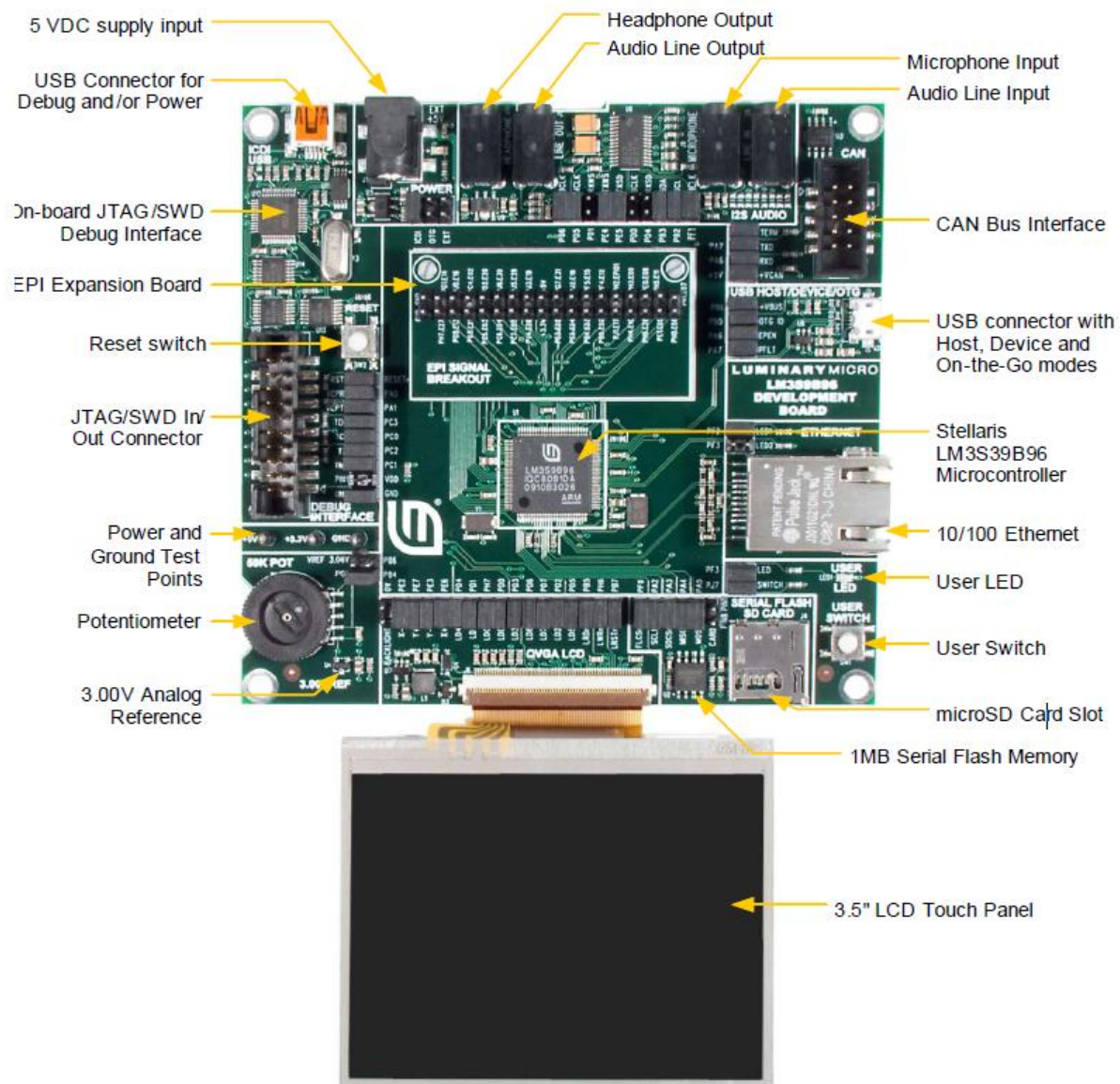


Figure 1: Development Board

The Development Board is supplied by 4.75-5.25 V dc voltage from USB cable, USB micro-B cable (USBs connected to a PC) or DC power jack. Power-over-Ethernet (PoE) technology will be used when power is detected by the TPS2376-H PoE PD. The power used from the Ethernet line will be converted to +5V DC in order to be used to power the Development Board. To have a rechargeable battery system with a wall adapter, the bq24070

Single-Chip LI-ION Charge and Power-Path Mgmt IC will be used. Once this power has been converted to +5V DC, it can be logically combined with the PoE using Option 1 illustrated in Figure 2. This will allow for switching between the rechargeable battery system with wall adapter and the PoE. The EIA will be designed such that the PoE will be the primary power supply with the batteries and wall adapter as an alternate. The battery will supply power when no other power source is detected.

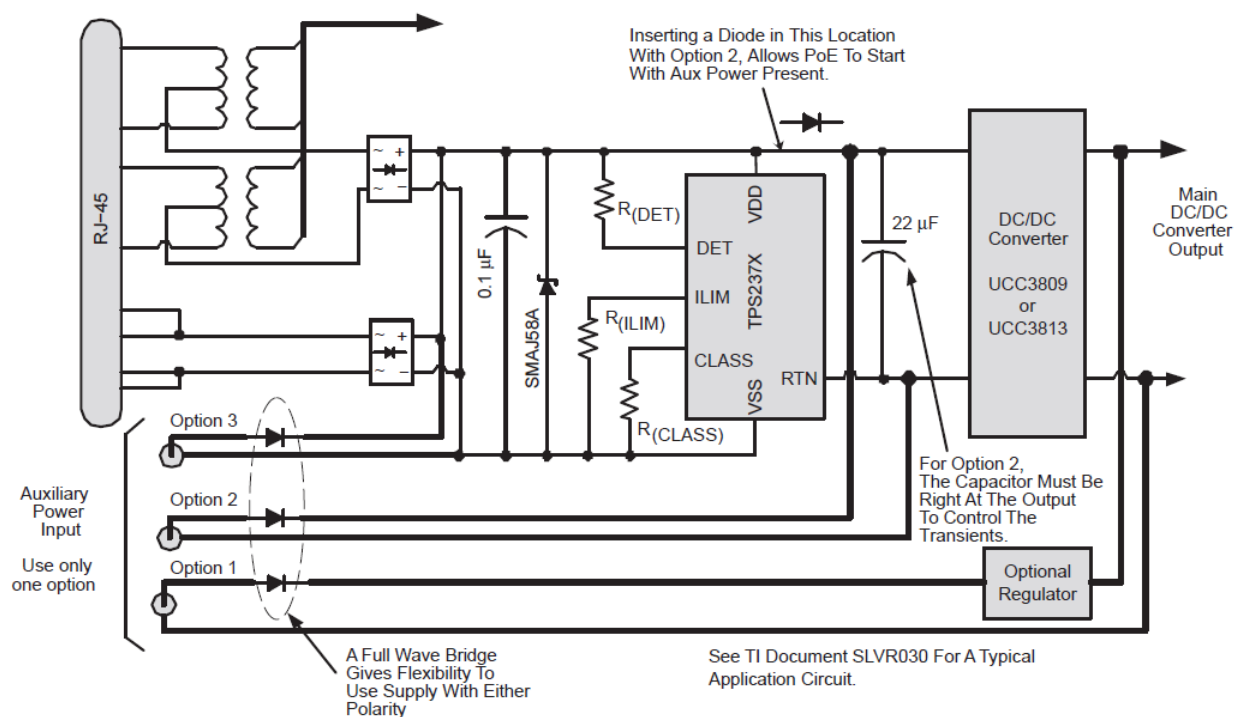


Figure 2: Power-over-Ethernet Schematic

The TLK100 will be used to provide the connection between the Media Independent Interface (MII) and the Media Access Controller (MAC). The mixed-signal processing is used by the TLK100 to equalize, recover data, and to correct error. The TLK100 is able to handle large amounts of interference and noise, creating a robust system. It has the capability to run Time

Domain compliance Reflectometry (TDR), Active Link Cable Diagnostic (ALCD), and Digital Spectrum Analyzer (DSA). Time Domain Reflectometry (TDR) will be used for locating errors in the cable as well as measuring the length of the cable. By analyzing reflections of a test pulse the TDR will be able to calculate impedances throughout the line and the locations of those impedances. Active Link Cable Diagnostic (ALCD) is capable of measuring the overall cable length with even higher accuracy than the TDR. Finally the Digital Spectrum Analyzer (DSA) will be used to find the magnitude of the frequency response (119.2 Hz Resolution).

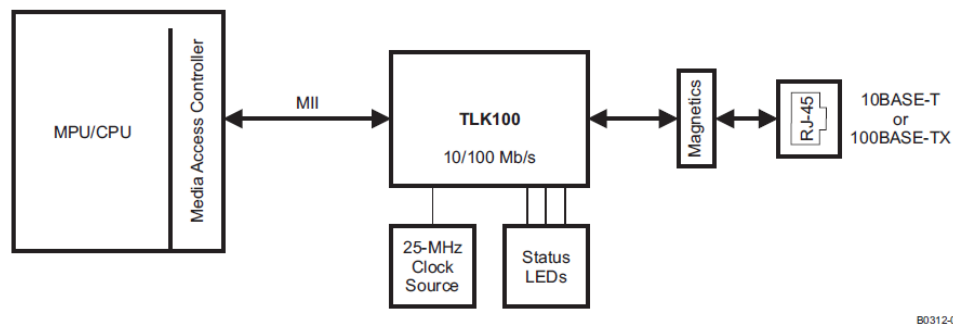


Figure 3: System Diagram

This single port transceiver will allow us to perform cable diagnostics. The TLK100 uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations. Also, TLK100 supports Active Link Cable Diagnostic. This offers a passive method to estimate the cable length during the active link. The other diagnostic our design will cover is analysis of the channel frequency response. The TLK100 offers a unique capability of Digital Spectrum Analyzer.

Below in figure 4 is a block diagram of the entire project.

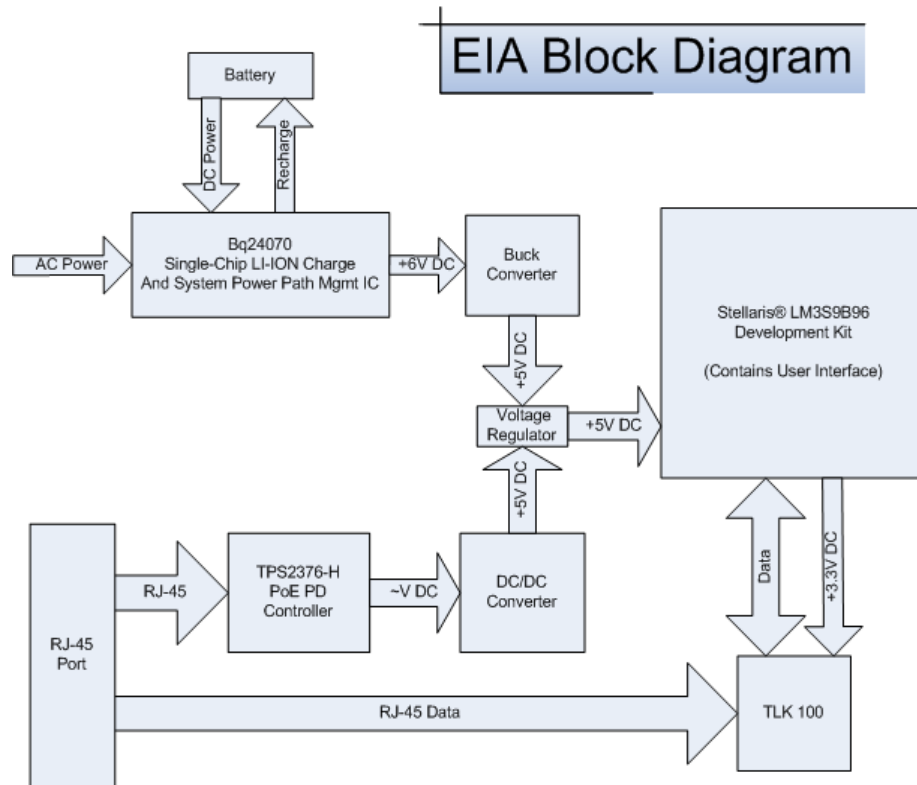


Figure 4: Ethernet Integrity Analyzer Block Diagram

Risk Analysis

Great care must be taken when working with Power over Ethernet. As detailed in the IEEE 802.3af standard, Power over Ethernet can provide between 44-57 volts with a current between 10- 350 mA. Even 50-150 mA can cause extreme pain, respiratory arrest and sever muscle contraction. We also must be careful when working with the AC adapter and make sure that we do not overcharge the Lithium Ion battery. In implementing the DC/DC converter resistances must be picked in order to get a desired voltage. Incorrect choices for the resistance could damage the development kit along with any other microchips in the circuit. Static electricity is also a concern. Proper care should be taken to make sure no chips get destroyed from the discharge of static electricity.

Project Management Plan

<i>Name</i>	<i>Non-Technical Role</i>	<i>Technical Role</i>
Ahmed Alsinan	Documentation Preparation	POE to battery switching
Andrew Christopherson	Web Design	Programming microcontroller/LCD display
Sedat Gur	Lab Coordinator	DC/DC conversion
Mark Jones	Manager	Programming TLK100 Ethernet PHY
Brian Schulte	Presentation Preparation	Battery/AC Power Implementation

<i>Week</i>	<i>Tasks</i>
Week 1: 1/11 – 1/17	• Meet with team • Receive Project Description • Meet with Facilitator
Week 2: 1/18 – 1/24	• Begin Research on project • Conference call with sponsor
Week 3: 1/25 – 1/31	• Request critical parts from TI
Week 4: 2/1 – 2/7	• Pre-Proposal Due • Request additional parts
Week 5: 2/8 – 2/14	• Voice of Customer Due
Week 6: 2/15 – 2/21	• Receive Development Kit • Final Proposal Due • Oral Presentation
Week 7: 2/22 – 2/28	• Begin coding touch display • Work on interface between microcontroller and Ethernet PHY

	• FAST Diagram Due • Design Day Program Page Due
Week 8: 3/1 – 3/7	• Begin work on Power Over Ethernet controller • Code Ethernet PHY to run diagnostics
Spring Break: 3/8 – 3/14	• Time Off
Week 9: 3/15 – 3/21	• Progress Report #1 • Demo of project • Complete implementation of switching between POE and batteries
Week 10: 3/22 – 3/28	• Student technical lecture • Implement Passive mode for analyzer
Week 11: 3/29 – 4/4	• Individual application notes due
Week 12: 4/5 – 4/11	• Progress Report #2 • Second demo of project
Week 13: 4/12 – 4/18	• Design Issues Paper • Working model of Ethernet Analyzer
Week 14: 4/19 – 4/25	• Finish Poster and Final Report • Practice Design Day Presentation
Week 15: 4/26 – 5/2	• Design Day • Turn in Engineering Notebooks

Budget

Since TI will be providing most of the parts needed for this project, our group has very little control over the cost of the final design. Our 500 dollar budget will be used for various minor tools and parts as they are needed.

References

"Interface - Ethernet - TLK100 - TI.com." *Focus Home Page*. Web. 02 Feb. 2010. <<http://focus.ti.com/docs/prod/folders/print/tlk100.html>>

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