

ECE 480 Proposal
Compact DC/AC Power Inverter, Team Seven
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Introduction

Power inverters are used to convert direct current (DC), such as that from a battery, to alternating current (AC), such as what can be drawn from a standard wall outlet. These devices are used in a large number of applications, including conditioning energy derived from solar cells into usable power and supplying electricity to household appliances during power outages. These devices are usually large, around the size of a cooler.

Team seven will design and build their own power inverter inspired by the *Little Box Challenge*, a contest hosted by Google and IEEE. The idea of this challenge is to create an inverter both very small, 40 cubic inches, and also powerful enough to rival the output of its larger counterparts. Accomplishing this small form factor would be an important step in attaining widespread high power inverter utilization. This would also increase the feasibility of solar power generation for the masses in the future.

The goal is to achieve a 1 kilo-volt-amp power output. The process involves inputting DC, stepping the voltage to the AC peak value, and using pulse width modulation from a microcontroller to drive transistors. This will create a 60 Hz sinusoid, which is the set frequency standard for wall outlets in the United States. Harmonic filtering is required before the output to comply with FCC regulations. Any inefficiency in the inverting process results in excess heat, so close attention will be paid to the efficiency of components and heat dissipation.

Background

The motivation behind team seven's project is based on a push from industry applications. In residential, commercial, and industrial settings, powerful inverters can be quite large. The extra space required can determine whether or not a design is feasible. Shrinking these inverters significantly is an important step in making their widespread use practical. Google and IEEE have teamed up to create a contest in an effort to bring such a device into existence. They also listed several semiconductor manufacturers that provide the necessary technologies to make it possible, which include Gallium Nitride and Silicon Carbide components.^{[2][3]}

The contest guidelines that these Google and IEEE have laid out are as follows: to have a power density of 50 W/in^3 , a physical size of less than 40 in^3 , and the ability to invert a 450 volt DC input to a 240 volt 60 Hz AC output. The inverter must perform the aforementioned with an efficiency of 95%, maintain an enclosure temperature of less than 60 degrees celsius, and comply with FCC Part 15 B electromagnetic compatibility requirements.

The IEEE/Google inverter redesign will have broad applications and must be easily altered to handle new environmental constraints such as dust, temperature extremes, and vibrations. The installation process of these inverters should be easy as they will be able to be oriented numerous ways without sacrificing the integrity of the design. With the new redesign, the inverters will need to be easily mass produced; specialty components and materials will need to be avoided. Applications of this inverter are not limited, but rather will spread over all of the power electronics industry. However, given the restrictions of the design presented by Google and IEEE, primary application will have applications within solar array power generation.

The team's guidelines for the power inverter redesign are structured around these *Little Box Challenge* technical details, though exact implementation will not occur due to time and price constraints. Rather, self-imposed constraints will be based on research and what the sponsor deems possible with the allotted time.

Objectives and Requirements

Due to a 15 week semester time requirement, the Google/IEEE guidelines are modified. Changing the voltage requirements will allow for an appropriate time table. The group will also have a modified power requirement, but the physical size and temperature specifications will remain the same as the Google/IEEE guidelines. Throughout the design process the group will be pushing different component types to their limits to identify baseline best practices. The team's design parameters are outlined in the table below.

Table 1: Design Specifications

Parameter	Requirement (Nominal)
Maximum Load	1 kVA
Power Density	> 25 W/in ³
Volume	< 40 in ³
Voltage Input	200 V DC
Voltage Output	120 V RMS AC
Frequency Output	60 Hz
Maximum Outer Temperature	< 60 °C
Electromagnetic Compliance	FCC Part 15 B

FAST Diagram

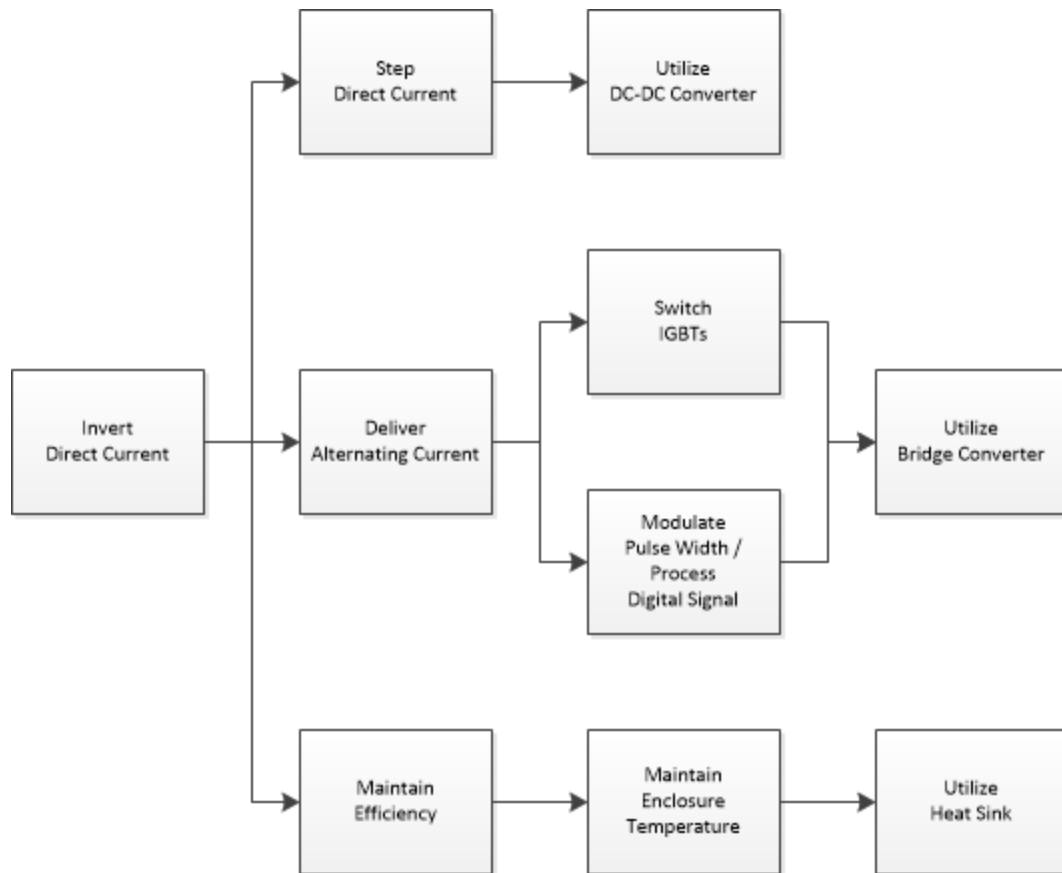


Figure 1

The basic function of the design is to invert the DC input into an AC output. Secondary functions include stepping the DC, delivering AC, and maintaining efficiency. Each of these functions can be seen in figure 1 above. To invert DC, the inverter must first step the DC to the AC peak amplitude. Direct current can be stepped up and down with the use of a DC-DC converter. Current is alternated by switching isolated-gate-bipolar-transistors on and off using pulse width modulation from a microcontroller. High efficiency will ensure less power is dissipated as heat. This is important because the enclosure will not contain a large excess of room, so maintaining an acceptably low temperature will be more difficult with a compact heat sink.

Conceptual Designs Outline

The most practical way to achieve the final power goal will be to split the design process into a number of phases. This is largely due to the fact that lower voltages are simpler to work with in regards to efficiency and heat considerations. There are four phases, each described below:

Phase One: The group will model four initial designs using PSpice. Special attention will be paid to the efficiency of these designs, which is amongst the most important design parameters. The group will buy a commercial inverter (designed for 12 V DC use), reverse engineer the layout, and model; close attention paid to board layout.

Phase Two: The group will analyze the PSPICE models from phase one and select the best with regards to efficiency and practicability. This design will be prototyped and the current will be increased to find the power limits of the material being worked with beginning with silicon transistors. Heat dissipation solutions will begin being formed.

Phase Three: The proposed design from phase one is prototyped using updated materials (Gallium Nitride and/or Silicon Carbide). Power is stepped up to test new materials for their limit. Heat sink solutions are expanded to include the use of aluminum, synthetic diamond, and thermo-electric coolers. Power is stepped up a final time.

Phase Four: The chosen design is built with the use of printed circuit boards, custom enclosure, and heat solutions. 100+ hours of testing is performed at objective specifications while design issues are troubleshooted and solved.

Conceptual Design Details

H-bridge using IGBTs (Figure 2): A set of four insulated-gate bipolar transistors configured in H-formation, using pulse width modulation from a TI MSP430 to achieve as high-resolution 60 Hz sine wave. This design would require gate drivers on either side of the bridge that would drive either the high side or low side IGBTs. Utilizing gate drivers allows a level of control and isolation between the MSP430 PWM pins and the gates of the IGBTs. The output rails of this bridge would require a RLC resonant filter to filter out the switching artifacts and leave a high resolution sine wave.^[4]

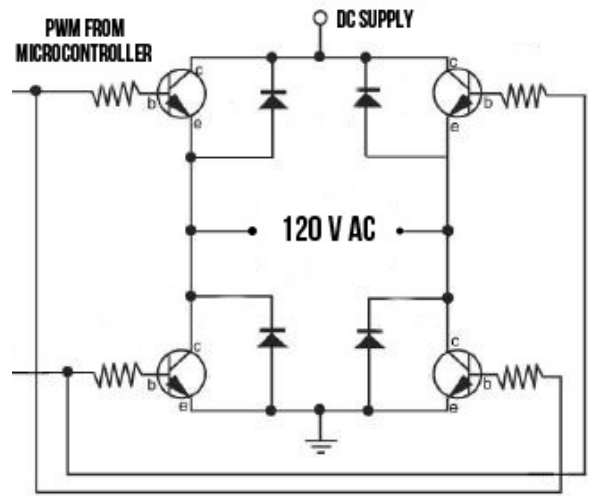


Figure 2: H-Bridge using IGBT's

Quantized-step MOSFET with output transformer: Metal-oxide semiconductor field-effect transistors are configured to deliver $\frac{1}{4}$, $\frac{1}{2}$, $\frac{3}{4}$, and full voltage of positive and negative peaks, triggered with a TI MSP430 to create a four step sine wave. This sine wave would not have a high resolution but offers respectable efficiency in the creation of the wave. The outputs of the individual MOSFETs creating each piece of the sine wave can only be as large as the supplied DC voltage rail so the resulting stepped output is then increased to the desired line voltage of 120 volts by utilizing an output transformer.

555 bridge design (Figure 3): A 555-timer is biased to create a continuous periodic 60 Hz pulse that is used to trigger a pair of NPN and PNP transistors. The transistors are used as valves to control the current direction from the energy stored in a resonant CL (capacitor-inductor) circuit tied to the drains of the NPN and PNP transistors. This CL circuit is designed to serve as a sharp resonance filter at 60 Hz. This filter has a very high Q which only allows the 60 Hz harmonic to pass through. This sine wave is then stepped up using an output transformer to the desired output line voltage of 120 volts RMS.^[5]

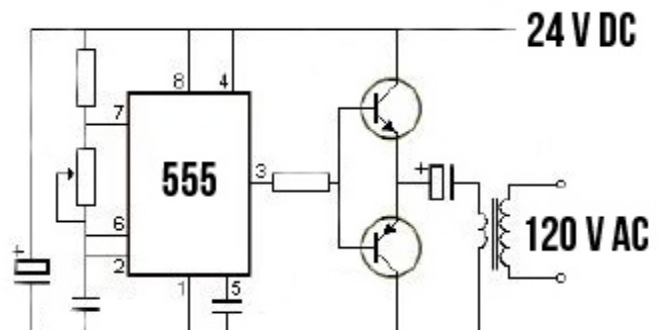


Figure 3: 555 Bridge Design

Proposed Design Solution

Based on preliminary testing using the above designs the team has decided to use a variation of the H-bridge to create the desired output based on the specifications given. The H-bridge offers the highest level of efficiency compared to the other industry standards and fits within the predetermined size constraint. The H-bridge will be made up of four different N-channel IGBTs that are used to create the desired AC across the output load. This is done by alternating the path of the DC supply rail across the load and to ground every 8.33 ms which results in the desired 60 Hz waveform.

The H-bridge is controlled by two different Pulse Width Modulated (PWM) signals - each signal is 180 degrees out of phase with the other. These PWM signals are created from a pure 60 Hz sine wave that is created within the microcontroller. The PWM signals are then routed to the input of the gate driver located between the microcontroller and IGBTs. From here the gate driver controls the voltage supplied to the gates of each IGBT on one side of the bridge. This is a crucial part of the design because the gate drivers guarantee that either the high side or low side transistors will be on at any instant in time, thus stopping the DC voltage rail from ever being shorted directly to ground.^[6]

Once the gate driver has been triggered by the PWM signal the respective gate on each side of the bridge is triggered and current is allowed to flow from the DC rail through the load and to ground. The output of the bridge is a PWM signal that has been amplified to the same value of the rail voltage, so in order to create a 120 Volt RMS sine wave the DC rail in this design must be set 170 volts DC. After this amplified PWM signal is created the next step is to filter the signal and get rid of the high frequency switching that is present in the PWM signal. A resonant filter is used to pull out only the 60 Hz fundamental harmonic from the PWM signal, thus resulting in a clean 60 Hz sine wave.

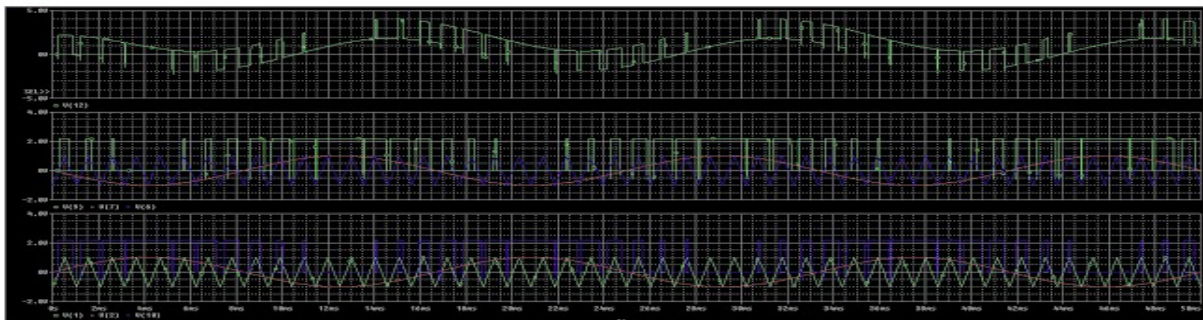


Figure 4: PSpice Phase One and Two Results

The required 170 volt DC rail comes from a series of DC to DC converters that will step the supplied DC voltage. These converters all must be rated at the final power specification of the inverter because they will be in series with the input supply and output load. This high power throughput makes these parts very hard to find to fit the size constraint of the teams project, so there is a possibility of the group building a switching supply to achieve the desired power and fit within the enclosure.

In order to power the microcontroller used to create the PWM feeding the gate drivers another set of DC to DC converters will be used to drop the supplied voltage down to a usable voltage that will power the microcontroller. This voltage is approximately 5 volts at a very lower current so the size of the needed DC to DC converter is small because of the low power constraints.

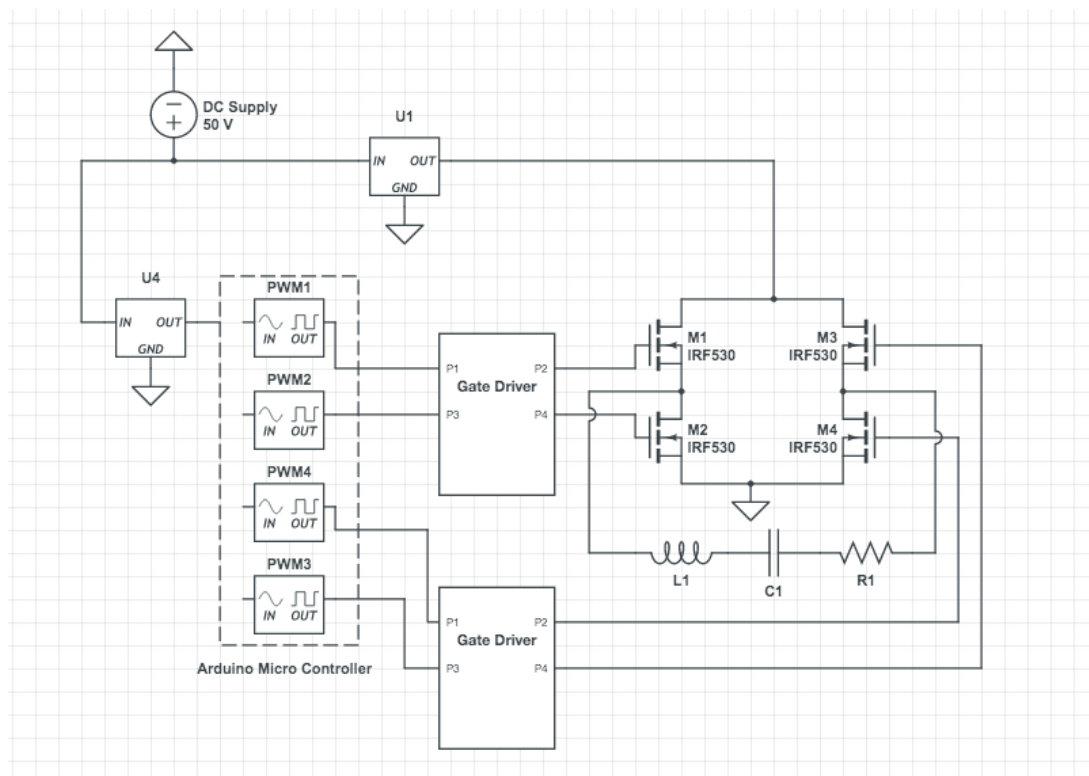


Figure 5: Proposed Final Design

Risk Analysis

The two main design challenges that the group faces are heat and physical size, both of which are a direct result of increasing the power through the components. Components will be spaced closer together, but this will make heat dissipation evermore crucial.

Containing the circuitry inside a 40 in³ box will limit air flow around the electronics and cause internal temperatures to rise quickly. To combat rising temperatures, four main areas will be researched and developed for the deliverable: materials, conduction of heat removed from the electronics, the convection of air inside the enclosure, and the design of heat dissipation systems.

In designing these power electronic systems, the group will look at the effective upper temperature limits for different components. The group plans on testing different components under like conditions. From the results it will be determined which components, Gallium Nitride and/or Silicon Carbide, would fit best within the constraints of the design. Copper, aluminum, and synthetic diamond will be tested for heat dissipation effectiveness. Effective surface area and materials in contact with the circuitry will be the primary conduction focus. Increasing fluid flow inside the enclosure is critical to increase convection for dissipation. Three methods are currently being considered: heatsinks, fans, and vents.

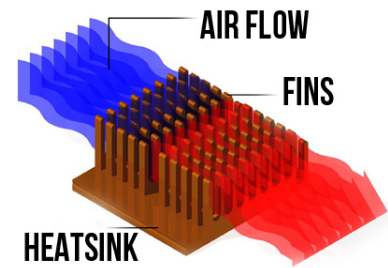


Figure 6: Heat sink air flow^[7]

The group will most likely use silicon carbide for circuit materials after silicon components, diamond and thermal grease for conduction, and copper - perhaps with fans or thermo-electric coolers - for the convection design. The final dissipation design will be a heat sink given the limited space inside the enclosure.

With higher power, considerations for safety will also be necessary. While the inverter is in operation it will be crucial that no components could be shorted or that an individual could touch a live component. The heat sink will be grounded, the size of case openings will be limited, and all external connections - the four wires for input and output - will be insulated and secured.

Project Management Plan

Team seven consists of five members. All five will participate in building and testing:

- Philip Beard - webmaster and design modeling; responsible for the creation and maintenance of the team's website and for design modeling and research with PSPICE
- Jacob Brettrager - document preparation and microcontroller integration; responsible for group resource management and interfacing the digital and analog system components
- Jack Grundemann - presentation preparation and heat analysis; responsible for maintaining presentation documents both informally and formally to both peers and faculty, focuses on the design of heat dissipation devices for the enclosed circuitry
- Stanley Karas - management and partially responsible for design modeling and architecture research; team liaison between facilitator, sponsor, and group
- Travis Meade - lab coordinator and microcontroller programming; responsible for acquisition and management of materials and supplies, procurement logistics

The timeline is detailed in the GANTT chart below. Careful attention was paid to allow buffers for each task to avoid delays in the overall design process.

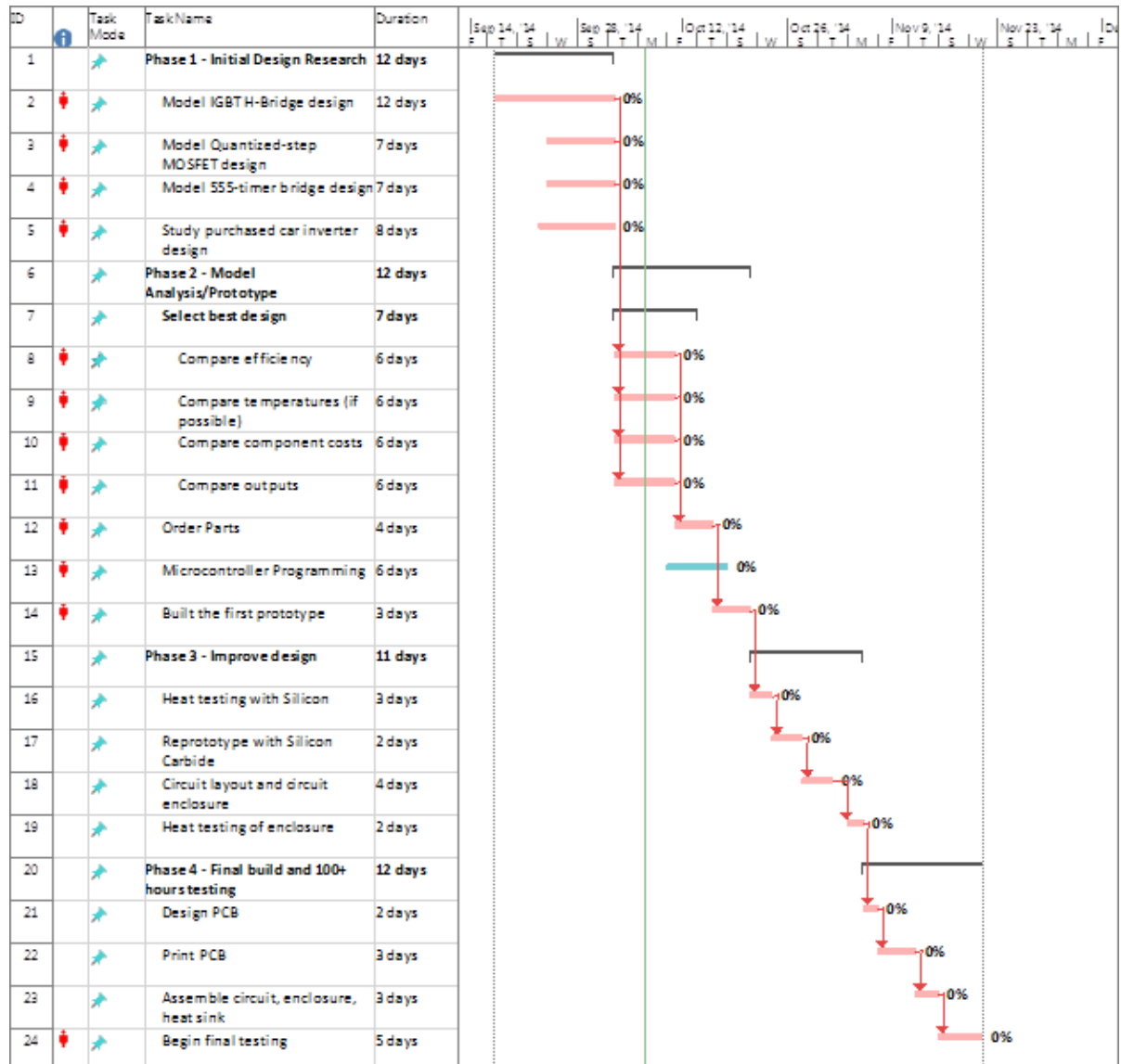


Figure 7: GANTT Chart

Budget

A thorough cost analysis began when the preferred design was chosen following completion of phase one.

Table 2: Line Item Budget

Item	Price	Quantity	Total	Description
UCC27211A	\$5.50	2	\$11.00	120 volt Gate Driver
C2M0025120D	\$91.61	4	\$366.44	Silicon Carbide MOSFETs
DC-DC Converter (50V - 3V)	\$32.15	3	\$96.45	Supply Rail for Micro Controller
Heat Sink	\$5.00	1	\$5.00	Aluminum Milled Heat Sink
Enclosure	\$8.00	1	\$8.00	High Temp Enclosure
Arduino Microcontroller	\$4.95	1	\$4.95	ATMega328
PCB	\$7.00	1	\$7.00	Printed Circuit Board
		TOTAL:	\$498.84	

As shown above, the inverter's most expensive components will be the high power transistors. Initial testing will begin with less expensive transistors (silicon) which the group already has available. These final transistors have a high price because they are new and expensive technologies; they were chosen for their high efficiency and power throughput. The case will be manufactured by DECS using 3D printing provided at a specified price per ounce; once a final design, printed circuit board (PCB), and heat sink are chosen, the exact dimensions of the case will be known.

References

- [1] [IEEE/Google Little Box Challenge Official Website](#)
- [2] [USCi Silicon Carbide Transistors](#)
- [3] [Transphorm Gallium Nitride Transistors](#)
- [4] [MIT Open-Courseware Power Electronics Notes](#)
- [5] [DC/AC Pure Sine Wave Inverter](#)
- [6] [555-Timer Inverter](#)
- [7] [ECNMag Official Website](#)