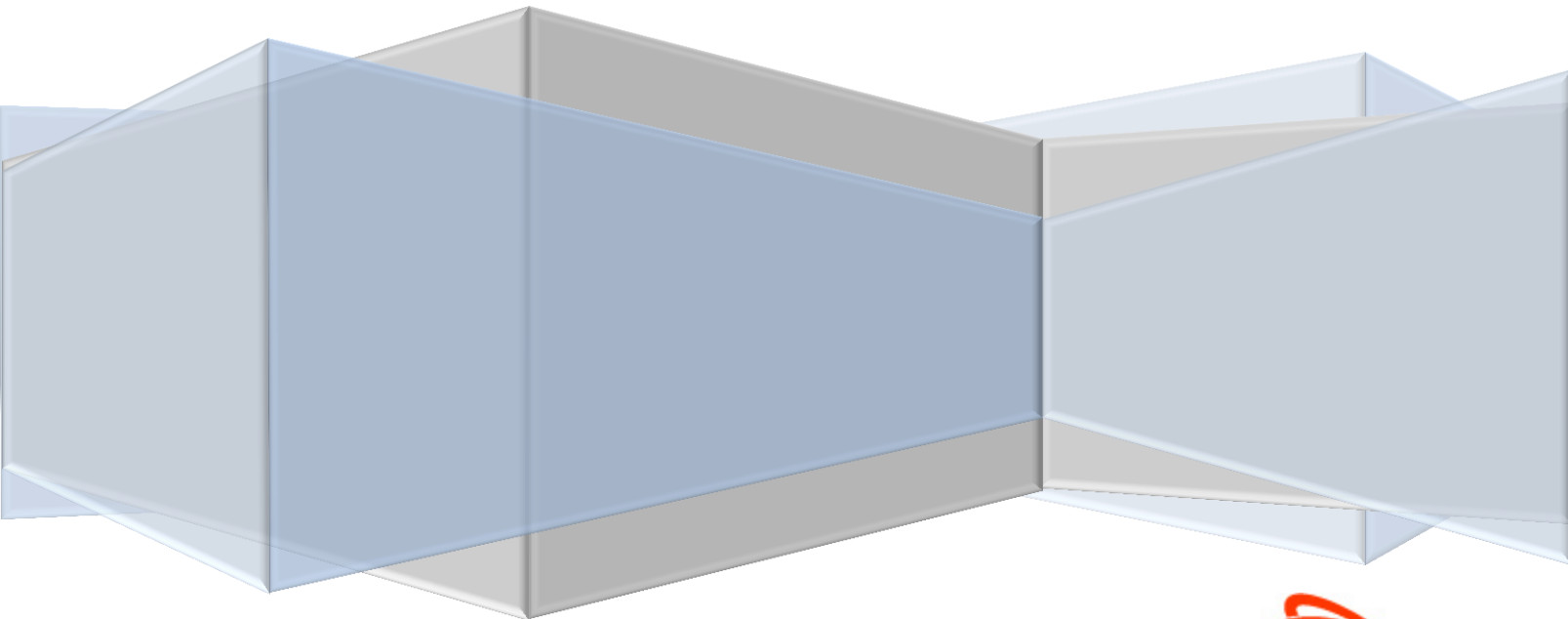


**MSU College of Electrical and Computer Engineering**

# **Load Metering and Transmission**

**ECE 480 Design Team 5**

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Project Sponsored by ArcelorMittal



## **Project Summary**

ArcelorMittal, a steel company in Burns Harbor, Indiana, has asked Design Team 5 to create a backup transmission system to monitor power usage at their steel mills. ArcelorMittal produces most of the power that they use from three onsite steam turbine generators. The rest of the power must be purchased from the Northern Indiana Public Service Company (NIPSCO). It is important that they understand the amount of power usage at any given time so that they do not over buy power. ArcelorMittal currently has a system in place to monitor their power usage. Team 5 must design a redundant system that can provide this data to the control center if the current system were to fail. After consideration of the problem, especially the distance that the signal must be transmitted, Team 5 decided to use Pulse Width Modulation to transmit the power signal. This system would allow encoding of the transmitted signal so that it could be delivered without attenuation as long as the frequency of transmission was low enough. Pulse Width Modulation needs a transmitter or modulator and a receiver or demodulator to successfully transmit the signal. Team 5 designed each of these components and then tested them using a long stretch of cable. The project was successful and the error in transmission was very low. A robust, reliable, and cost effective solution can now be implemented as a backup to the existing system.

THANK YOU!

Special thanks to our Sponsor, ArcelorMittal, and their representatives Eduardo Ferragini and Thomas Whittaker, for their dedication and willingness to see this project through to conclusion.

Special thanks to our facilitator, Joydeep Mitra, for aiding us in the design process.

Special Thanks to our instructor, Michael Shanblatt, as well as all the other classroom guests who helped us in our learning process.

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We have learned a lot from this project and will always be grateful for all the people that supported us in our learning experience.

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#### NOTE ON ABBREVIATIONS

Abbreviations are used throughout the paper, but will be stated once in full text with the abbreviation in parentheses before they are used.

All scientific units in this paper use SI prefixes and are in scientific notation unless otherwise noted.

Units include:

s – second(s)

m – meter(s)

C – Celsius

V – Volt(s)

A – Amp(s)

W – Watt(s)

$\Omega$  – Ohm(s)

H – Henry(s)

F – Farad(s)

# CHAPTER 1

## INTRODUCTION

ArcelorMittal is a company in Burns Harbor, IN that produces steel from its raw components. Their facility requires the power of several small cities, and it is crucial that the processes are continued so that revenue is not lost. Damage can also occur to some of the mills used in the steel making process, if operations were to cease for a long period of time.

Michigan State University's Design Team 5 was charged with the task of working with ArcelorMittal to monitor the plant's power consumption. The plant produces around sixty percent of the power that they require through steam turbine generation. The rest must be bought from the local power company, NIPSCO. It is important to know at any time how much power is being used by the plant so that ArcelorMittal can buy the right amount of power from NIPSCO. Any power that is bought in excess of ninety-four megawatts is very expensive.

The existing power monitoring system is an old system, and ArcelorMittal is worried about its reliability. The design team's task is to develop and implement a redundant transmission system that can act as a backup to the existing system. The new system would run in parallel and cannot affect the existing system in anyway.

Several Ideas were put forth to transmit the data, including Pulse Width Modulation (PWM), Frequency Hopping Spread Spectrum (FHSS), Ethernet Remote I/O, wireless Frequency Modulation (FM) transmission, and Fiber Optic transmission. Currently, FHSS is the common way to transmit these power signals. These systems are designed by manufacturers who target the power industry, and because of this the designs are too expensive for the allowable budget. The transmission of FHSS is also wireless and needs a line-of-sight transmission path. After weighing the pros and cons of each system, it was decided that Pulse Width Modulation is the optimal solution for the problem. Using the budget and time constraints that were provided by Michigan State University, a plan was established to be completed by design day.

## BACKGROUND

ArcelorMittal's steel operations in Burns Harbor, IN routinely require up to approximately 100MW of total facility power usage. Due to the cost of electrical power and the company's limited generating capabilities, it is vital to have immediate and uninterrupted knowledge of the current total electrical load throughout the facility. To monitor the total facility electrical load, ArcelorMittal needs to have the ability to transmit a signal, containing information on the electrical loads at each plant, to the central control room. Based upon routing estimates the wired transmission path could be located up to one mile away.

At each plant there are a series of transducers that convert the plant's total electrical load to a 0 to 100 mV analog signal. A voltage of 0mV represents 0MW of power usage and a voltage of 100mV represents a known ceiling value of power usage for a particular plant. Any linear variation between 0 to 100mV from the transducers represents a linear variation in power usage of the plant between 0MW and the ceiling value. The voltage signal from the transducers is then converted into a frequency modulated (FM) signal which has a deviation of 10-30Hz with a 1020Hz carrier. The signal is sent to the control room over a shielded, twisted-pair cable. At the control room the FM signal is converted to a 1 to 5V analog variation which is read by a Programmable Logic Controller (PLC). This information is then stored in the company's computer system.

The current system of signal transmission is the same system which was originally implemented when the facility was built over fifty years ago. ArcelorMittal would like to have a redundant way to transmit the electrical load signal from the plant to the control room due to the age of the current system, its unknown level of reliability, and the critical nature of the electrical load information being transmitted.

ArcelorMittal has asked ECE480 Design Team 5 to create a new, reliable and robust system of electrical load signal transmission, specifically for the company's hot rolling plant. The new system must begin with using the existing 0 to 100 mV analog signal from the load transducers at the plant, specifically within the 138kV switchyard, and end with a 1 to 5V or 4 to 20mA signal at the PLC, in the Central Dispatch control room.

PWM is an inexpensive, reliable solution that can provide the redundancy required. PWM is conceptually simpler than FM and can be produced at half the cost. It is robust and the theory is well developed. This circuit will provide a critical back-up system and could potentially save ArcelorMittal a lot of money if there current system were to ever fail.

## CHAPTER 2

### SELECTING A DESIGN APPROACH

#### DESIGN SPECIFICATIONS

ArcelorMittal was very open to new design ideas from the team, but did provide a few restrictions. The design chosen by the team had to use the already existing 0 to 100 mV electrical load analog signal provided by the load transducers at the hot mill. The design had to then provide a linear output within a range between 1 to 5 V and 4 to 20 mA at the output as a scaled representation of the input to be totalized by a PLC in the control room. The designed solution had to be capable of fitting inside the cabinet which houses the transducers in the switchyard and the cabinet which houses the PLC at the control room. The chosen design had to also be capable of running in parallel with the current electrical load signal transmission system from the hot mill and must be implemented with zero down time of the hot mill or the current signal transmission system. The chosen design had to be able to transmit the electrical load signal potentially up to one half mile. The team also had the option to run a second cable from the hot mill to the control room to transmit the electrical load signal, if it was desired.

Key specifications included:

#### Accuracy

The goal of the project is to transmit the load signal over a long distance. Depending on the application, a high standard of accuracy is required. A percentage error of positive and negative two percent is considered acceptable. Keeping the accuracy as low as possible is one of the major goals of the project.

#### Reliability

Reliability is also an important requirement. As an alternative signal transmission system, it will be running 24 hours a day and seven days a week to back up the current system. At any given time the system must be working.

#### Cost

As an alternative signal transmission system, the cost of the project needs to be kept as low as possible, and within the confines of the given budget of five-hundred dollars. Intuitively, lower-cost solutions are favored to give room for error and possible changes in the project design.

#### Compatibility

The signal transmission system will be working in parallel to the current system. The system must implement the collective input from the transducers in the switchyard and be able to output to the PLC in the control room within the specification requirements.

#### Power Consumption

The power consumption needs to be limited due to the fact that the system may need to run on a failsafe battery system at some point. Additionally, the heat generated by the devices needs to be kept as low as possible. There is no limit of power consumption, but the team will attempt to keep the consumption under 1W.

### Size and Weight

The devices of the project will be mounted somewhere in the switchyard; while the exact place of mounting is to be determined. The size and weight of the devices should be kept as low as possible for ease of installation.

### Feasibility

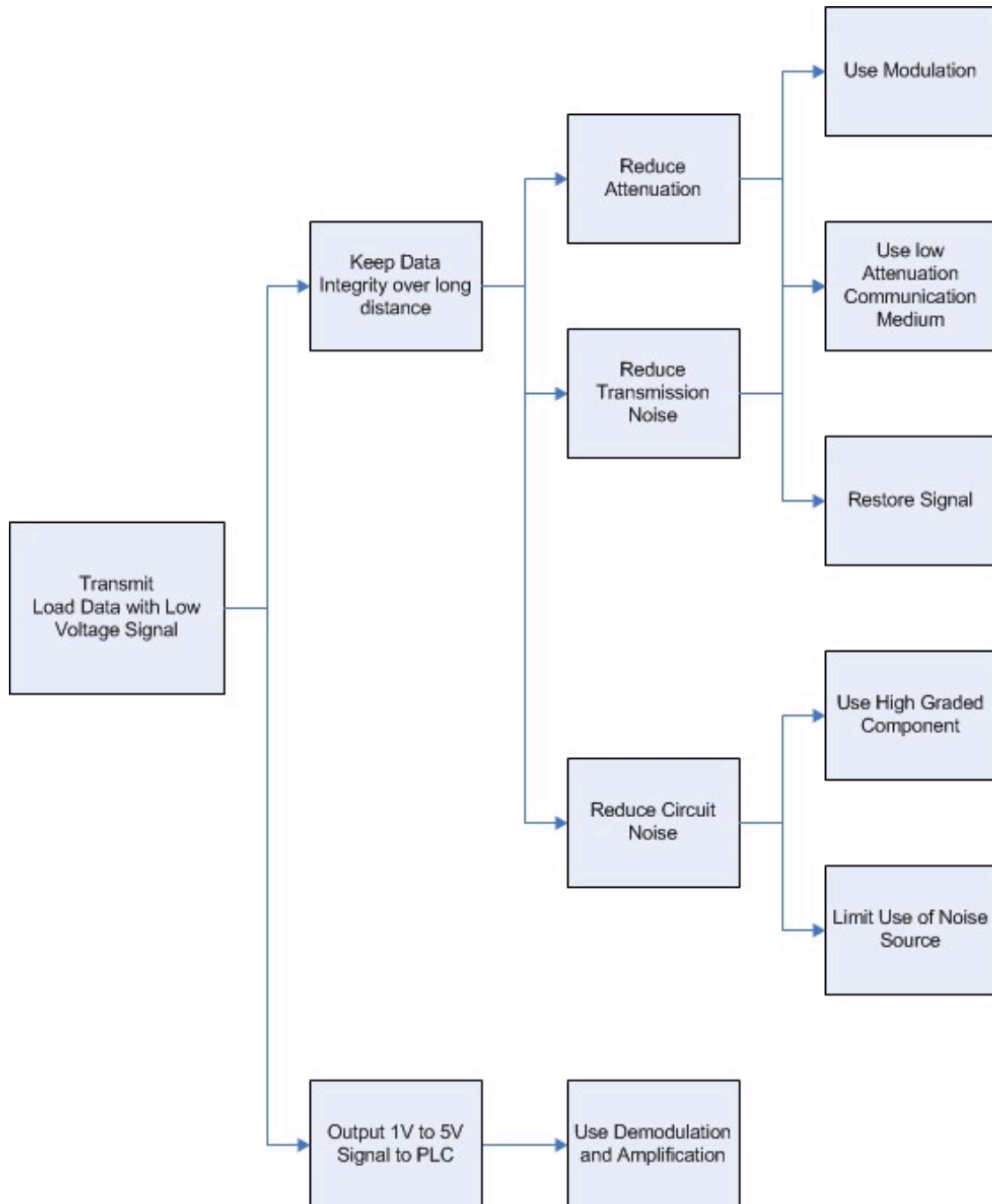
Due to the fact that the project has an absolute deadline of Design Day on December 7, 2012, the feasibility has to be considered as a significant requirement. There is no standard of feasibility, but the intended solution will have to be practicable with the resources and time that are given.

### Manufacturability

The final product should be able to be reproduced with minimal effort. The design should not include custom sections that cannot be replicated in a manufacturing process.

## FAST DIAGRAM

The Function Analysis System Technique or FAST Diagram is an efficient method of determining the necessary functions a system is required to perform. Reading the FAST Diagram from left to right indicates a “how” relationship between requirements and tasks, while reading from right to left indicates a “why” relationship between tasks and requirements. With the help of the FAST Diagram, several conceptual designs were determined for further selection. The FAST Diagram can be seen below in Figure 1.

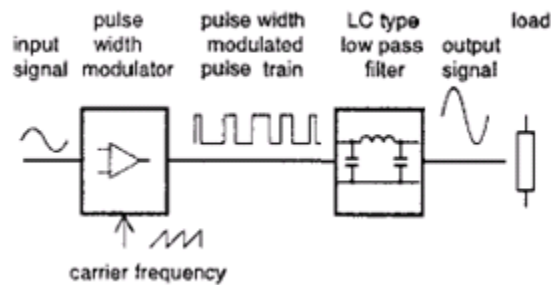


FAST DIAGRAM - FIGURE 1

## CONCEPTUAL DESIGNS

### a) Pulse Width Modulation Transmission

Pulse Width Modulation (PWM) as a means of telemetry encodes the analog signal value from a finite magnitude into a function of time. By designating the voltage level from the transducers as the modulating signal, a circuit would be used to control the duty cycle, or instantaneous pulse width, of a pulse train at any given instant in time. This duty cycle will be proportional to the original amplitude. The amplitude of the pulses are either full “on” or full “off”, analogous to a logic “1” or logic “0”, similar to a digital transmission. Attenuation from the channel, therefore, is minimized due to the fact that the information is encrypted not in the magnitude but in the pulse duration. Demodulation will be performed at the receiver to extract the original analog signal <sup>[1]</sup>.



PULSE WIDTH MODULATION DIAGRAM - FIGURE 2

### b) Frequency Hopping Spread Spectrum Transmission

Frequency Hopping Spread Spectrum (FHSS) transmission is a concept that consists of wireless transmitter and receiver units. Specific wireless transmitters and receivers manufactured by Weidmuller were found to fit in to the design specification. The transmitter and receiver pair features an output of the industry standard 4-20mA analog signal. FHSS is a technology that switches a carrier frequency rapidly among many channels within a spectrum. The sequence of the rapid changing frequency channels are only known by the transmitter and receiver. This means the data that is transmitted will be highly secured. The transmitter and receiver use 902MHz to 928MHz frequency range as its spread spectrum. The transmitter is capable of sending a signal in a range up to 15km <sup>[3]</sup>.

### c) Ethernet Remote I/O

As an alternative design solution, Ethernet Remote I/O is a remote input and output device using Ethernet as the communication medium. The use of Ethernet I/O includes two Ethernet I/O devices that are connected using TCP/IP protocol through an Ethernet network. The Ethernet I/O device is capable of taking analog signal inputs and outputting peer to peer communication.

Ethernet I/O devices are usually very reliable and robust. As a good example, the Ethernet I/O device that was manufactured by Advantech has a very wide operating temperature, which is from -10 to 50°C, and a sampling rate of 10 samples per second, which is more than enough for the design objective. The resolution is 16-bit which gives even higher resolution than needed. It comes with isolation protection, over voltage protection and even power reversal protection <sup>[4]</sup>. Used in a typical industrial environment, this device is expected to be durable and long lasting.

### d) Frequency Modulated Transmission

Frequency Modulation (FM) is a way of transmitting a signal without having to worry about attenuation corrupting the signal being sent. A signal that is sent over a great distance without any type of modulation will experience

attenuation due to the impedance of the medium and the lack of impedance matching across different mediums. FM is a process that shifts the frequency of a carrier signal to encode the amplitude of the signal being sent. The frequency of a signal is maintained throughout transmission so attenuation is not a factor if the FM signal is powerful enough to reach its destination. The signal is then demodulated on the receiving end, typically through a process called phased-lock loop <sup>[5]</sup>.

#### e) Optical Fiber Transmission

Optical fiber is a waveguide that can transmit light between two ends. Optical fiber can achieve longer distance and higher bandwidth communication than others kinds of communication. In an optical fiber, there is a higher refractive index core and a lower refractive index cladding surrounding the core. The combination of the core and cladding can achieve a waveguide of light due to total internal reflection <sup>[6]</sup>. To use optical fiber in the transmission of a load signal, the design would need to be split into three parts. The first part would be analog to digital (A/D) conversion. There would be two A/D converters on the two ends of the system. The A/D converter on the load side of the system would convert the analog load signal into a digital signal. On the central dispatch side of the system, a digital to analog (D/A) converter would convert the digital signal back into a 1 to 5V, 4 to 20mA standard analog signal. The second part of the system would be the transmitter and receiver of the light signal through the fiber. The transmitter and receiver also modulate the signal into a light signal and demodulate. The transmitter and receiver used in this system would be a gigabit interface converter device (GBIC). GBIC devices are commonly used in fiber communication. The third part of the system would involve running the fiber.

## SOLUTION SELECTION

In order to select an intended solution among the conceptual designs, a Solution Selection Matrix was used. The Solution Selection Matrix evaluates the six conceptual designs based on the eight engineering criteria and requirements of the customer. Each requirement was weighted so that it shows the actual needs of the customer. Using the Solution Selection Matrix, the conceptual design of Pulse Width Modulation stood out to be the intended solution. The Solution Selection Matrix can be seen in Figure 3 below.

**Solution Selection Matrix**

| Engineering Criteria | Importance | Possible Solutions     |              |               |                                                |                                           |                                              |
|----------------------|------------|------------------------|--------------|---------------|------------------------------------------------|-------------------------------------------|----------------------------------------------|
|                      |            | Pulse Width Modulation | Ethernet I/O | Optical Fiber | Frequency Hopping Spread Spectrum Transmission | Frequency Modulation Transmission (Wired) | Frequency Modulation Transmission (Wireless) |
| Reliability          | 5          | 9                      | 9            | 9             | 3                                              | 9                                         | 3                                            |
| Cost                 | 4          | 9                      | 3            | 1             | 3                                              | 1                                         | 1                                            |
| Feasibility          | 3          | 9                      | 9            | 3             | 3                                              | 3                                         | 3                                            |
| Size/Weight          | 2          | 9                      | 9            | 9             | 3                                              | 3                                         | 3                                            |
| Power Consumption    | 3          | 9                      | 3            | 3             | 9                                              | 1                                         | 1                                            |
| Accuracy             | 5          | 9                      | 9            | 9             | 3                                              | 3                                         | 1                                            |
| Manufacturability    | 3          | 9                      | 9            | 3             | 3                                              | 3                                         | 3                                            |
| Compatibility        | 4          | 9                      | 3            | 3             | 3                                              | 3                                         | 3                                            |
| <b>Totals</b>        |            | <b>261</b>             | <b>195</b>   | <b>151</b>    | <b>105</b>                                     | <b>103</b>                                | <b>63</b>                                    |

Importance Rating: 1 - 5 Scale, Strong = 9 points, Moderate = 3 points, Weak = 1 point

Total Calculation =  $(S1)(ImpC1) + (S1)(ImpC2) + \dots + (S1)(ImpCn)$

**FIGURE 3**

## HOUSE OF QUALITY

Based on the selected solution and customer's needs, a House of Quality method was adapted to further discover the interrelationship between customer's needs and the characteristics of the project. The House of Quality was used during the design phase of the project. A balancing of all the qualities was decided based on the information given by the House of Quality. For the House of Quality of the project, refer to the Appendix 3.

## PROJECT SCHEDULE

Each of the five members of the team was designated non-technical roles and worked on their specific section for the project. The initial project plan consisted of six weeks to completion of the chosen design, starting on September 24, 2012 with an additional five weeks until project delivery for unanticipated setbacks and preparation of the final project presentation. The initial project plan is detailed below in Table 1. For a detailed schedule and technical role of each team member, refer to the Gantt Chart in Appendix 3.

|              |                                                                             |
|--------------|-----------------------------------------------------------------------------|
| 9/24 – 10/5  | Gather data, experiment, research, prototype, and create the project design |
| 10/6 – 10/19 | Order parts for the chosen design and wait for delivery                     |
| 10/20 – 11/2 | Build the chosen design and troubleshoot, if necessary                      |
| 11/3 – 11/16 | Extra time allotted for unanticipated problems or needed rework             |
| 11/17 – 12/6 | Preparation for final project presentation and delivery                     |
| 12/7         | Project delivery                                                            |

TABLE 1

## PROJECT BUDGET

The proposed design of PWM has a big advantage over the other proposed designs because of the low cost. The parts, including all the electronic components and chips, can be found in the ECE shop with no cost. Parts may be ordered once the design is finalized. Low noise and low power consumption ICs will increase the signal integrity and overall power consumption of the design. The entire circuit needs to be fabricated on a printed circuit board. There are several options for fabrication. The ECE shop is capable of doing a simple Printed Circuit Board (PCB) fabrication. Since the design circuit is not complicated this may be a possibility. If the designed circuit board needed to be fabricated by a PCB fabrication company, it was estimated that the cost of fabrication will be one hundred dollars.

Cases and mounting devices which are needed for mounting and installing the devices in the plant would be required. It was estimated that the cost of the cases would be around thirty dollars and the cost of mounting devices would be fifty dollars. All the cost at this moment was estimated. However, with no more elements to be purchased, it was predicated that the cost of the entire project would be controlled at about two-hundred dollars. The breakdown of the total predicted cost is show in Table 2 below.

|                       |        |
|-----------------------|--------|
| Electronic components | \$10*  |
| ICs                   | \$10*  |
| PCB Fabrication       | \$100* |
| Enclosure             | \$30*  |
| Mounting device       | \$50*  |
| Total                 | \$200* |

\*ESTIMATED COST

TABLE 2

## CHAPTER 3

### PRINCIPLE OF PULSE WIDTH MODULATION

Pulse Width Modulation (PWM) is a method of encoding the voltage amplitude of a signal within the width of a pulse. Information contained within a pulse width instead of voltage amplitude has the advantage of being less susceptible to both attenuation due to resistance and noise within a transmission line. The goal of the design project is to transmit the power usage information presented in the amplitude of the transducer voltage between two separated locations with the greatest accuracy possible. PWM was chosen as the transmission method due to its ability to maintain a high degree of integrity of transmitted data regardless of potential signal noise over transmission line lengths ranging up to and exceeding the design length of one half mile.

It should be noted that the level of noise which might be present in the transmission line due to electromagnetic interference and other noise sources is unknown and not able to be estimated. There may be a great amount of noise or no noise at all present in the transmission line, PWM was chosen as the transmission method due to the possibility of noise. The PWM signal transmission method along with the shielding on the transmission line should eliminate or at least greatly diminish any external noise should it be present.

### PULSE WIDTH MODULATION DATA INTEGRITY EXAMPLE – PSPICE SIMULATION

The ability of PWM to maintain the integrity of data against externally caused noise can be demonstrated using a PSPICE simulation of a model transmission line.

For the transmission line one half mile of Belden 8761 shielded twisted pair cable or a cable with very similar specifications will be used by the project sponsor. To model how the transmission line will react to a PWM signal a simulated PWM signal can be transmitted as a fifty percent duty cycle one kilohertz pulse with a twelve volt peak and zero volt low level. The Belden cable has specifications listed in Table 3. Figure 4 is a circuit which models a pulse generator as  $V_p$ , a signal noise as  $V_{noise}$ , a terminating resistance of one  $M\Omega$  simulating the input of an op amp, and the transmission line as a lumped element model with a series of three resistor-inductor-capacitor networks. The noise on the line represented by  $V_{noise}$  is an extreme case in which the noise is a sine wave with 1Vp-p and a frequency of 100kHz.

|                                         |      |                                 |
|-----------------------------------------|------|---------------------------------|
| Inductance                              | 0.20 | $\mu\text{H}/\text{ft}$         |
| Capacitance<br>(conductor to conductor) | 24   | $\text{pF}/\text{ft}$           |
| Resistance                              | 16   | $\text{Ohms}/1000 \text{ feet}$ |

TABLE 3

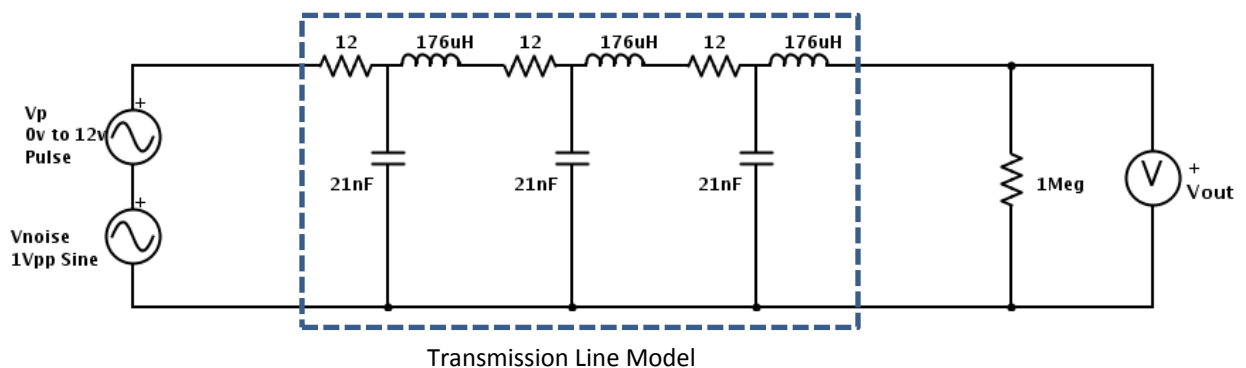


FIGURE 4

Figure 5 is a PSpice simulation of the circuit in Figure 4 showing the transient result of  $V_{out}$  for two periods of the PWM signal. The high time of the pulse measured in PSpice can be calculated by measuring the one volt point on both the leading and trailing edge of the pulse. The pulse high time is  $31.504\text{ms} - 31.002\text{ms} = 502\mu\text{s}$ . The actual high time of the pulse is  $500\mu\text{s}$  evident by the fact that  $V_p$  is fifty percent duty cycle with a frequency of one kilohertz. Thus in the example the PWM signal maintains the integrity of the transmitted data to less than one percent error even in an extreme case of noise in the transmission line.

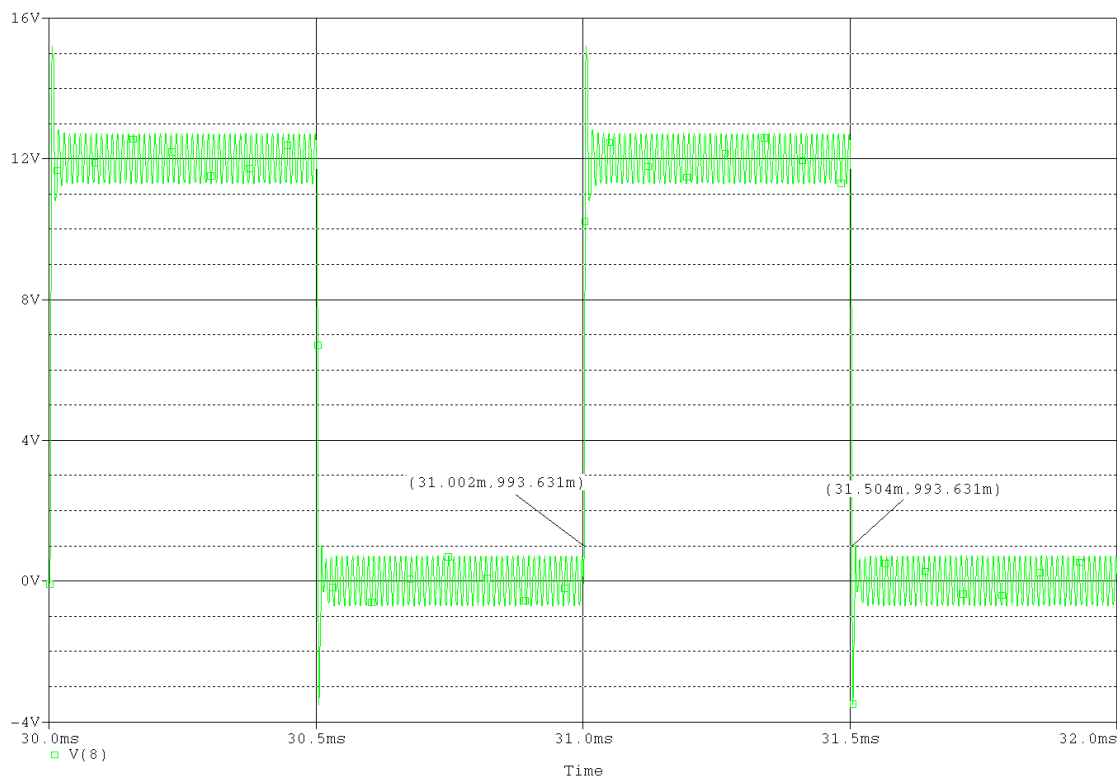


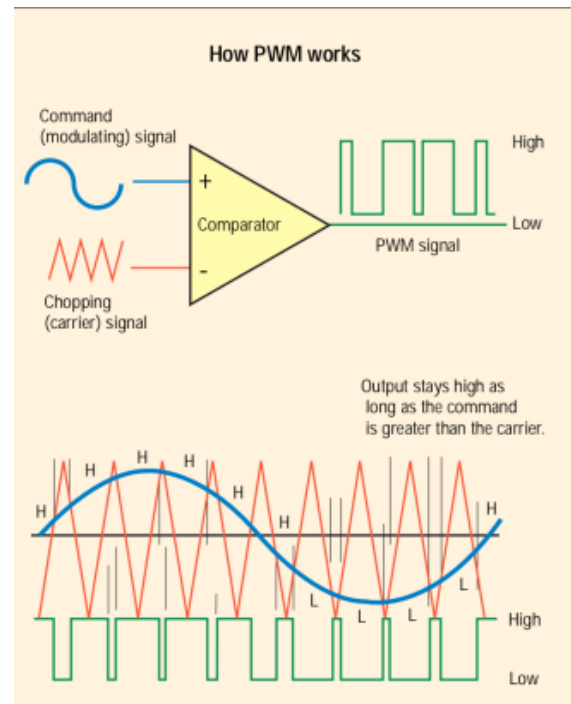
**FIGURE 5**

## CREATING A PULSE WIDTH MODULATION SIGNAL

A PWM signal is created by comparing a voltage input modulating signal with a repeating linear ramp or triangular waveform carrier signal. In the project modulating circuit a ramp waveform carrier signal was used due to the greater simplicity of creating a precise ramp waveform.

Figure 6 is from an MIT online instructional document which has a good explanation of PWM using a triangular carrier signal. As seen in Figure 6 the modulating signal is applied to the non-inverting input of the comparator and the triangular wave carrier signal is applied to the inverting input of the comparator. Whenever the input modulating signal is greater in amplitude than the carrier triangular wave the pulse width modulated output of the comparator stays high. When the input modulating signal is less than the carrier signal the pulse width modulated output goes low. Thus the information on the voltage amplitude of the input signal is encoded as the pulse width of the PWM output.

In the final product the input modulating signal from the load transducer is converted to a pulse width modulated signal in the same way as shown in Figure 6 except a ramp waveform is used as the carrier signal. The comparator configuration used in the project modulating circuit is configured as shown in Figure 7. Note that a pull-up resistor is required for the LM339 comparator for proper operation which is not shown in the MIT document from Figure 6.



MSD 101, Pulse-Width Modulation <sup>[7]</sup>

FIGURE 6

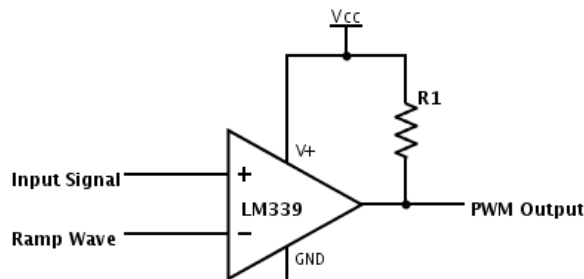


FIGURE 7

## CIRCUIT DESIGN

The project requirements specify that the amplitude signal from the load transducer must be transmitted one half mile and converted to a signal capable of being read by a PLC. Since a PWM method of signal transmission is being used there are two major circuit components required to transmit a signal, the modulator and the demodulator.

The modulator will convert the 0-100mV input signal from the load transducer into a PWM signal on the transmitting side of the transmission line while the demodulator will convert the PWM signal to a signal ranging between two to four volts DC on the receiving end of the transmission line. The two major circuit components will be further discussed individually.

## MODULATOR

The entire modulator circuit can be seen in Figure 8. The purpose of the modulator is to convert the 0-100mV input signal from the load transducer into a PWM signal to be sent over the transmission line. The modulator consists of six blocks each of which performs individual functions within the circuit. The six blocks are the: LM555 short duration pulse generator, linear ramp generator, input gain, input offset, comparator, output buffer. Each of the six major blocks of the modulator circuit will be described in detail in following sections.

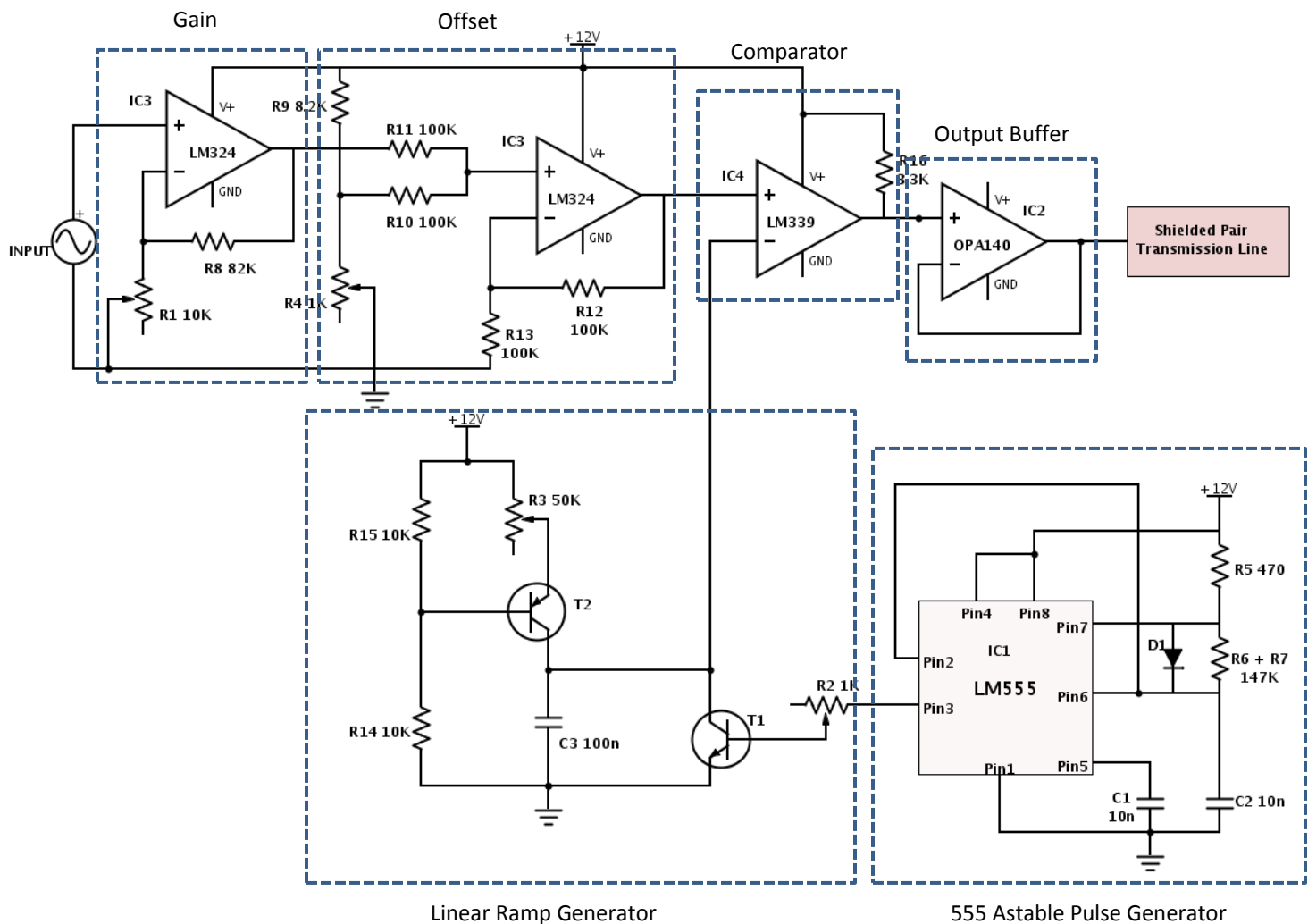
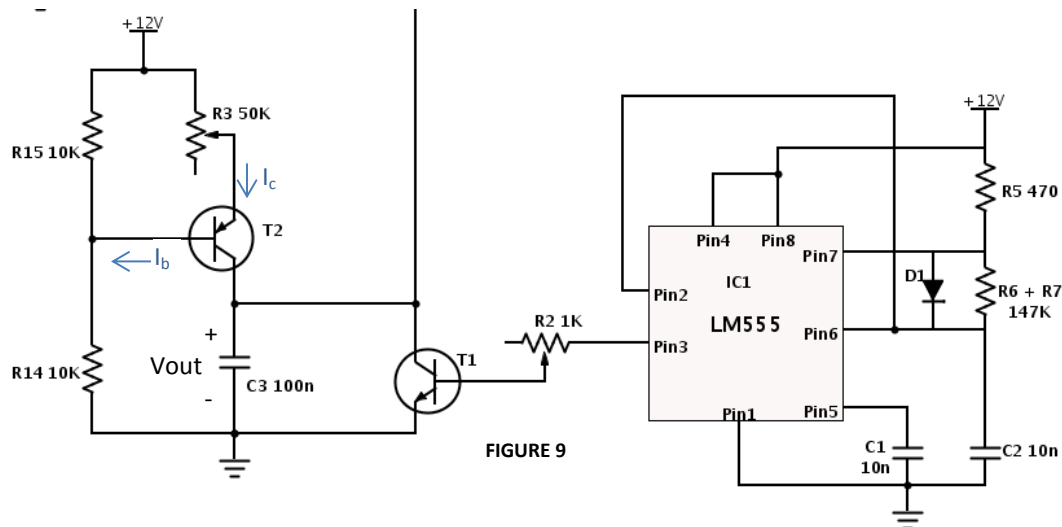


FIGURE 8

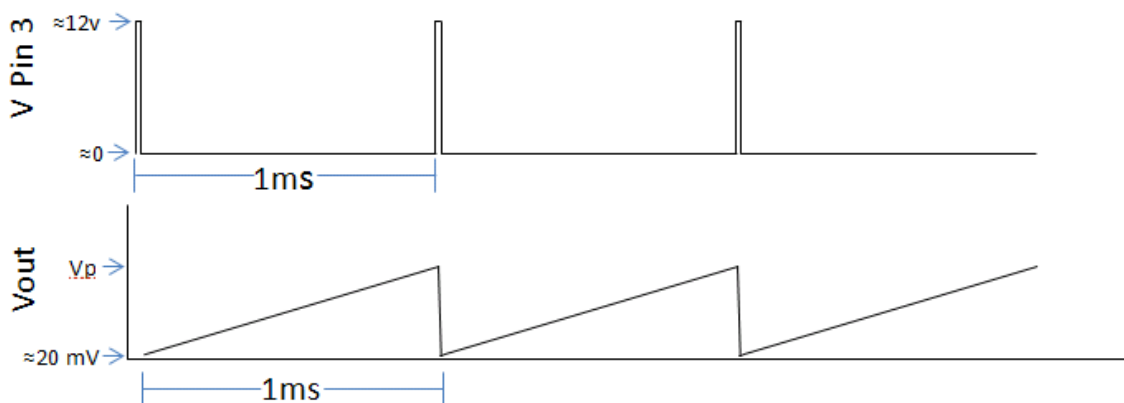
## LINEAR RAMP GENERATOR AND LM555 PULSE GENERATOR

The linear ramp generator creates the carrier signal ramp waveform used for comparison with the input to create the PWM signal. The linear Ramp waveform generator is seen in Figure 9. The ramp generator was created by modifying a ramp generator application listed in the Texas Instruments LM555 Datasheet. In the TI LM555 Datasheet the ramp generator application creates a ramp waveforms which varies between  $V_{cc}/3$  and  $(2/3)V_{cc}$ , where  $V_{cc}$  is the LM555 supply voltage. The variation between  $V_{cc}/3$  and  $(2/3)V_{cc}$  is due to the LM555 internal JK flip flop which is referenced to those voltages through an internal resistor voltage divider. However the team needed to create a carrier ramp waveform which varied from zero volts to an adjustable peak voltage. To create



the ramp generator which met the team's specifications the circuit in Figure 9 was created which uses the same transistor circuitry as the LM555 Datasheet application, as seen on the left of the figure, but as the triggering device an adjustable astable LM555 was used as seen on the right.

The generator is made by combining an LM555 astable pulse generator with less than one percent duty cycle along with a transistor configured as a constant current source flowing into a capacitor as seen on the left hand side of Figure 9. Components R5, R6+R7, and C2 were chosen to produce a pulse train at the output pin three of the LM555 with a 1Khz period and a duty cycle less than one percent shown theoretically in Figure 10.



Transistor T2 is configured as a constant current source. T2 has a constant fixed base current,  $I_b$ , between the emitter to base junction through R3 and to the voltage divider formed between R15 and R14. If T2 is operating in active mode with a constant base current the collector current through T2 must also be constant and will equal to  $\beta I_b$ , with  $\beta$  being the DC gain of the transistor. In other words, because the transistor has a fixed bias current it must also have a fixed collector current in the active mode.

The current flowing through the collector of T2 can then go in two directions depending on the state of the LM555 output at pin three. If the LM555 output is low transistor T1 is in cutoff and appears like an open circuit between the collector to emitter. With T1 cutoff the collector current of T2 can only flow into the capacitor C3 and begin charging the capacitor and increasing  $V_{out}$ . When a constant current is charging a capacitor there must be a constant  $+dV/dt$  across the capacitor equal to the current divided by the capacitance, thus there is a linear ramp voltage present across the capacitor C3. The amount of current flowing through the collector of T2 and thus the maximum ramp voltage  $V_p$  can be adjusted by varying potentiometer R3. Lowering the resistance of R3 allows more current to flow from the collector of T2 during the duration between pulses from the LM555 and increases  $V_p$ . Alternatively, raising the resistance of R3 lowers the collector current of Q2 and reduces  $V_p$ .

During the brief time in which the output of the LM555 at pin three is high the transistor T1 becomes saturated. When T1 becomes saturated it appears almost like a short circuit between the collector to emitter. C3 then discharges toward zero volts very quickly through the saturated T1. However the capacitor voltage  $V_{out}$  cannot discharge all the way to zero volts because of the small transistor saturation voltage present between the collector and emitter of T1. Once the output of the LM555 at pin three returns to a low state T1 again goes into cutoff and the charging process of C3 starts again until the output of the LM555 returns high.

The Resistor R2 is needed to prevent the base current of T1 from exceeding its maximum allowed value when the output of the LM555 is high.  $V_{cc}$  should be at least twice the desired  $V_p$  of the ramp waveform to ensure linearity of the ramp over the entire range of ramp voltage.

In the lab it has been observed that the minimum voltage of the ramp wave,  $V_{out}$ , is approximately 20mV when using Q2N3904 and Q2N3906 transistors for T1 and T2 respectively over a range of  $V_{cc}$  and  $V_p$  voltages and LM555 pulse duty cycles.

Figure 11 displays an oscilloscope plot taken from the ramp generator in Figure 11 used in the modulator. The voltage  $V_{out}$  across capacitor C3 is on channel one and the voltage at pin three of the LM555 is on channel two. Resistor R3 was adjusted to obtain a ramp waveform with a 2.00 volt peak. The output of the LM555 at pin three is a 1Khz pulse with less than one half percent duty cycle. The pulse time can just barely be seen at the moment the ramp waveform transitions from 2.00 volts to about zero volts.

Note- A PSPICE simulation of the linear ramp generator from Figure 11 can be found in Appendix 3



FIGURE 11

## INPUT GAIN AND OFFSET

Before the input is used for conversion to a PWM signal a gain of ten and an offset of 500mV is applied to the input. The goal of the Input gain and input offset sections of the modulating circuit is to change the 0 to 100mV input signal into a more easily usable signal ranging from 500mV to 1.5V to be compared with a zero to 2.00V peak linear ramp. A gain of ten is applied to the input through an op amp non-inverting amplifier then an adjustable offset of +500mV is applied to the signal via an op amp non-inverting summer. Figure 12 shows the input gain and input offset sections of the modulator circuit. The boxed section on the left of the figure is the non-inverting amplifier and the boxed section on the right is the non-inverting summer.

The gain of the non-inverting amplifier is fine-tuned through potentiometer R1 and the offset voltage is fine-tuned through potentiometer R4. Detailed reasons for adding a gain and offset to the input signal are discussed in the following section. A detailed explanation of how the non-inverting summer functions can be found in Appendix 3.

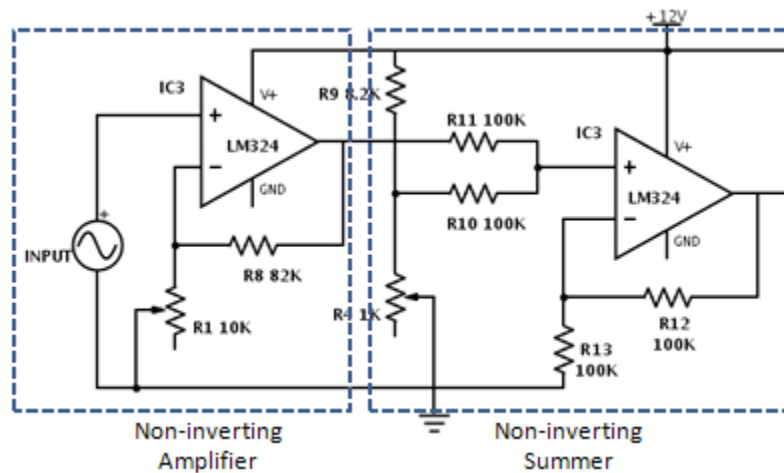


FIGURE 12

## REASONS FOR ADDING GAIN AND OFFSET TO THE INPUT SIGNAL

The input signal from the load transducer is a very small voltage ranging between 0-100mV, which means that a 100mV variation represents the full range of the measured load. To convert the voltage amplitude of the input signal to PWM the input must be compared with a linear ramp voltage with the same or larger peak-to-peak voltage range as the input. A problem is presented when the modulator circuit components create small errors or add a small fixed amplitude noise to the input signal as it progresses through the different parts of the modulator circuit. The peak-to-peak voltage range of the input is so small that an error of even 1mV presented in the circuit due to a fixed amplitude noise or the input offset voltage of the comparator will be a large proportion of the signal, a one percent error for a 100mV signal. If a gain of ten is applied to the input signal the peak-to-peak voltage range of the input will increase to one volt and a 1mV error will be a smaller proportion of the signal, thus the percent error will be reduced to 0.1% for a one volt signal.

In the initial tests the range of both the input modulating signal and carrier signal were approximately zero to one volt. In other words, a ten times gain was applied to the input transducer signal and then compared directly with a one volt peak ramp waveform carrier signal to produce a PWM output. Unfortunately there was error found in the

conversion to PWM in the lower five percent and the upper fifteen percent of the 0-100mV transducer input range.

For any 10mV change in the transducer input signal over the 0-100mV range there should be an equal change in the duty cycle of the pulse width modulated output into the transmission line. At the lower five percent and upper fifteen percent of the transducer input range the change in the output PWM duty cycle was not linear as expected based on changes seen in the middle part of the 0-100mV input range. The reasons for the lower and upper range error in the PWM signal are unknown but there are two theories to account for some the error seen.

The minimum voltage of a ramp waveform from the linear ramp generator is approximately 20mV instead of 0V, as discussed in the linear ramp PSPICE simulation in Appendix 3. If the linear ramp generator is adjusted to a one volt peak ramp wave and compared with a zero to one volt modulating signal the information presented in the bottom 20mV of the input modulating signal will be lost in the conversion to PWM because the carrier ramp waveform does not extend below about 20mV. The amount of the input signal information lost at the bottom end of the input range will not be equal to five percent of the bottom range but there will be some small amount lost.

The error on the upper fifteen percent range of the input signal could be due to small voltage spikes on the ramp waveform or input voltage however this would not fully account for the error seen. Ultimately the exact cause of the nonlinearity in the PWM output seen on the lower and upper ends of the input signal range is unknown. However, a way of solving the nonlinearity problem was discovered by increasing the range of the carrier ramp signal such that it extends both above and below the maximum value of the transducer input signal after the ten times gain.

The ramp generator was adjusted to a two volt peak ramp waveform and an offset of 500mV was added the input signal after the ten times gain. Thus the transducer input of 0-100mV would vary from 500mV to 1.5 volts at the non-inverting comparator input and the ramp would vary from approximately zero volts to two volts at the inverting comparator input. By utilizing only the middle half of the range of the ramp carrier signal the nonlinearity error seen in the PWM output at the bottom and top ends of the input range was eliminated.

On the following page Figures 13, 14, 15 are oscilloscope plots of the transducer input after gain and offset in on channel one, the ramp waveform on channel two, and the PWM output to the transmission line on channel three. The plot in Figure 13 was taken with a 0mV input from the transducer, thus the modulating signal after gain and offset is  $0\text{mV} \times 10 + 500\text{mV} = 500\text{mV}$  as seen on channel one. The carrier ramp waveform has a range of zero to two volts displayed on channel two. The PWM output has a measured duty cycle of about 25% as displayed in the measurement section at the bottom of the plot.

Figures 14 and 15 have the identical setup as Figure 13 except a Figure 14 was taken with a 50mV transducer input and Figure 15 was taken with a 100mV transducer input. Notice the duty cycle of the PWM output pulse as displayed in the measurement section of the plots. The duty cycle of the PWM output pulse is 25% at the minimum transducer input of 0mV and the duty cycle is 75% at the maximum transducer input of 100mV.

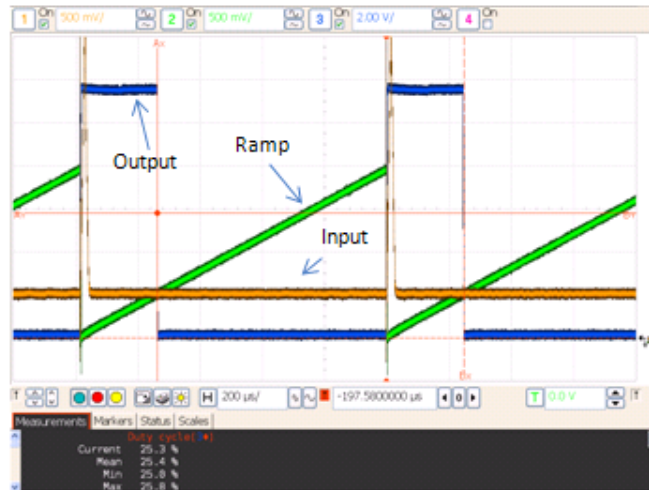


FIGURE 13

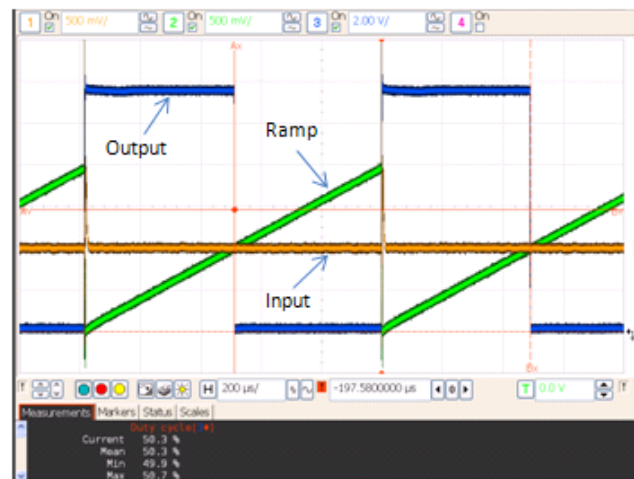


FIGURE 14

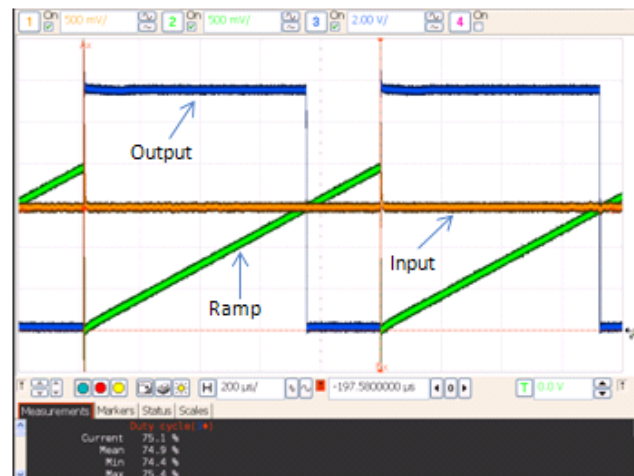


FIGURE 15

## COMPARATOR AND OUTPUT BUFFER

The comparator and output buffer sections of the modulator are shown in Figure 16. The comparator converts the input signal into PWM by comparing the input after gain and offset with a linear ramp waveform. Figure 17 shows an oscilloscope plot of the input signal after gain and offset on channel one, the ramp waveform from the ramp generator on channel two, and the output from the comparator to the buffer on channel three. The transducer input used to produce the oscilloscope plot in Figure 17 is 50mV. Note that the signal on the non-inverting input of the comparator, seen on channel one is a constant one volt. This is due to the ten times gain and 500mV offset applied to the transducer input. Thus  $50\text{mV} \times 10 + 500\text{mV} = 1\text{V}$ .

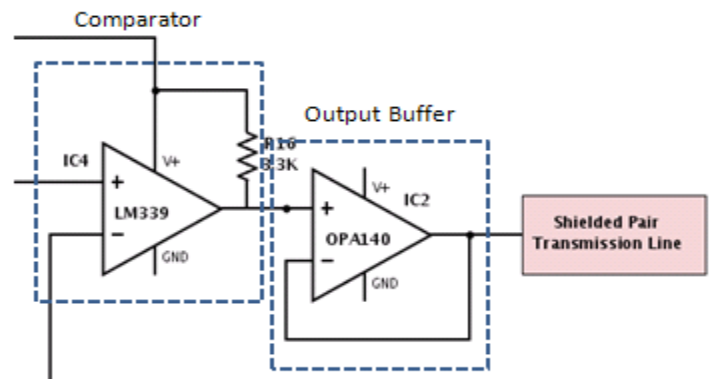


FIGURE 16

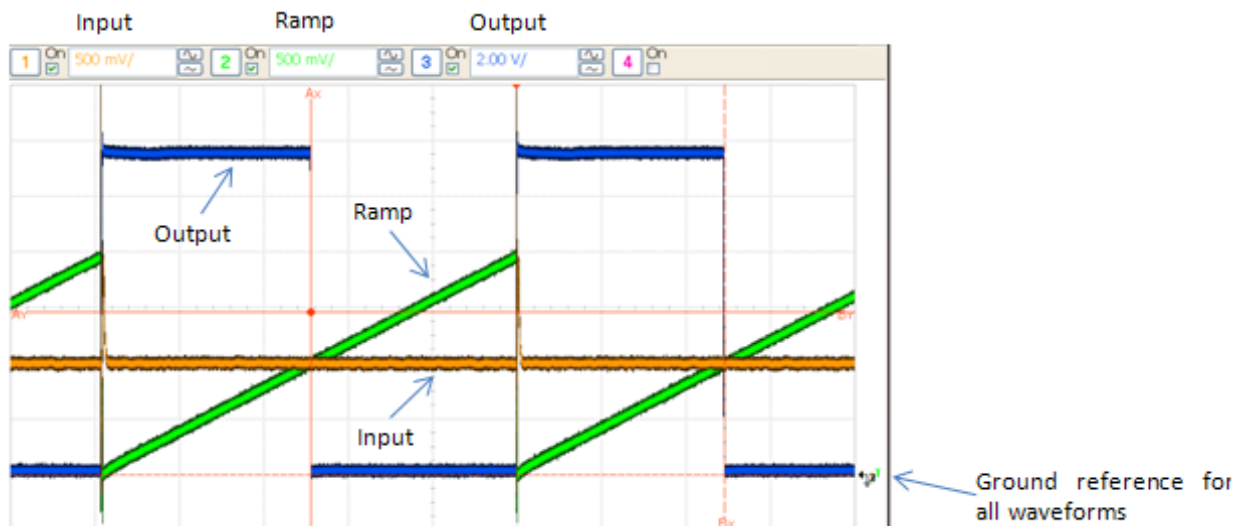


FIGURE 17

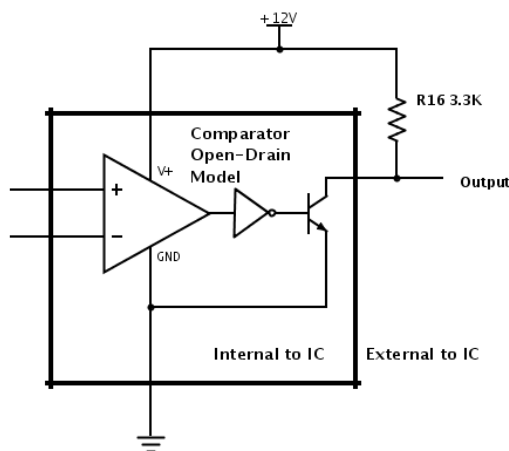


FIGURE 18

The output buffer was added after the comparator to minimize loading effects on the comparator from the transmission line. The comparator is an LM339 which has an open-drain output. Due to the open-drain output configuration the pull-up resistor R16 is required between the voltage supply and output of the comparator. Figure 18 shows a model of an open-drain comparator. When the comparator is output high an internal output transistor is in cutoff and the comparator output is brought up to the level of the supply voltage through the external pull-up resistor. When the output of the comparator is low the internal transistor is saturated and the comparator output is attached to ground through the

saturated transistor. When the output is low current flows through the pull-up resistor from the voltage source, but all current through the pull-up resistor flows to ground through the essentially short circuited output transistor.

During initial designs of the modulating circuit the output buffer was not in place and the transmission line was connected directly to the output of the comparator. Due to the absence of the output buffer a problem developed from the capacitive loading effects of the transmission line on the comparator.

When the comparator is output high the internal transistor is cutoff and ideally the output voltage of the comparator should be immediately pulled-up to the supply voltage of twelve volts through the pull-up resistor. Almost no current should flow through the transmission line due to the greater than  $1\text{M}\Omega$  termination resistance at the demodulator input. However since the transmission line has a small capacitance between conductors current will flow into the transmission line through the pull-up resistor R16 until the capacitance between conductors is charged to twelve volts. A problem is encountered because when current flows through the pull-up resistor there is a voltage drop developed across the resistor and the pulse voltage sent across the transmission line does not immediately jump to twelve volts. Instead the pulse will look like a characteristic RC charge curve.

A PSPICE simulation was ran to investigate the capacitive charging problem in the transmission line. The circuit in Figure 20 is repeated from the 'Pulse Width Modulation Data Integrity Example' section however to simulate the action of the pull-up resistor when the comparator output is high R16 was added and to simulate the saturated internal comparator transistor when the output is low a diode was added. The resulting transient output plot of the voltage Vout as seen on the demodulator end of the simulated half mile transmission line is shown in Figure 19. The charging effect of the transmission line capacitance can be clearly seen as the output waveform looks more like a characteristic RC charge curve rather than a pulse. If the transmitted signal is not a pulse waveform the demodulator will not be able to accurately demodulate the transmitted PWM signal for use by a PLC.

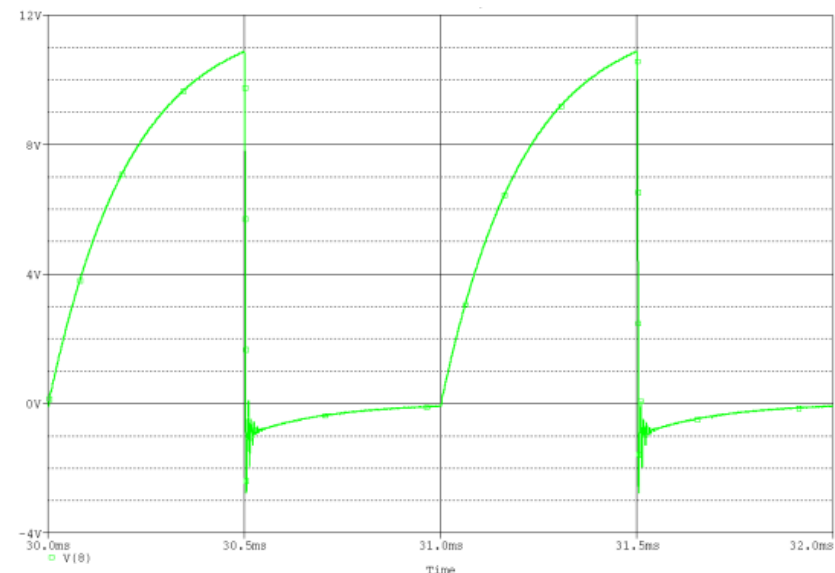


FIGURE 19

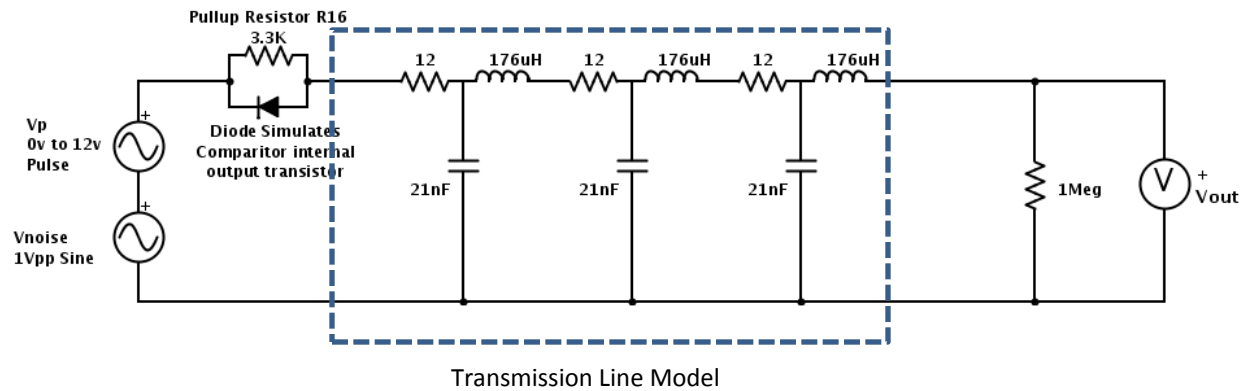


FIGURE 20

The current drawn through the pull-up resistor during the high output swing of the comparator can be nearly eliminated by adding an op amp configured as a voltage follower between the output of the comparator and the transmission line. The comparator will see a high resistance with very little capacitance from the non-inverting input of the voltage follower and the transmission line will see a low source impedance from the output of the voltage follower. Thus the capacitive loading effects from the transmission line on the PWM signal will be eliminated.

## CHOICE OF OPERATIONAL AMPLIFIERS AND COMPARATORS

Two different kinds of operational amplifiers are used in the project circuit, the LM324 and OPA140. Both of these op amps were chosen due to their negative rail output capability, single supply voltage capability, and wide operating temperature range. The main difference between the two op amps is the slew rate. The LM324 has a slew rate of about 0.5 volts per microsecond and the OPA140 has a much higher slew rate of about 20 volts per microsecond.

In applications in which a low slew rate op amp can be used such as in the input gain and offset along with the demodulator low pass filter the LM324 is used due to its low cost and simplicity. In applications which require a high slew rate such as the demodulator output buffer the OPA140 is used due to its high slew rate. However the OPA140 is much more expensive than the LM324 and is only available in the surface mount package, which requires special and more expensive parts to convert to a through-hole mounting configuration that can be used on a PCB. In general there is a very small selection of single supply, high slew rate, op amps available on the market and the OPA140 is the best fit for the project requirements.

An LM339 comparator is used both in the modulating and demodulating circuits. A comparator is very similar to an op amp except that a comparator has a much higher slew rate than an op amp due to the lack of internal stability compensation and a comparator also requires a pull-up resistor if it is an open-drain output type. The advantage of using a comparator instead of an op amp is that a comparator has a much higher slew rate and can respond faster to a step voltage increase as seen in a pulse signal. Figure 21 demonstrates the effect an op amp voltage follower has on an input pulse waveform. The pulse waveform becomes distorted because the output voltage of the op amp has a maximal rate of change equal to the slew rate. Any type of op amp will always present slew rate distortion but different op amps can be selected such that the specified slew rate is high enough such that the pulse distortion is within an acceptable minimal amount. Figure 22 displays an oscilloscope plot of the pulse signal from the output of the comparator in the completed modulator circuit on channel one and the output of the OPA140 buffer on channel two. The ground references are not aligned so that each waveform can be more easily seen. Notice that there is no noticeable distortion of the pulse waveform between the LM339 comparator and the OPA140 op amp. The OPA140 was chosen due to its high slew rate and does not present a problem with pulse distortion.

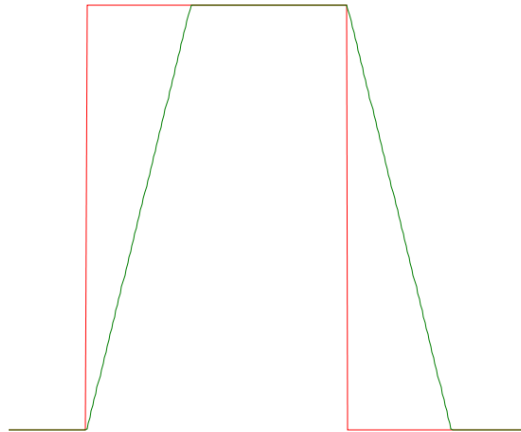


FIGURE 21

There was discussion in the team as to the relevance of using comparators with the modulating and demodulation circuit due to the addition of an OPA140 op amp buffer on the outputs of both comparators. In theory the advantage of the higher slew rate of a comparator cannot be utilized if an op amp is used on the comparator output as a buffer. Since the slew rate of the op amp is much lower than the slew rate of the comparator, the op amp will be the limiting factor on output switching speed, thus the comparator could potentially be replaced by an OPA140 op amp in both the modulator and demodulator. Both of the comparators would then be essentially unneeded and provide no advantage because of the OPA140 buffers used on the comparator outputs. On the other end, saturation issues can occur

with op-amps that result in low recovery times in order to switch the state of the output. Comparators are designed to operate with minimal instability. Unfortunately this issue was not fully examined until after the modulating and demodulating circuits had been built and tested on the PCBs and thus the design was not changed.



FIGURE 22

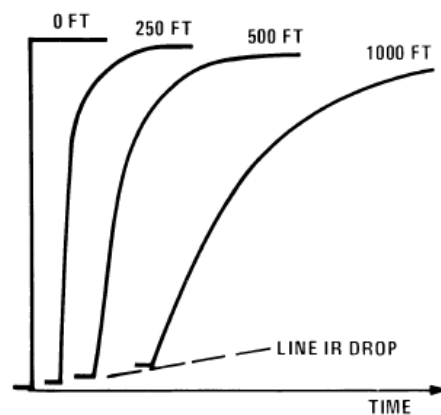
## DEMODULATOR

### CONSIDERING INTERFERENCE

For telecommunication purposes, the utility of pulse width modulation (PWM) lies within the duty cycle of the encoded signal. Like frequency modulation as mentioned earlier, PWM has inherent noise-immunity that permits an analog signal to be sent on a relatively lengthy wire-line communication channel with minimal interference. The amplitude assumes one of two relatively discrete values similar to digital communication; thereby the noise has to be significant enough to change the switching of the states. However, as the length of the transmission channel increases, the probability of outside interference affecting the signal integrity also increases. Noise and distortion can compromise the function of PWM by skewing the duty cycle and altering the wave shape of the pulse.

### Distortion

Distortion for a PWM waveform is a direct function of the transmission channel. For a given step function, the rise time or fall time of the pulse edge will increase as the cable length increases due to attenuation ( $I^2R$  losses).



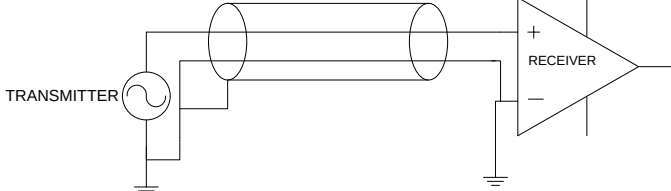
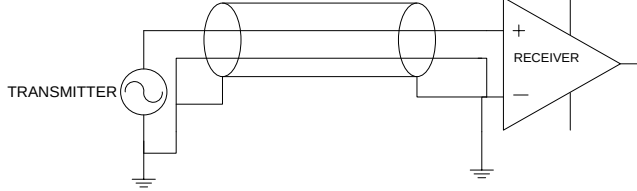
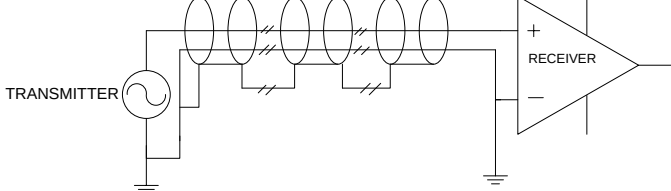
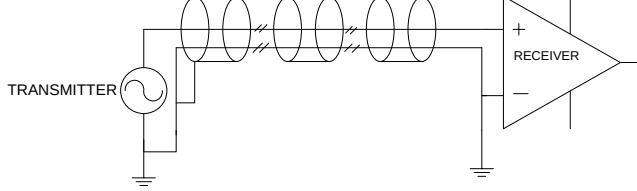
Example of Distortion of a Pulse Edge with Increased Cable Length <sup>[8]</sup>

FIGURE 23

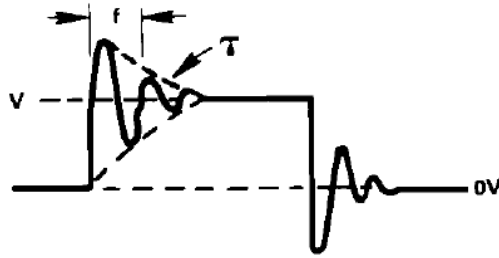
Also mentioned prior, the transmission line can be modeled using distributed parameters such as capacitance and inductance that give the channel a bandwidth, analogous to a filter. A pulse is composed of several harmonics of sine functions; the high frequency components of the pulse will have the highest susceptibility to attenuation and delay. If the frequency of the transmission exceeds the bandwidth of the channel, significant distortion will occur. Therefore, consideration was given in our approach to understand the bandwidth of the channel relative to the maximum switching speed of the PWM output from the transmitter in order to reduce distortion. Use of the Nyquist rate is a model for digital transmission, though it can be a tool for use with PWM even though it is analog. For example, Level 1 Twisted Pair cable used for telephony has a bandwidth of 0.4MHz. In order not to have significant distortion, using the Nyquist principle, the maximum frequency of transmission must not exceed half of 0.4MHz or 200kHz. The maximum switching frequency from the transmitter for the design was approximately 1kHz, well-below the required Nyquist frequency.

## Noise

There are many different mechanisms for generating noise within the transmission line. The basic principle involves a noise source that interacts with the line via a coupling method. Knowing all the coupling methods, it is virtually impossible to have a noise-free transmission. Environmental interference such as inductive, capacitive and radiative coupling were outside of the team's modeling capability. Perhaps the simplest, though the most effective, method of noise protection from coupling interference is the use of shielding. As indicated by the sponsor, shielded twisted-pair cable was available. The twisting helps to eliminate the influence of crosstalk within the channel, as well as minimize the impact of EMI. The principle works by having opposing currents twisted together, the net magnetic field created between the two conductors are cancelled out. The shield further limits the amount of interference that occurs on a lengthy channel. The shield provides a surface area for noise sources to deposit their charge, and if properly grounded, the drain wire will provide a path for the charge carriers to travel to ground. Proper field wiring therefore is essential in minimizing the impact of noise introduced by our transmitter.

| Do                                                                                                                                                                                                             | Don't                                                                                                                                                                                                              |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  <p>Only tie one end of the shield (transmitter-side recommended) to ground.</p>                                              |  <p>Tying the both ends of the shield to their respective grounds has the potential to introduce ground loops.</p>               |
|  <p>For any breaks in the wire or junctions, the shields of each section must be tied together back to a common ground.</p> |  <p>Any portion of the conductor shielding not tied to ground has the ability to accumulate charge and cause interference.</p> |

Beyond noise due to coupling, several other noise contributions could be considered. One of the greatest contributions the team could make in noise-preclusion was to reduce the noise sent from the transmitter. Especially concerning was the potential existence of common-mode noise that often gets exhibited in ringing of the pulse-width modulated output. The natural frequency will be of the standard relationship,  $f=1/2\pi\sqrt{LC}$ , with a dampening time constant,  $\tau=L/R$ .



Pulse with Ringing <sup>[8]</sup>

FIGURE 24

The team had very little knowledge of the transmission line route or its varying degree of susceptibility to interference along its path. A base set of assumptions was chosen to be provided by the sponsor to let the team proceed with development of receiving the input from the transmitter.

#### Transmission Line Assumptions

1. Cabling and wiring is done at the site consistent with industry standards, such that there is separation of high voltage power cables from instrument and control cables (i.e. dedicated cable trays).
2. Shielded twisted-pair wire will be used as the chosen transmission medium due to its lower cost and higher tolerance to interference in field wiring applications pertaining to instrument/control applications.
3. Proper field wiring will be implemented to minimize the risk of common mode noise, noise due to ground loops, etc.

#### THE RECEIVER

The final design of the receiver or demodulator is implemented in three stages of circuits. The repeater stage is used to restore the PWM signal from attenuation and loss of signal integrity due to distortion. The clipper circuit is a combination of circuits that is used to lift the bottom of the PWM signal and clip the top as well, such that when it is averaged, it is confined into a specific range. The Bessel lowpass filter then averages out the PWM as a demodulator and then is output to the PLC in the dispatch control room for analysis and measurement.

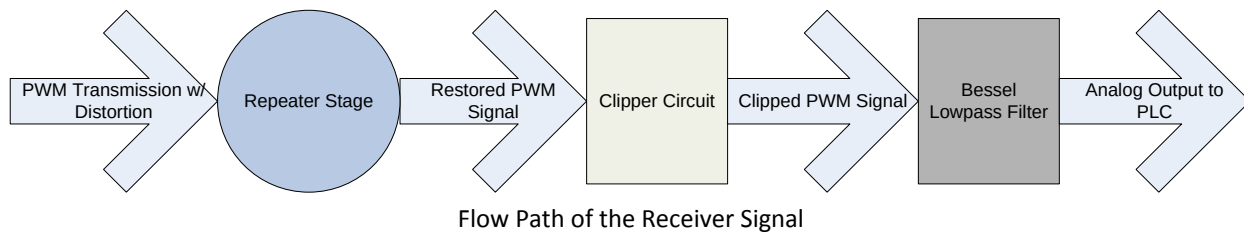
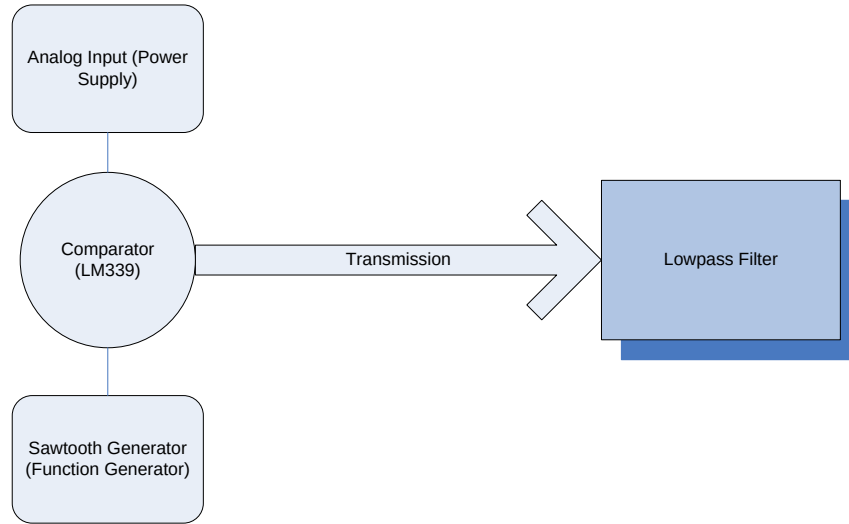


FIGURE 25

[illegible]

## Early Design

35



Early Development of PWM Transmission

FIGURE 27

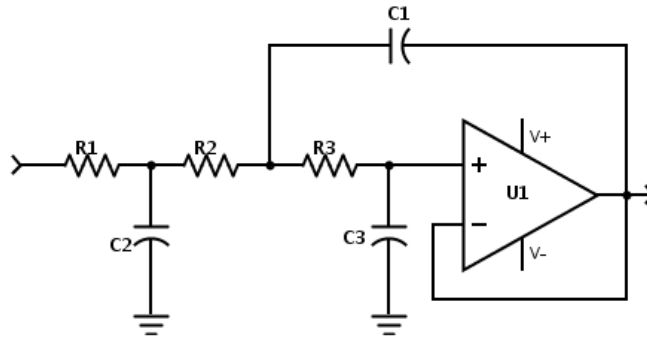
The first decision had to be whether we wanted to use a passive or active design. In order to determine this, a careful assessment of the corner frequency had to be made. Ideally, the transducer input could be thought of as a DC signal without any periodicity. In reality, load fluctuations at the mill happen quite often. What relevant information that ArcelorMittal would want to know had to be determined. Based upon the discussion during the site visit, there wasn't a very clear answer. The default update for the PLC was to capture load information every five seconds, or a sampling frequency of 0.2Hz. Updates could be increased in frequency based upon how close they might be operating to a critical margin, such as at maximum load where load transients might cause automatic protective functions to occur. A conservative choice was made to capture load changes at a maximum frequency of a 10Hz or once every 100ms. That value is then assumed to be our corner frequency for the filter. For such a relatively low corner frequency, choosing a passive filter became impractical. For instance, if one were to consider use of a simple LC passive filter with a corner frequency,  $f_c$ , of 10Hz and choosing large capacitor of 100 $\mu$ F to try and lower the inductor value, the required value still is a larger result with its own set of complications such as tolerance errors and other parasitic characteristics that result in noise at the output.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \therefore L = \frac{1}{C(2\pi f)^2} = \frac{1}{(100\mu)(2\pi(10))^2} = 2.533H \text{ (Too large)}$$

A simple two-stage RC network to form a second order low-pass filter will never have a quality factor, Q, greater than one-half. Most filters require Qs larger than one-half. <sup>[9]</sup> In order to attain greater Q values, positive feedback through amplifiers are required.

#### Butterworth Filter Design

Exploring active filter design, one of the popular topologies is the Butterworth low-pass filter. It is desirable filter to use in that it has a relatively flat frequency response in the passband. It was determined to begin with an odd-ordered filter. Even-ordered was avoided due to a non-ideal principle that was later found to not apply to the design application, but only applied to crossover networks using Butterworth filters. Observing the topology in the figure below, the team first assumed a scale factor determined by the resistor values chosen in the circuit. That scale factor was chosen to be 100,000, and therefore all resistors assumed to be 100k $\Omega$ .



Third-order Low-pass Butterworth Filter

FIGURE 28

Then implementing the normalized values for the capacitors,  $n$ , in the circuit from the Butterworth approximations, their values can be determined for a frequency of 10Hz:

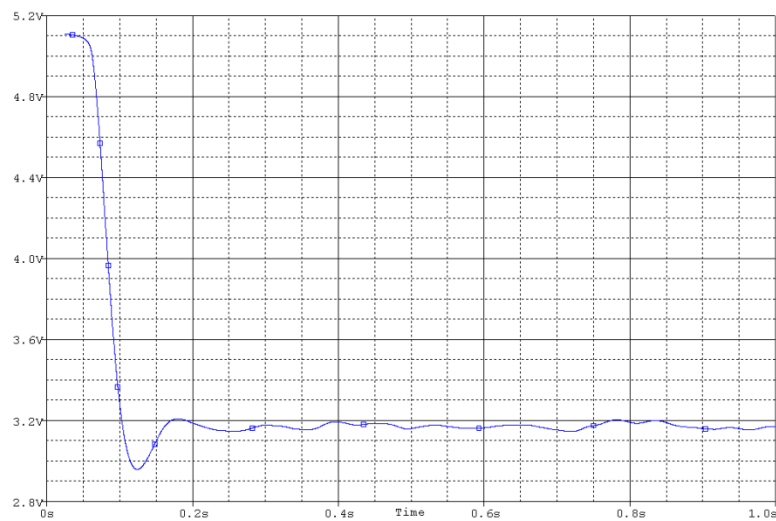
$$R1=R2=R3=100k\Omega;$$

$$C = \frac{n}{2\pi f(100k)}$$

| Capacitor | $n$    | Value (Farad) |
|-----------|--------|---------------|
| C1        | 3.546  | 564.36n       |
| C2        | 1.392  | 221.54n       |
| C3        | 0.2024 | 32.21n        |

TABLE 4

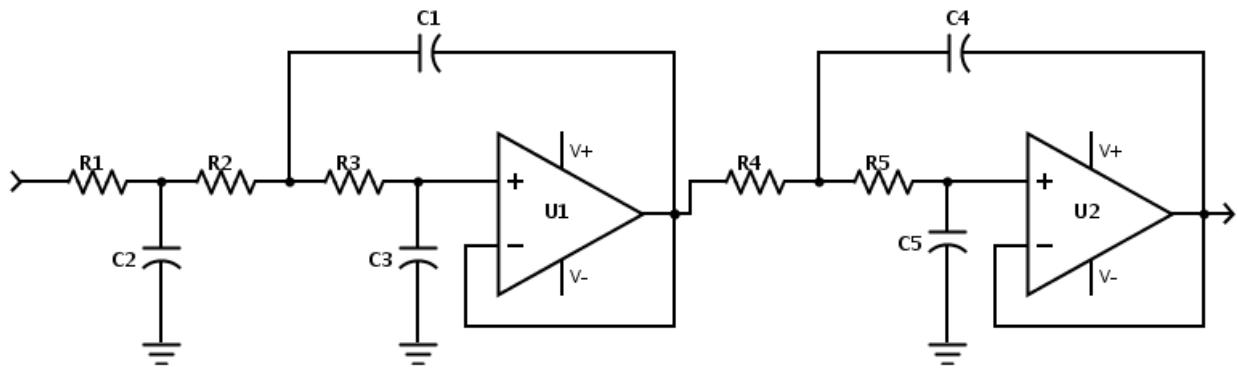
The 3<sup>rd</sup> order Butterworth filter design was tested by simulating it in PSPICE, fed from a comparator (LM139) with inputs from a fixed DC level and a sawtooth waveform. For the op-amps in the filter, LF411s, requiring a dual supply, were chosen due to their availability and versatility. Without thoroughly understanding the expected output, the team was displeased with subtle fluctuations around 50 mV once it reached steady-state in the output, as seen in the figure below.



## PSPICE Simulation of 3<sup>rd</sup> Order Butterworth

FIGURE 29

An initial hypothesis was that by increasing the order, the fluctuations would be less noticeable. The team later realized that the non-ideal fluctuations were not the result of inadequate filter design, but in how the pulse-width modulated input tested on the filter was constructed. Continuing on the trend of keeping an odd-ordered filter, the team then constructed a 5<sup>th</sup> order low-pass Butterworth filter using the topology displayed below. The same scale factor of 100,000 was selected and therefore, following the same methodology as the prior design for a 10Hz corner frequency, came up with new component values for the capacitors.



Fifth-order Low-pass Butterworth Filter

FIGURE 30

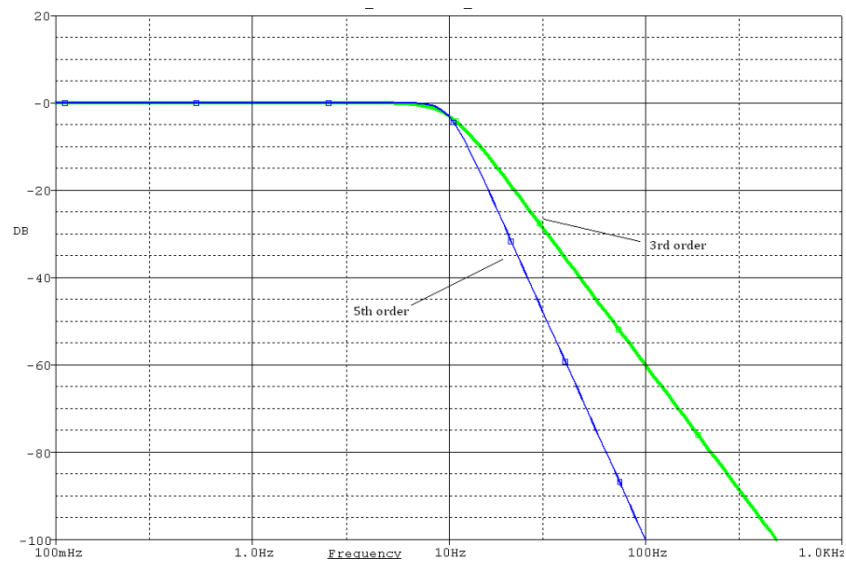
$$R1=R2=R3=R4=R5=100k\Omega;$$

$$C = \frac{n}{2\pi f(100k)}$$

| Capacitor | n      | Value (Farad) |
|-----------|--------|---------------|
| C1        | 1.753  | 279.0n        |
| C2        | 1.354  | 215.5n        |
| C3        | 0.4214 | 67.07n        |
| C4        | 3.235  | 514.87n       |
| C5        | 0.3089 | 49.16n        |

TABLE 5

Again the filter design was simulated in PSPICE. The resultant fluctuations were similar in magnitude, though at the time, it was still unclear from the team's understanding that it was not the fault of the filter. It was believed that it would be beneficial to have the increased attenuation rate in the frequency domain of the 5<sup>th</sup> order filter at approximately -100 dB per decade.



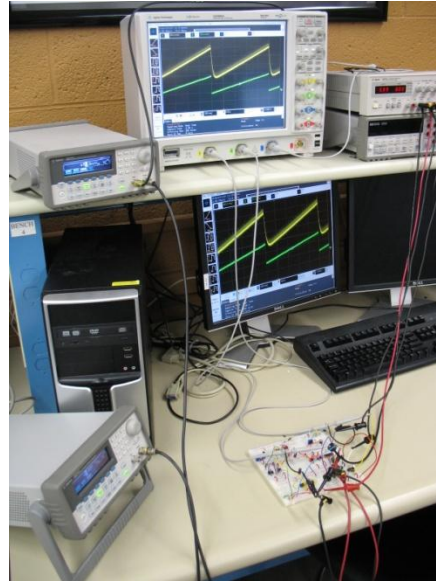
PSPICE Frequency Response of 3<sup>rd</sup> and 5<sup>th</sup> order Butterworth Filters

FIGURE 31

The 5<sup>th</sup> order Butterworth filter was our first demodulator constructed on the breadboard for physical testing.

#### Butterworth Filter Testing

At the time of assembling the Butterworth low-pass filter on the breadboard, the constraints of the transmitter were still in development. The simple comparator topology with external test equipment was still the driving inputs. The input of the transducer was simulated as a ramp function changing at a frequency of 1Hz driven by a function generator, while a 1kHz sawtooth waveform was also being output from a function generator. The output of the comparator was then input to the filter.



Test Setup of Butterworth Filter

PICTURE 1

The goal was to observe the output trends of the filter, paying special attention to linearity and fluctuations due to changes in the input.



Output (Yellow) Compared to Input (Green) in Butterworth Filter Test

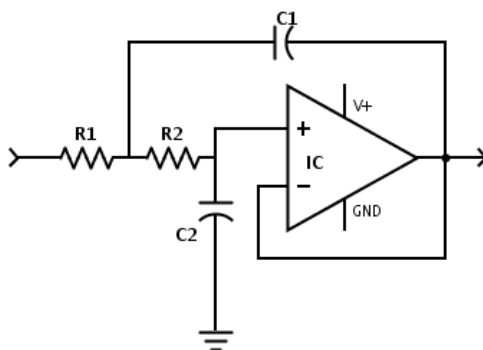
FIGURE 32

Upon inspection, some disapproval came in regards to linearity. Some delay was expected from the transitioning from high to low of the ramp function, but subsequent data collection began to show a trend of a decreasing slope at the high end of the output. Some ringing was also occurring from using a higher order filter than what was necessary. A concern about how dual supplies were needed for the LF411 op-amp also became a prominent

discussion. The team was uncertain about have a negative supply readily available. As far as what was understood during that stage of development, only a single power supply was needed at the transmitter. A new approach toward a low-pass filter with more linear response using single supply op-amps was needed.

### Bessel Filter Design

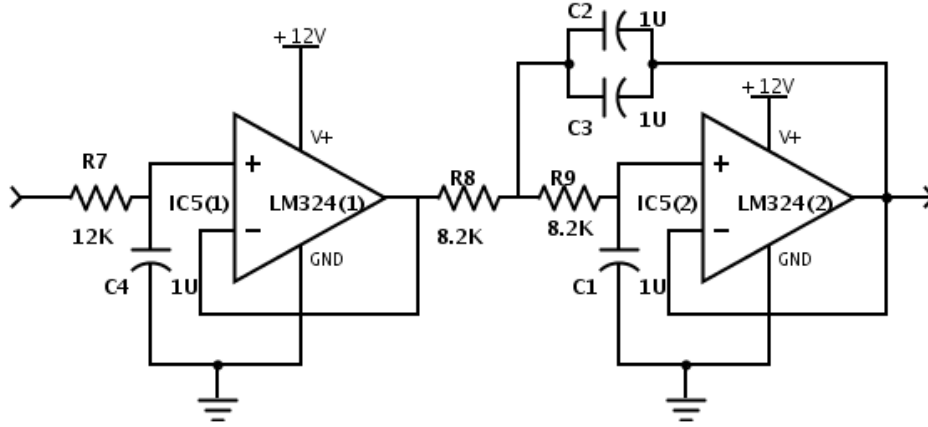
Though higher attenuation rate was achieved through a relatively higher order Butterworth filter, not enough attention was given to the time domain response of our demodulator. More awareness needed to be given to the damping factor contributed by the receiver modeled as linear time invariant (LTI) system. As mentioned before in the team's consideration of active filter design, a higher Q factor was desired, but the low-pass filter was too underdamped. The ringing and overshoot were undesirable in the output. Another filter design was needed to achieve a critically damped response. The team chose to try to construct a Bessel filter. Bessel filters have the most linear phase response, thereby the flattest group delay. Therefore, for any components causing delay within our circuit becomes delayed by a relatively similar amount of time, such that the output will have a smoother approach to steady-state. A Sallen-Key topology is one similar to the construction exhibited in the previously discussed Butterworth filter, except it is a second-order model for active filter design whose novelty for use is emphasized in its simplicity. The responses of the topology or transfer functions, determined by the chosen component values, classify each filter as Butterworth, Bessel, etc.



Sallen Key Low-pass Filter

FIGURE 33

Using a Sallen-Key topology with a unity gain voltage follower with resistors and capacitors of the same value achieves a step response very close to being critically damped. Another enticing quality for the Sallen-Key topology, specific to the team's latest challenge, is the use op-amp in a non-inverting mode; therefore the single-ended power supply can be used. The team was able to design a third-order Bessel low-pass filter in a two stage form utilizing the Sallen-Key architecture via software developed by Texas Instruments. The software called Filter Pro™, made for users to perform various forms of electronic filter design, was utilized to alleviate the time needed to perform hand calculations. In the Appendix, the necessary steps taken to develop the Bessel filter can be viewed. The resultant low-pass filter from the software can be seen below with component values chosen to be the closest standard value. The component labeling is based on a convention that applies to the completed design that will be later shown. The previous LF411 op-amps were replaced with the quad op-amp package, LM324, which had a single-ended supply capability and exceeded the LF411 performance.



Bessel Filter Low-pass Filter Design

FIGURE 34

There is two stages to the low-pass filter with two slightly difference corner frequencies. The first stage is a passive RC filter with a unity gain voltage follower to provide a high input impedance at the output and not load down the gain of the filter while maintain the corner frequency. The corner frequency and Q factor can be derived by the following equations:

$$f_c = \frac{1}{2\pi R7 C4} = \frac{1}{2\pi (12k)(1\mu)} = 13.3\text{Hz}$$

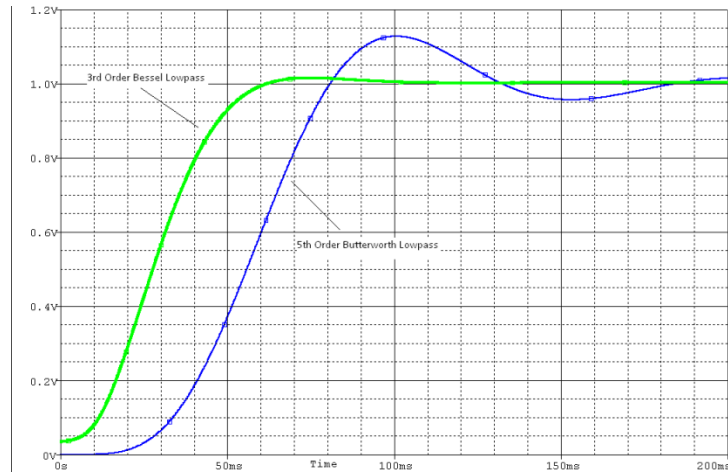
$$Q = \frac{\frac{1}{2\pi f_c C4}}{R7 + (\frac{1}{2\pi f_c C4})} = \frac{\frac{1}{2\pi (13.3)(1\mu)}}{(12k) + (\frac{1}{2\pi (13.3)(1\mu)})} = 0.5$$

The second stage is the Sallen-Key topology that has a corner frequency and Q factor that can be derived from the following relationships:

$$f_c = \frac{1}{2\pi \sqrt{R8 R9 C1 (C2 + C3)}} = \frac{1}{2\pi \sqrt{(8.2k)(8.2k)(1\mu)(1\mu + 1\mu)}} = 13.7\text{Hz}$$

$$Q = \frac{\sqrt{R8 R9 C1 (C2 + C3)}}{C1 (R8 + R9)} = \frac{\sqrt{(8.2k)(8.2k)(1\mu)(1\mu + 1\mu)}}{1\mu (8.2k + 8.2k)} = 0.707.$$

The design was simulated in PSPICE using a step input to verify the filters impulse response, and the improvement in the filter's quality factor can be seen as the output did not exhibit the underdamping that was not desired.

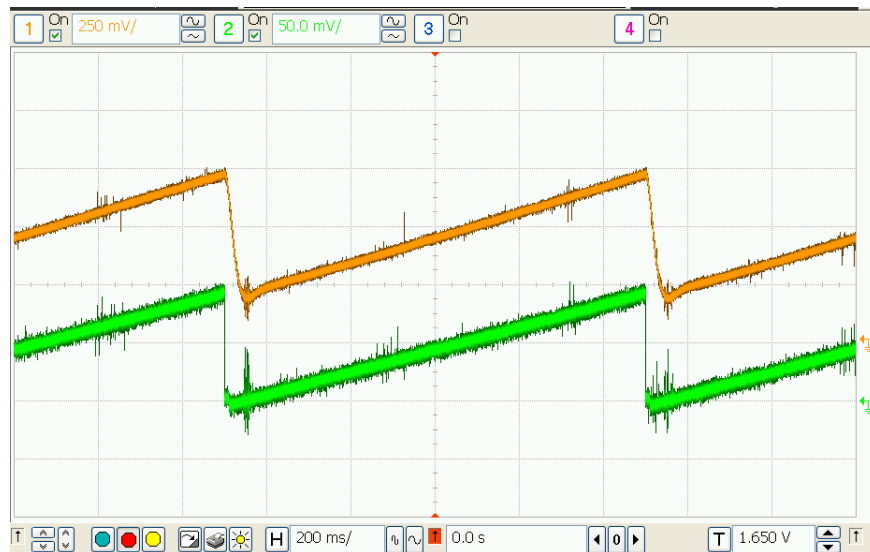


PSPICE Comparison of Lowpass Filter Designs

FIGURE 35

### Bessel Filter Testing

The lowpass Bessel filter design was assembled quickly as the LM324 was available within the ECE department shop. Using the same test setup as what was tested on the previous Butterworth design, the ripple and non-linearity in the output was no longer as evident.



Output (Yellow) Compared to Input (Green) in Bessel Filter Test

FIGURE 36

The third-order Bessel filter design was chosen to be the team's method of demodulation. Moving forward revolved around understanding was the constraints of the pulse-width modulated signal that was going to be output by the transmitter as the receiver input.

## OPTIMIZATION OF THE RECEIVER

### Understanding the Transmitted Signal

Mentioned previously were the steps necessary to complete construction of the transmitter or modulator. Once design and testing of the transmitter had reached an acceptable performance level, the team was able to procure 500 feet of shielded twisted-pair wire (22 AWG), Belden 8761, from MSU Surplus to verify and test the theoretical expectations of the project.

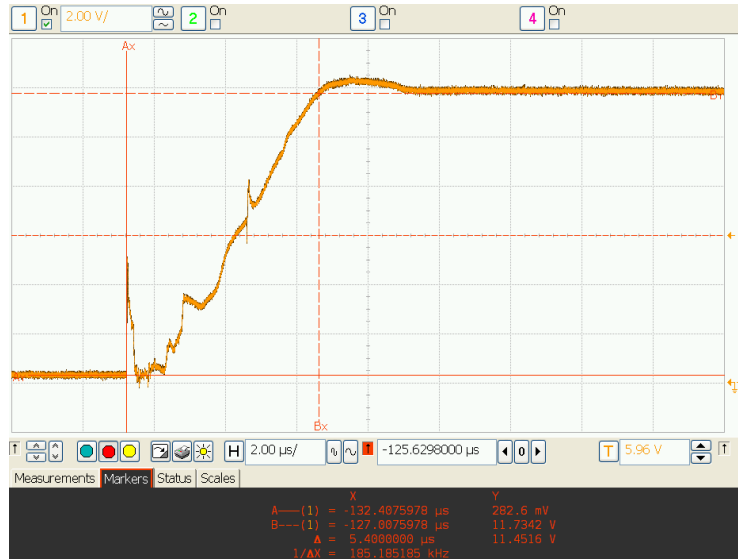


Belden 8761 Shielded Twisted-Pair Wire

PICTURE 2

The length of the wire was understood not be approximately 20% of the maximum anticipated length of the transmission line. Though based on the performance of 500ft, some assumptions or conclusions could be made on how to optimize the receiver to prepare the signal to be passed through the lowpass filter.

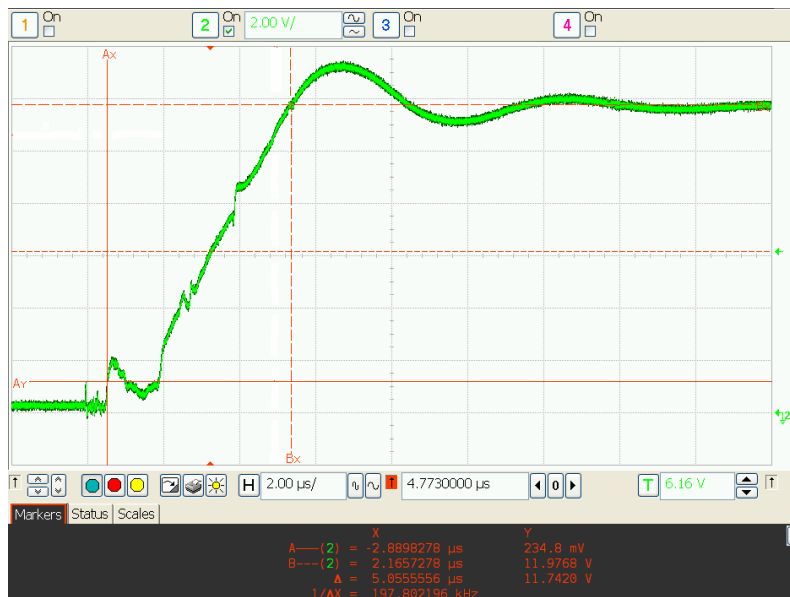
Particular attention was given to the rising edge of a pulse from the transmitter. The test PWM output from the transmitter was established to be about at a duty cycle of 75% of 1kHz signal. Some noise and ripple was observed on the rising edge before the signal was then driven down the transmission line. The rise time, identified for the experiment to be the time required to rise from 0% to 100%, was approximately 5.4 $\mu$ s.



Test Pulse Measured at the Input to the Transmission Line

FIGURE 37

What was observed at the output of the shielded twisted-pair wire had surprising results. The rise time was measured at approximately  $5.06\mu\text{s}$ . The rise time appeared to improve along the transmission, though after deliberation seemed to be an illusion. At  $2\mu\text{s}$  per division, each subdivision is approximately  $0.4\mu\text{s}$ . The first noise spike at the transmitter is about the width of a subdivision or the  $0.34\mu\text{s}$  difference lost in the transmission. The team's best estimate is that the wire acted as a lowpass filter and did not even register the first jump until a point where it reached its maximum and it can begin to be recognized on its falling edge with some delay added. The subsequent noise spikes became less defined. Some overshoot was also added.



Test Pulse Measured at the Output of the Transmission Line

FIGURE 38

In line with the previous filter discussion, the selection of the Belden 8761 worked to the benefit of the project. It appeared to filter out the unwanted noise in the transmitter's output. The overshoot can also be attested to the changing of the damping factor and making the pulse slightly more underdamped. Perhaps the most significant conclusion is that virtually no loss in the rise time or the subsequent measurements in fall time were observed in the pulse train. A conclusion was made that for the remaining distance implemented at the ArcelorMittal site, one could expect that noise ripples will become attenuated away and that any delay added to the rise/fall time will be within an acceptable tolerance. However, to alleviate any uncertainty, the full integrity of the pulse waveform and duty-cycle should be attempted to be restored at the receiver.

## REPEATER DESIGN

A comparator circuit was used as a tool to create the PWM signal, and the same principle could be used to restore it from any distortion that may have occurred when it is used again as a repeater.

A choice had to be made on an acceptable voltage threshold value where the comparator, the LM339, would switch from low to high and vice versa. As discussed in a previous portion, there existed an initial noise spike of concern from the transmitter that had a potential maximum of nearly 2V that dipped by approximately 1V before rising again. A fixed DC bias had to be established and applied at the inverting input of the comparator that was greater than or equal to 1V, but not too great that it did not accurately capture the moment of switching. Such a compensation method could be revisited if the actual distance at the site contributed greatly to the distortion of the original PWM signal where a near perfect duty cycle restoration could be calibrated. The team chose an approximate 1.1V reference, performed by a voltage divider of the power supply (12V) using a 8.2k $\Omega$  and a 82k $\Omega$  resistor. An improvement to the design would be for a 10k $\Omega$  potentiometer to be used in place of the 8.2k $\Omega$  resistor.

$$V_{\text{ref}} = \frac{8.2k}{8.2k + 82k}(12V) = 1.09V$$

As mentioned prior in the transmitter portion, as to avoid loading effects changing the shape of the pulse-width modulated waveform, a unity gain voltage follower, using the aforementioned single-supply OPA140, was connected at the output of the comparator circuit. All subsequent mentioning of unity gain buffers employ the use of the OPA140.

## REPEATER TESTING

There existed a slight lengthening of the duty cycle in the measurements performed after the construction of the repeater. The frequency of the transmitted PWM signal is approximately 1.0135kHz or a period of 986.667 $\mu$ s. For a 75% duty cycle with marker set approximately half way between the transition states, the pulse duration is 740 $\mu$ s. Output from the repeater was a 75.2% duty cycle or a pulse duration of 742.222 $\mu$ s with a virtually non-existent rise/fall time so the markers were set in line with the transition state. This result could be indicative that the choice of the bias reference level should be increased to a higher voltage threshold.



### PWM Input to the Repeater

FIGURE 39



### PWM Output from the Repeater

FIGURE 39

### CLIPPER CIRCUIT DESIGN

Fundamental to preparing of PWM output from the repeater for averaging was defining a range of output that would be acceptable to be read by the PLC. The specification limit provided by Arcelormittal was voltage range between 1 and 5V. The team felt it was not imperative to design the average for use of the full voltage range. It was important to design for around a linear relationship found within the range. The input provided from the transducer was an approximation, ranging from 0 to 100mV. As long as the team found a linear region within the span of 1 to 5V, there would be sufficient margin on the top and bottom for flexibility, such as if the load limit was expanded, and performance improvement. Therefore the goal of the team's averaging circuit, accomplished by the Bessel filter, was to provide a linear region of voltage in a range from 2 to 4V that represents the full span of the existing transducer range. As stated in the modulator portion, the duty cycle range available was between 25% and 75%. The most important relationship to the design project was represented in the following equation:

$$V_{AVG} = V_{HIGH\_PWM}(Duty\ Cycle\%) + V_{LOW\_PWM}(1 - Duty\ Cycle\%).$$

Therefore by assuming the "HIGH" state of the pulse to be 5V and the "LOW" state to be 1V, using the given range of the duty cycle, the average voltage at the output of the lowpass filter will be confined within a range of 2 to 4V.

$$V_{AVG} = (5V)(0.75) + (1V)(1 - 75\%) = 4V$$

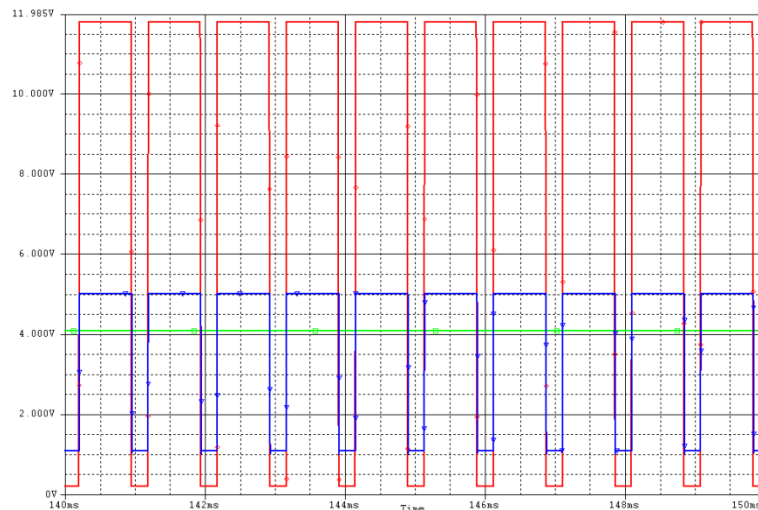
$$V_{AVG} = (5V)(0.25) + (1V)(1 - 25\%) = 2V.$$

In order to clip the high state of the PWM output at a voltage limit of approximately 5V, a 1N4733 Zener diode was placed at the output the repeater followed by a unity gain buffer to provide isolation to the following stage of the clipping circuit. At the next stage of the clipping circuit, a resistive voltage divider sets a 1.1V bias in the similar relationship discussed in the repeater portion, in order to lift the low state of the PWM signal up. A 1N4148 diode was placed at the output of the voltage follower to provide isolation from the low impedance of the buffer output

from the biasing provided by the power supply. The final unity gain buffer used is to prevent loading effects between the biasing network and the input of the Bessel filter.

### CLIPPING CIRCUIT TESTING

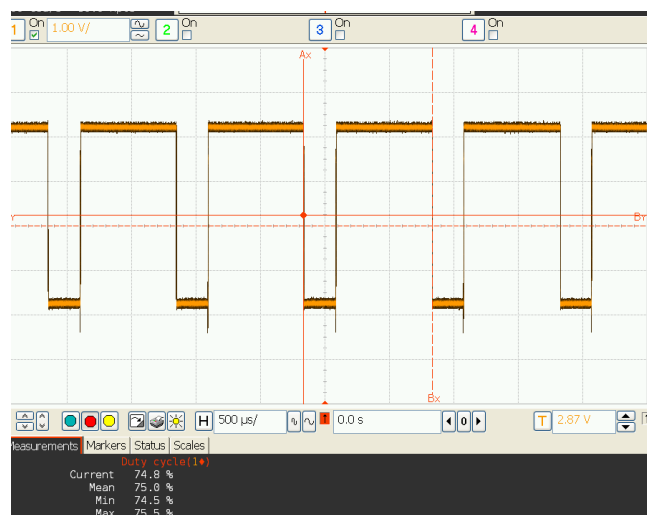
The completed receiver design, adding the final clamping stage, was simulated and analyzed in PSPICE.



PSPICE Simulation of Receiver (Output of Repeater – Red, Output of Clamping Circuit –Blue, Output of the Bessel Filter – Green)

FIGURE 41

The actual physical construction tested on the breadboard was very comparably to what was simulated. However, more thorough physical testing upon the breadboard could have been performed before the circuit was sent to the ECE shop for fabrication onto the PCBs. In the Appendix the steps taken to place the receiver onto a PCB using the Eagle software can be found.



Output of the Clamping Stage at a 75% Duty Cycle

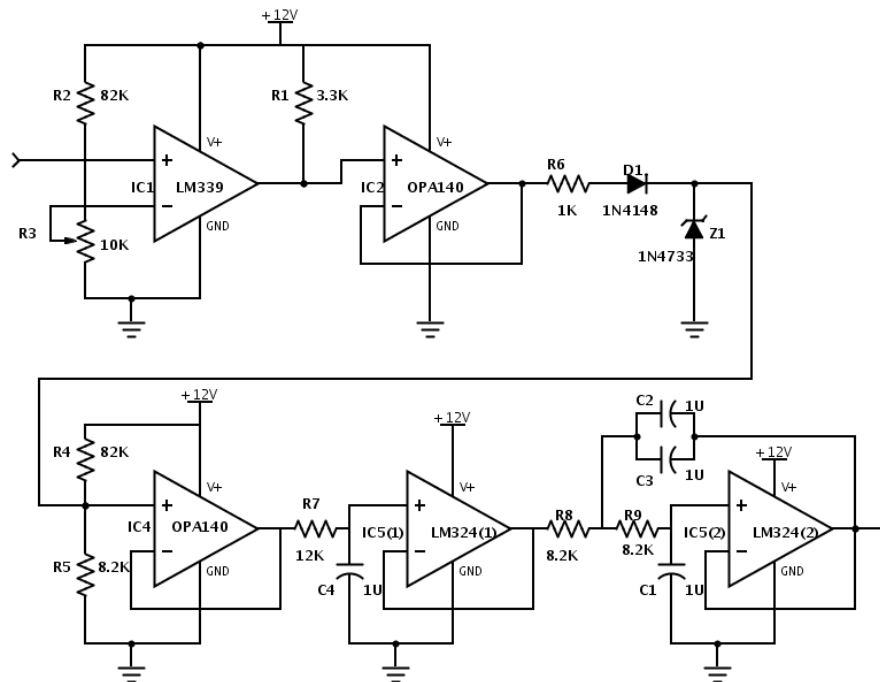
FIGURE 42



Output of the Bessel Lowpass Filter at 75% Duty Cycle

FIGURE 40

One point of optimization was noticed in that one more unity gain buffer was used than what was necessary for the design, and could have been avoided if component order was slightly reconfigured. The recommended layout, also taking into account the potentiometer used at R3, can be seen in the figure below. The design was reaffirmed in PSPICE, though never actually constructed.



Recommended Improvement for Final Design

FIGURE 44

## CHAPTER 4

### GENERAL SPECIFICATIONS

Team five's final design of the Load Metering Transmission included two PCBs one for the transmitter portion and one for the receiver portion. These PCBs were mounted into an enclosure with two four pin connectors on each. According to the sponsor, ArcelorMittal, the design needed to be able to transmit a power signal over a great distance and receive the signal with tolerable error. The received signal was to be ready for a PLC card input and was to give reliable data on the power usage at the mills. This signal was to be updated so that the output was visually continuous. In other words the signal was not to be choppy when viewed on a computer screen. The cases need to fit in the areas that were identified at the plant and needed also to be light enough to rest in the area provided. The circuit was to be powered by a 24VDC or less positive input signal and was to be as low wattage as possible. The team decided that the design was to be as easy to understand as possible so that any issues could be resolved by the team when asked to perform maintenance or resolve an issue with the circuit if one were to arise. The design was also to be robust and capable of handling the amount of heat that would be generated in a switchgear type building as well as the cold of an Indiana winter. The circuit was to perform as a dependable backup to the current system until such time as this entire system could be replaced.

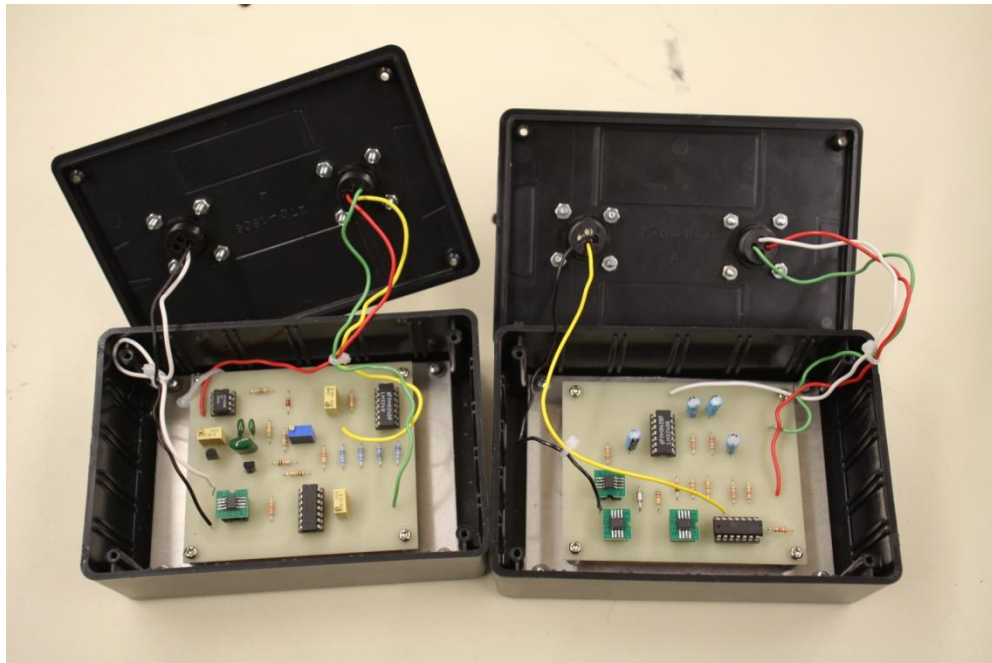
### DISCUSSION OF SPECIFICATIONS

The final design was tested and was successful according to the specifications that were agreed upon by the sponsor and team five. For the sake of verifying reliability, the project passed three separate tests that were done on three separate days. Initially there was an issue with calibration, but the issues were resolved during the course of the testing. The circuit performed better than expected and surpassed the specifications given by the sponsor. As a qualitative test, the signal was transmitted across a long length of cable with transformer windings of an inductively noisy power supply being passed over the cable. The received signal conformed to the specifications of a PLC card. The signal was transmitted at roughly one kilohertz which gives an updated data point every millisecond. This is more than enough intervals to maintain a smooth signal. The enclosures were much smaller than anticipated and provided seventy-five percent spare room in the spaces provided. The circuit operates at 12VDC and draws roughly 500mW. Power consumption is low when compared to the power available at any time at the plant. The circuit will operate continuously, but both the team and the sponsor deemed the usage acceptable. Since the circuit that was created was designed and built from the component level, the team understands every section of the circuit and how it operates. Using buffering to isolate sections of the circuit decreased the amount of variation in the circuit by decreasing any loading effects. The circuit is designed to be calibrated and can be adapted to change in environment or drift that may occur over time. Potentiometers can be adjusted to achieve a variable output level and range. The circuit is limited to a high temperature of 85°C and a low temperature of -40°C by the capacitors and the LM324 IC. This temperature will be sufficient for the environment that the project will encounter. The circuit will be a dependable backup to the existing system, and will transmit the power signal in a cost effective manner.

## ENCLOSURE

The final circuits were mounted to cases that were bought at Radio Shack™. These cases were six inches long, 4 inches wide and 2 inches deep. This was the minimum amount of space that was needed to fit a three by four inch circuit board with standoffs and mount connectors on the top of the enclosure. A bottom plate was attached to the standoffs of the enclosure because they did not fit the PCB dimensions. The PCB was then attached to this plate with insulated standoffs. The Tyco™ Amp-style four pin connectors were then mounted on the top of the enclosure. Wires were crimped to the pins and inserted in the plastic connector piece. The transmitter and receiver both have two connectors. One is for the transmission line signal and ground. The other is for the input or output signal, one is for power, and one is for ground. For color coordination of the wire leads, green/black wires were set to be ground, red wires were used for power, yellow was the input signal to the device, and white wires were established to be the output. When the twisted pair transmission line is connected to the circuit it is important to only connect the ground shield on one side so that ground currents do not flow through the line. The top of the enclosure can be sealed in with screws to prevent tampering after the circuit has been calibrated.

The following pictures show the final design.



**PICTURE 3** TRANSMITTER (LEFT) AND RECEIVER (RIGHT)

The bottom plate and circuit board can be seen mounted in the enclosure in Picture 1. The signal, power, and ground wires are zip-tied and inserted into the connectors on the cover of the enclosure. The covers can be screwed down as shown in Picture 2.



**PICTURE 4** TRANSMITTER AND RECEIVER SHOWN SEALED.

## TESTING PROCESS

On the three tests performed on the circuit for the reliability test, all of them yielded results that were within the specifications and actually exceeded expectations. It was initially decided that the signal should be accurate up to plus or minus two percent. Since the input signal is from 0 to 100mV and the output is designed to be from 2 to 4V, we can derive an equation to calculate the desired output based on a test input value.

The equation is as follows:

$$\text{Desired Output} = (\text{Input}) \times (\text{Gain Factor}) + (\text{Offset Factor})$$

The gain factor can be determined as follows:

$$\begin{aligned}\text{Gain Factor} &= \frac{(\text{Max Output Value}) - (\text{Min Output Value})}{(\text{Max Input Value}) - (\text{Min Input Value})} \\ &= \frac{(4V) - (2V)}{(100mV) - (0mV)} = 20\end{aligned}$$

The offset factor can be determined as follows:

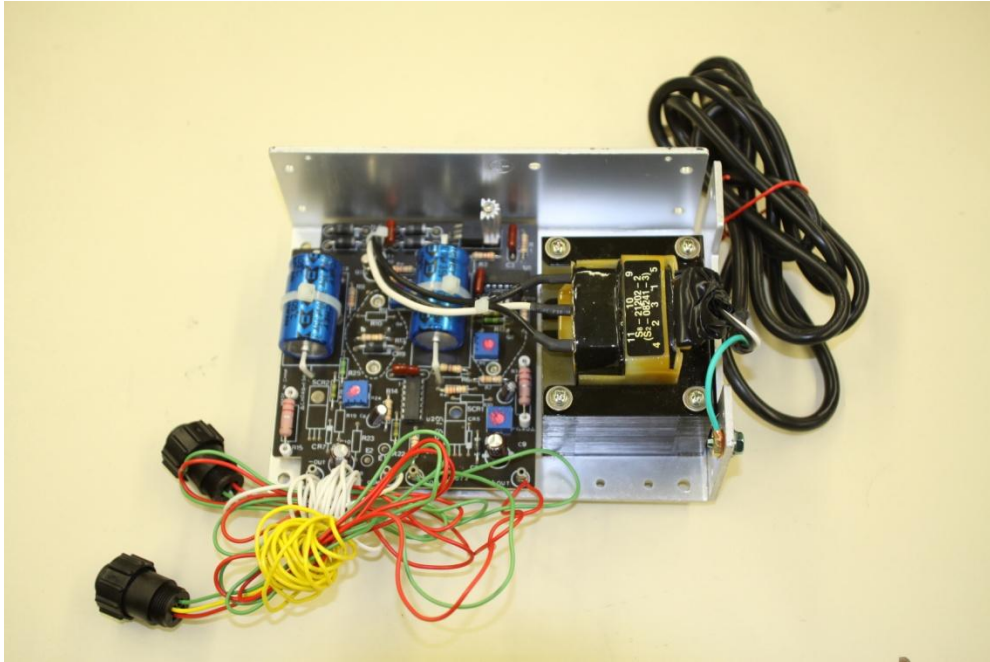
$$\begin{aligned}\text{Offset Factor} &= (\text{Min Output Value}) - (\text{Min Input Value}) \\ &= 2V - 0mV = 2V\end{aligned}$$

This equation was used to test the output data and determine the percent error. Once the percent error was calculated a plot was made from the data that was collected and correlation was checked. If the data showed a real correlation then there may be a problem with the circuit or the calibration method. If the plot showed no real correlation there could either be a problem with the components or waveforms being non-linear or the input and measurement devices are causing an error in the output data due to accuracy. All of this was taken into account when looking at the data collected and once all three tests were completed the data was sufficient to draw solid conclusions.

## TEST PREPARATION

The tests were performed on three separate days using three different input signal power supply and oscilloscope stations. Scope probes were initially checked for correct compensation and then the circuits were connected to a 12V power supply that was graciously donated by the MSU Cyclotron.

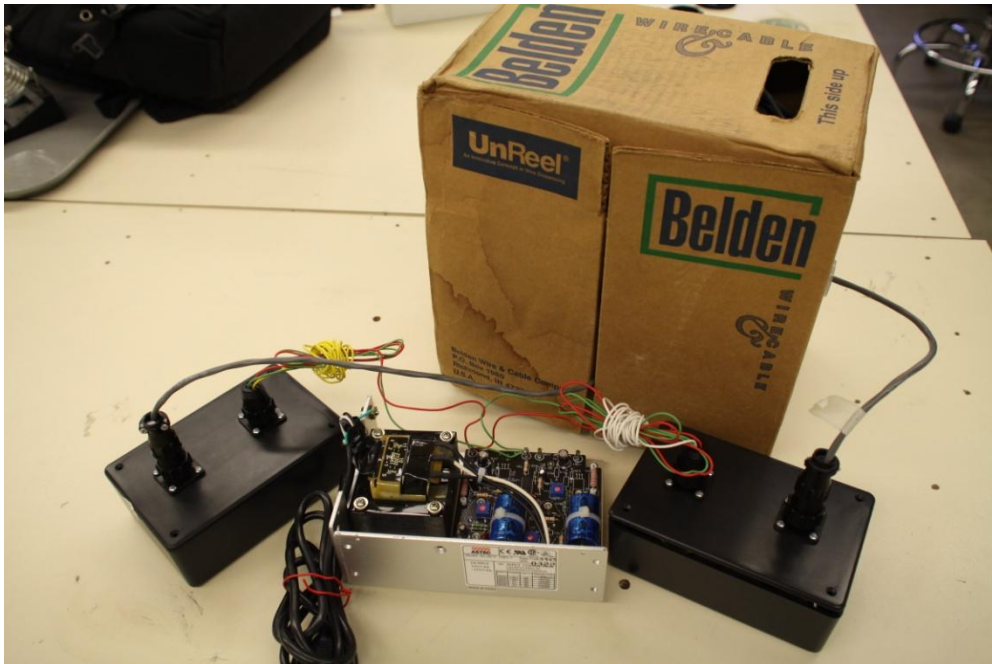
The follow picture shows the power supply that was used in the testing process:



PICTURE 5

The transmitter was attached to one side of a 450 foot twisted shielded pair cable and the receiver was attached to the other side.

The connections can be seen in the following picture:



PICTURE 6

Once the circuit was connected an input power signal was set up using the HP E3630A power supply in lab. An input of 110mV placed on one side of a 10 turn 10KΩ potentiometer. This allowed for the level of accuracy needed to plot the waveforms with roughly equidistant points. The input was connected to the other side of this potentiometer and measured with the Agilent 33250A multimeter. The output was connected to the Agilent DSO9064A oscilloscope. Inputs of 0 to 100mV with 5mV steps were placed at the input and the output was recorded. The output was then check for error based on the equation derived above and the following error equation.

$$\% \text{ ERROR} = \frac{(\text{Measured Value}) - (\text{Expected Value})}{(\text{Expected Value})}$$

The average, maximum, and mean errors were then calculated and the results were plotted for each test.

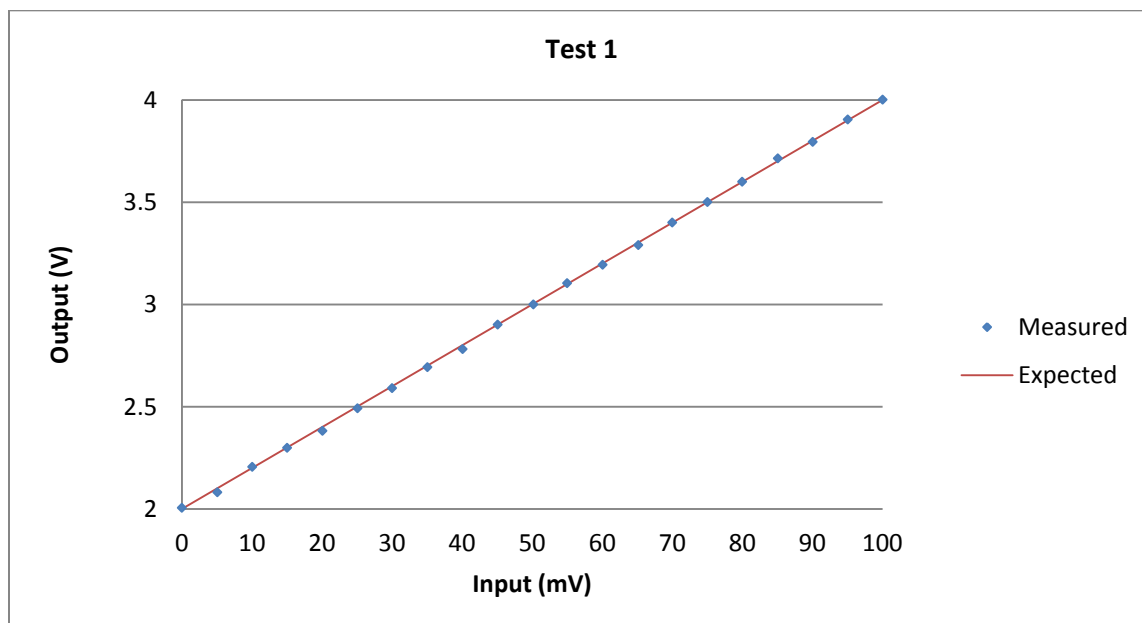
#### CALIBRATION

It was determined after many preliminary tests that the best way to calibrate the circuit is to set the input to 0mV and adjust the input offset potentiometer so that the output is at 2V. The input is then changed to 100mV and then gain potentiometer is adjusted so that the output is exactly 4V. The offset can be thought of as the y-intercept of a line and the gain is the slope of the line. This calibration was performed before each test.

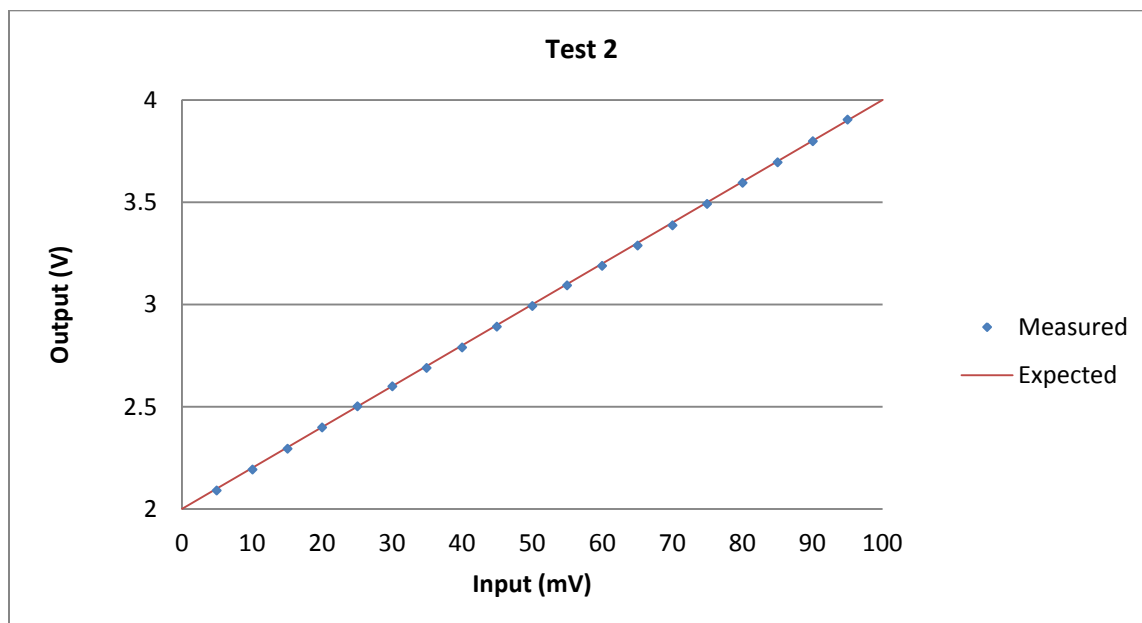
#### TEST RESULTS

Figure 47 below shows the numerical data as well as visual plots of the data from 0 to 100mV at 5mV input intervals for three different tests. Each test was perform two days apart from another.

| Test 1     |            |            |                 |        |
|------------|------------|------------|-----------------|--------|
| Test       | INPUT (mV) | OUTPUT (V) | THEORETICAL (V) | ERROR  |
| 0          | 0.001      | 2.00572    | 2.00002         | 0.28%  |
| 5          | 5.05       | 2.08125    | 2.101           | -0.94% |
| 10         | 10.03      | 2.2058     | 2.2006          | 0.24%  |
| 15         | 15.023     | 2.29867    | 2.30046         | -0.08% |
| 20         | 20.075     | 2.38171    | 2.4015          | -0.82% |
| 25         | 25.075     | 2.4924     | 2.5015          | -0.36% |
| 30         | 30.001     | 2.59061    | 2.60002         | -0.36% |
| 35         | 35.051     | 2.69314    | 2.70102         | -0.29% |
| 40         | 40.087     | 2.78211    | 2.80174         | -0.70% |
| 45         | 45.086     | 2.90133    | 2.90172         | -0.01% |
| 50         | 50.178     | 3.00054    | 3.00356         | -0.10% |
| 55         | 55.002     | 3.10463    | 3.10004         | 0.15%  |
| 60         | 60.061     | 3.19471    | 3.20122         | -0.20% |
| 65         | 65.17      | 3.2905     | 3.3034          | -0.39% |
| 70         | 70.004     | 3.40114    | 3.40008         | 0.03%  |
| 75         | 75.025     | 3.50119    | 3.5005          | 0.02%  |
| 80         | 79.995     | 3.60066    | 3.5999          | 0.02%  |
| 85         | 85.081     | 3.71481    | 3.70162         | 0.36%  |
| 90         | 90.069     | 3.79544    | 3.80138         | -0.16% |
| 95         | 95.06      | 3.90509    | 3.9012          | 0.10%  |
| 100        | 100.04     | 4.0019     | 4.0008          | 0.03%  |
| AVG ERROR= |            |            |                 | 0.27%  |
| MAX ERROR= |            |            |                 | 0.94%  |
| MEAN=      |            |            |                 | -0.15% |



| Test 2     |            |            |                 |        |
|------------|------------|------------|-----------------|--------|
| Test       | INPUT (mV) | OUTPUT (V) | THEORETICAL (V) | ERROR  |
| 0          | 0.002      | 1.99493    | 2.00004         | -0.26% |
| 5          | 4.97       | 2.09023    | 2.0994          | -0.44% |
| 10         | 10.09      | 2.19293    | 2.2018          | -0.40% |
| 15         | 15.081     | 2.29426    | 2.30162         | -0.32% |
| 20         | 20.031     | 2.39836    | 2.40062         | -0.09% |
| 25         | 25.063     | 2.50196    | 2.50126         | 0.03%  |
| 30         | 30.051     | 2.59964    | 2.60102         | -0.05% |
| 35         | 34.952     | 2.68947    | 2.69904         | -0.35% |
| 40         | 40.011     | 2.78976    | 2.80022         | -0.37% |
| 45         | 44.977     | 2.89137    | 2.89954         | -0.28% |
| 50         | 50.033     | 2.99275    | 3.00066         | -0.26% |
| 55         | 55.002     | 3.09334    | 3.10004         | -0.22% |
| 60         | 60.009     | 3.1889     | 3.20018         | -0.35% |
| 65         | 65.075     | 3.28869    | 3.3015          | -0.39% |
| 70         | 70.05      | 3.38709    | 3.401           | -0.41% |
| 75         | 74.985     | 3.49178    | 3.4997          | -0.23% |
| 80         | 80.046     | 3.59514    | 3.60092         | -0.16% |
| 85         | 85.07      | 3.69502    | 3.7014          | -0.17% |
| 90         | 90.083     | 3.79838    | 3.80166         | -0.09% |
| 95         | 95.035     | 3.90449    | 3.9007          | 0.10%  |
| 100        | 100.048    | 4.00456    | 4.00096         | 0.09%  |
| AVG ERROR= |            |            |                 | 0.24%  |
| MAX ERROR= |            |            |                 | 0.44%  |
| MEAN=      |            |            |                 | -0.22% |



| Test 3     |            |            |                 |        |
|------------|------------|------------|-----------------|--------|
| Test (mV)  | INPUT (mV) | OUTPUT (V) | THEORETICAL (V) | ERROR  |
| 0          | 0.002      | 1.9956     | 2.00004         | -0.22% |
| 5          | 5.025      | 2.08801    | 2.1005          | -0.59% |
| 10         | 9.96       | 2.18846    | 2.1992          | -0.49% |
| 15         | 14.994     | 2.29619    | 2.29988         | -0.16% |
| 20         | 20.063     | 2.39956    | 2.40126         | -0.07% |
| 25         | 25.072     | 2.50118    | 2.50144         | -0.01% |
| 30         | 30.074     | 2.5992     | 2.60148         | -0.09% |
| 35         | 34.998     | 2.6999     | 2.69996         | 0.00%  |
| 40         | 40.06      | 2.80101    | 2.8012          | -0.01% |
| 45         | 45.062     | 2.90056    | 2.90124         | -0.02% |
| 50         | 50.032     | 2.99565    | 3.00064         | -0.17% |
| 55         | 55.068     | 3.1036     | 3.10136         | 0.07%  |
| 60         | 60.014     | 3.20607    | 3.20028         | 0.18%  |
| 65         | 65.039     | 3.30958    | 3.30078         | 0.27%  |
| 70         | 70.04      | 3.40967    | 3.4008          | 0.26%  |
| 75         | 75.001     | 3.50505    | 3.50002         | 0.14%  |
| 80         | 80.009     | 3.60443    | 3.60018         | 0.12%  |
| 85         | 85.072     | 3.7051     | 3.70144         | 0.10%  |
| 90         | 90.028     | 3.80186    | 3.80056         | 0.03%  |
| 95         | 95.007     | 3.90186    | 3.90014         | 0.04%  |
| 100        | 100.055    | 4.00428    | 4.0011          | 0.08%  |
| AVG ERROR= |            |            |                 | 0.15%  |
| MAX ERROR= |            |            |                 | 0.59%  |
| MEAN=      |            |            |                 | -0.03% |

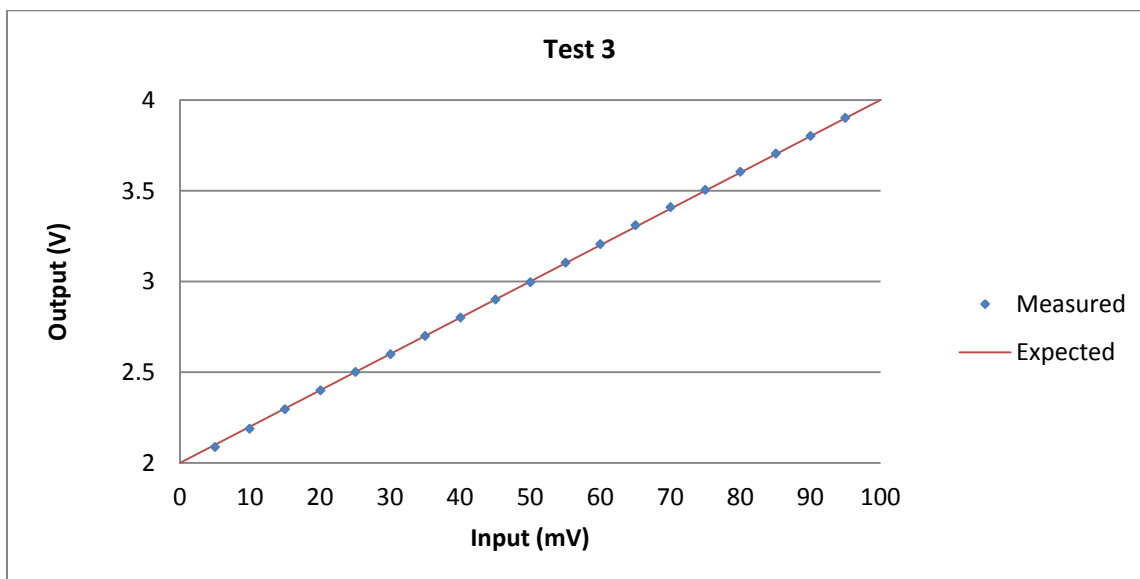


FIGURE 47

The results were very accurate. The largest magnitude error was 0.94% and the team safely assessed that the error was within plus or minus one percent. The average error for all tests was very low at 0.22%. The mean for each test is -0.22%, -0.15%, and -0.03%. The team thought that these figures were very important to determine the success of the project. The mean shows that the spread for each test is very closely centered around the expected results. Seeing that the mean is less than the average error it was suspected that the measurement devices have some error associated with them. As long as there are no high magnitude max errors and the average error is low one could assume that a line could be drawn at -0.22% from the expected results, the highest mean error. This line would indicate the normal error inherent in the product. It would be better if the values fluctuated around 0% mean error, and then it could be said that there is most likely only a measurement device or setup type error.

To encapsulate the whole picture though, each individual graph must be analyzed for a correlation in the data. If two or more of the graphs have a similar correlation then there may be a problem with the calibration method or potentially non-linearity in the circuit. Test 1 had the largest max error at 0.94% and this error seems to occur in an area that is inconsistent with the rest of the graph. The area of plots with the greatest error was within the range from 0mV and less than 20mV. This test also has increasing error from negative to positive. This would indicate that the calibration offset is slightly low and the calibration gain is too high. Test 2 does not show the same type of non-linearity in the lower values but seems to have a consistent negative error correlation. This is simply an offset calibration error. If the offset were to be corrected then all values would increase by the same amount. Test 3 is similar to Test 1 with non-linearity in the lower values. It also has increasing error from negative to positive.

The results are twofold. The first analysis would indicate that there is a normal error inherent to circuit and due to component values tolerances. The second result is that there is some non-linearity issues for input values greater than 0mV and less than 20mV. The remaining correlation is due to calibration error and can be corrected if the potentiometers are precise enough to correct the errors.

#### CALIBRATION ISSUE

There seems to be a calibration issue with the circuit. When the circuit is powered down it loses calibration and must be recalibrated. This is an issue that the team could not determine the cause of, but we speculate that there may be some inductance in the potentiometers and when they are powered down they shift slightly. This will not be an issue at the plant because the system is tied to a backup battery bank. If the power were to be disconnected from the circuit a quick recalibration would need to occur. This could be done with a battery, a potentiometer, and a handheld multimeter.

#### OVERALL RESULTS

The project is a success. It meets all specifications and the error tolerance was lower than expected. The non-linearity of the circuit and the calibration issue are the other two things that were unforeseen, but they are not issues that will affect the results of the measurements more than is tolerable.

## CHAPTER 5

### COST

Design Team 5 was able to stay within the five-hundred dollar budget given by the College of Engineering. Most of the parts were provided by the ECE shop, as well as the PCB fabrications. Also thanks to the Cyclotron shop which donated a 12 V single power supply and Amp pin connectors. Very few parts were ordered from other vendors. The final cost was very close to the budget with the exception of the PCB fabrication. Table 6 below shows a detailed cost breakdown of the final product.

| Final Project Cost    |              |                       |
|-----------------------|--------------|-----------------------|
| Items                 | Quantity     | Total Cost            |
| LM324 (sockets)       | 2            | Free (ECE Shop)       |
| LM555 (sockets)       | 1            | Free (ECE Shop)       |
| LM339 (sockets)       | 2            | Free (ECE Shop)       |
| OPA140 (adapter)      | 4            | \$48                  |
| Resistors             | 17           | Free (ECE Shop)       |
| Capacitors            | 7            | Free (ECE Shop)       |
| Diodes                | 2            | Free (ECE Shop)       |
| Potentiometers        | 4            | Free (ECE Shop)       |
| Precision resistors   | 4            | \$2                   |
| Power supply          | 1            | Free (Cyclotron Shop) |
| Amp pin               | 20           | Free (Cyclotron Shop) |
| Amp pin connectors    | 8            | Free (Cyclotron Shop) |
| Twisted cable (500ft) | 1            | \$12                  |
| Project box           | 2            | \$13                  |
| Insulate Stand        | 2            | \$7                   |
|                       | <b>Total</b> | <b>\$82</b>           |

TABLE 6

## SCHEDULE

Over all, Design Team 5 successfully stayed on the schedule from the Gantt chart which was created at the beginning of the semester. The only extension time was power source for the project. It took some time to decide on single supply or dual supply because it changed the op-amp that was able to be used for the project. After the designing and testing, the final fabrication and packaging of the project only took a few days. This allowed more time for final testing and calibration. At last, Design Team 5 finished the project earlier than the schedule on the Gantt chart.

## SUMMARY

ArcelorMittal has asked ECE480 Design Team 5 to create a new, reliable and robust system of electrical load signal transmission, specifically for the company's hot rolling plant, which is used for monitoring the total facility electrical load in the control room about a half mile away. The new system must begin with using the existing 0 to 100 mV analog signal from the load transducers at the plant, specifically within the 138kV switchyard, and end with a 1 to 5 V and 4 to 20 mA signal at the PLC, in the Central Dispatch control room.

The transmission system of the project was decided to use Pulse Width Modulation (PWM). The use of PWM as a means of telemetry of the transducer voltages has several favorable attributes in comparison to the other design concepts. Consideration of the project's overall cost and feasibility were especially weighted in its support. The technology inherent to PWM transmission and similar modulation schemes is that it has very high noise immunity. This characteristic also makes PWM desirable in that if the transducer input were simply amplified along the transmission line, any noise along the channel would also be amplified and sent to the receiver. By encoding the input as a small signal, the original amplitude becomes proportional to the duty cycle. The transmission of the input to the output does not require any synchronization between the transmitter and receiver.

For the design of the project, it contains two parts: transmitter and receiver. It is designed to use a twisted shielded pair cable with overall shielding for transmitting the analog signal. Each portion of the circuit is powered with 12 V supply. In the transmitter circuit, a free-running sawtooth generator is used for generating a pulse-width modulated carrier signal to transmit the information through transmission line. The twisted transmission line with shielding helps preclude any obstructive EMI. The line has inherent resistive, capacitive and inductive components per unit length of the line which are factors in the final design. In the receiver, low-pass filtering removed the higher frequency component of the carrier signal, and leaves a low frequency direct current from the transmission line. At last, the 1 to 5 VDC output will be utilized by the PLC.

## CONCLUSION

Pulse Width Modulation transmission system met the critical project specifications and was considered a success. The system is fully functional. With 500ft range, the system can transmit the continuous 2 to 4 V output signal while varying the input signal between 0 to 100 mV. To achieve the most accuracy in any environment condition, the system is designed with potentiometers on the PCB for calibrating the output signal. The tested results achieved high precision accuracy. The average error is less than 0.25% and the highest error is still less than 1%. The system is working correctly. Design Team 5 followed the schedule with only a very small budget to achieve the goal.

For future work, future design teams can develop the system even more to get more accurate final results. Design Team 5 suggests:

- 1) Using high precision resistors and potentiometers to achieve a more precise output.
- 2)
- 3) Using better twisted cable such as shielded foiled twisted pair cable for increased protection against outside electrical signals and physical effects.
- 4) Developing a more noise and vibration resistant enclosure for better protection against any interference or mechanical agitation.
- 5) Improving the system by attaching a digital voltage meter on each side of the transmission line giving the option of locally monitoring the input and output of the circuit.

## APPENDIX 1 – TECHNICAL ROLES, RESPONSIBILITIES, WORK ACCOMPLISHED

### Alex Gollin - Document Prep

Alex's technical role in the project can be split into three sections. The three sections are the testing and development phase. The second portion is the actual building and testing phase. The final part of the project is the final considerations and final testing of the circuits. At the beginning of the project he helped to perform some initial P-SPICE simulations that would kick the project off. Using Belden cable specifications, he was able to simulate a pulse signal over a transmission line to see if the signal would distort in any way. This helped to narrow down the frequency band that the project could operate at. He also helped in developing the low pass filter idea that was used in the receiver. The second portion of the project was during the building and testing of prototypes phase. He worked on the theoretical design ideas and proposed changes to the design, including simplifying the sawtooth waveform generator working with a non-inverting summing amplifier to adjust the input waveform with a gain as well as a DC offset. Shifting of the input waveform was an important part of the design because the circuit can be calibrated to give a different output range. The third part of the design process was the building and testing portion. He worked on designing and building the final enclosure using the engineering shop. He worked on testing the final project and developed criteria for comparing the data. This data was then used to plot the results verse the expected results and then develop a calibration method for the circuit. Alex then performed three final tests that would give the data that was needed to show the success of the project.



### Cheng - Team Manager

Cheng's technical tasks included initial design research, design implementation including PCB layout, PCB fabrication and design testing and casing. Cheng initially worked with the team and came up with several conceptual designs. His major contributions to the conceptual designs were the optical fiber and Ethernet I/O. Cheng also cooperate with other members and used solution selection method to choose the intend solution. During the design phase of the project, Cheng participated in the circuit building and testing. He together with the other members built and tested the circuit on the protoboard. He was also involved in the troubleshooting and refining phase of the design. He communicated with other team members and the sponsor, discussing and determining the design specification and design parameters. Cheng's major contribution to the team level outcome was the implementation of the circuit design to PCB layout. Due to the fact that both time and budget of the project is limited, Cheng insisted to have the PCBs fabricated by the ECE shop. To accomplish that, he used Eagle as the CAD tool to design the PCB layout. He designed the PCB as a single layer so that could be made by the ECE shop. His PCB design includes two printed circuit boards. One of the PCB is the entire circuit for the transmitter and the other PCB is the entire circuit for the receiver. Due to the limitation of the maximum size and single layer of the PCB, Cheng did several unique routings so that the circuit would fit on the relatively small boards. Cheng was also involved in the soldering and troubleshooting of the fabricated PCBs. During the final testing of the project, Cheng contributed in designing and building the project enclosure.



## Kenneth Young - Presentation Prep

Ken's principle technical role on the design team was to create the linear ramp generator used in the pulse width modulation transmitter and the low-pass filter used in the receiver. He also worked on selecting appropriate integrated circuit chips for the project. His work on the team heavily surrounded the initial research into determining how to build the entire pulse width modulation (PWM) signal transmission circuit on a breadboard with emphasis on implementation of the ramp generator and low-pass filter.



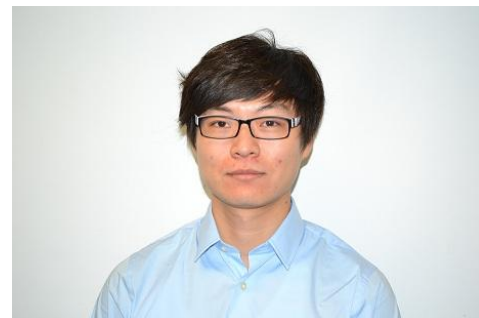
He began his research into building the PWM circuit by looking at PWM information online from academic sources and textbooks. He utilized online documents from courses at MIT, Georgia Tech, and other universities which he found had very didactic and effective information. He continued my research by using industry tools and reading a number of Texas Instruments application notes on operational amplifier and comparator specifications. Some of the tools that were used include a filter design software package called TI Filter Pro along with the AMS PSPICE Simulator.

As the circuit design progressed and the PWM circuit began to be developed on a breadboard there were numerous issues in the circuit design which were errors to the signal transmission which needed to be addressed. He continually found himself searching for solutions on Google Books and reading PDF files posted online from various universities' coursework to find solutions to these problems.

At one point during the project he had a problem finding operational amplifiers which had a high enough slew rate for our application along with fitting into numerous other specifications required for the teams design. He needed to find op amps which would fit into the required project parameters such as requirements for single supply operation, minimum operating temperature, negative rail output capability, and appropriate IC package size. To find op amps fitting the range of required specifications I used an online tool from TI to filter down nearly a thousand available op amps to about three which would fit the required optimal specifications for the designed PWM circuit.

## Nan Xia - Webmaster

Nan Xia is a senior in electrical engineering. He is the webmaster of Design Team 5. His major contribution on the initial project design is Frequency Modulation Transmission and Frequency Hopping Spread Spectrum Transmission design ideas. He helped in doing research to choose the final solution. He also participated on circuit designing and testing as well as making the protoboard design. He was focused on the hardware design and final test of the project. He contributed on the PCB layouts using Eagle software, assembling two final PCBs and package them, and debugging errors found during fabrication. He helped decide on the enclosure and the necessary modifications for best applying adjustment. For the final product testing, he helped to collect all the testing data and plot it against the input to compare with the theoretical data. He analyzed the multiple testing result percentage errors by precisely adjusting the offset voltage and gain. The error was minimized and the final results were achieved. He was also involved in the project design and discussion.



#### Patrick Powers - Lab Coordinator

Patrick contributed throughout the design development by performing the necessary modeling of components and running simulations using PSPICE. He was able to develop a complete working simulation of the entire demodulation circuit. His primary design interest focused on the receiving end of the circuit. He provided assistance in optimizing the demodulation of the PWM signal, and provided insight into the lowpass filter development. On the transmitting side, he helped to correct conceptual errors in the comparator circuit. Throughout the entire process, he explored several design approaches for parts minimization as a function of reducing cost. Patrick closely monitored the factors related to noise or distortion within the circuit, to provide improved resiliency.



He fulfilled his role as the lab coordinator to ensure timely ordering of parts within the specifications as well as procuring donations from the Cyclotron laboratory. His prior technician skills were beneficial in the fabrication and assembly of various layers of construction. He provided a significant contribution into soldering of sensitive components and construction of the enclosures and connectors. He also provided administrative support

Patrick assisted in ensuring thorough and proper testing of the prototype was performed. He assisted in collecting the raw data, as well as providing the post-testing analysis.

## APPENDIX 2 - LITERATURE AND WEBSITE REFERENCES

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- [6] Christopher C. Davis. *FIBER OPTIC TECHNOLOGY AND ITS ROLE IN THE INFORMATION REVOLUTION* [Online]. Available: <http://www.ece.umd.edu/~davis/optfib.html>
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- [8] Bill Fowler, "Transmission Line Characteristics," *National Semiconductor - Application Note 108*, pp. 1-7, 1986.
- [9] Karki, James. "Analysis of the Sallen-Key Architecture," Texas Instruments Application Report, July 1999 (Revised September 2002).

APPENDIX 3 - DETAILED TECHNICAL ATTACHMENTS

HOUSE OF QUALITY

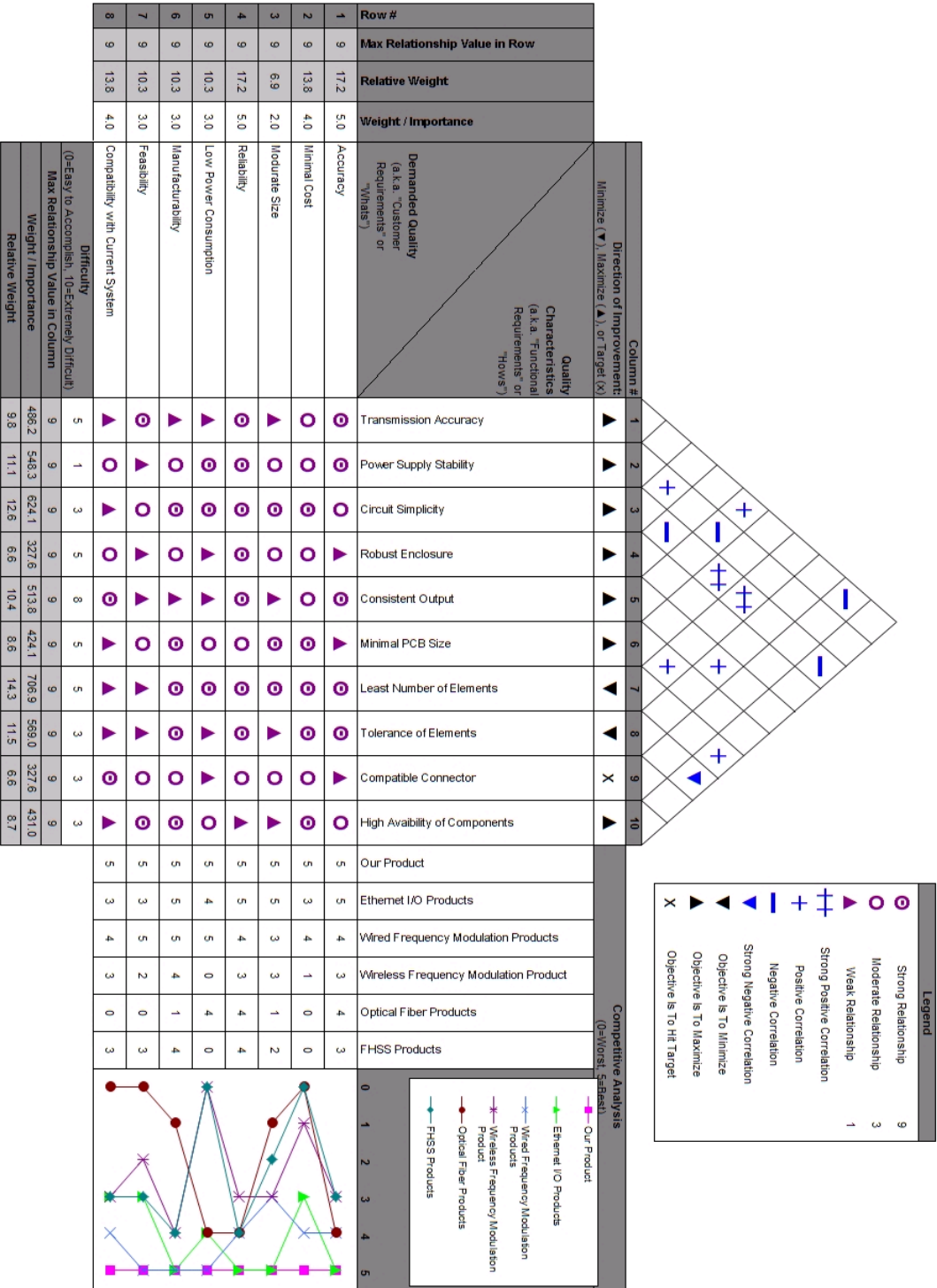


FIGURE 42

# GANTT CHART

| ID                                                                                                                                                                                                                                                                                                                                                                                                                                     | Task Mode | Task Name                                                                   | Duration       | Start               | Finish              | Prek      |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-----------------------------------------------------------------------------|----------------|---------------------|---------------------|-----------|
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                      | ✓         | Contact Sponsor - ArcelorMittal Corporation                                 | 5 days         | Mon 9/10/12         | Fri 9/14/12         |           |
| 2                                                                                                                                                                                                                                                                                                                                                                                                                                      | ✓         | Conference call with sponsor                                                | 1 day          | Mon 9/17/12         | Mon 9/17/12         |           |
| 3                                                                                                                                                                                                                                                                                                                                                                                                                                      | ✓         | Finding questions about the project                                         | 4 days         | Tue 9/18/12         | Fri 9/21/12         | 2         |
| 4                                                                                                                                                                                                                                                                                                                                                                                                                                      | ✓         | <b>Project objective</b>                                                    | <b>10 days</b> | <b>Mon 9/17/12</b>  | <b>Fri 9/28/12</b>  | <b>1</b>  |
| 5                                                                                                                                                                                                                                                                                                                                                                                                                                      | ✓         | First meeting with facilitator                                              | 1 day          | Mon 9/17/12         | Mon 9/17/12         | 1         |
| 6                                                                                                                                                                                                                                                                                                                                                                                                                                      | ✓         | Perparing for the tour                                                      | 3 days         | Tue 9/18/12         | Thu 9/20/12         | 5         |
| 7                                                                                                                                                                                                                                                                                                                                                                                                                                      | ✓         | Tour to the ArcelorMittal Corporation plant in Burns Harbor                 | 1 day          | Fri 9/21/12         | Fri 9/21/12         | 6         |
| 8                                                                                                                                                                                                                                                                                                                                                                                                                                      | ✓         | Researching conceptual design and defining proposed solution                | 5 days         | Mon 9/24/12         | Fri 9/28/12         | 7         |
| 9                                                                                                                                                                                                                                                                                                                                                                                                                                      | ✓         | Writing first draft of proposal and making slides for proposal presentation | 9 days         | Mon 9/24/12         | Thu 10/4/12         | 7         |
| 10                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Revising proposal                                                           | 6 days         | Fri 10/5/12         | Fri 10/12/12        | 9         |
| 11                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Delivery of final proposal                                                  | 0 days         | Fri 10/12/12        | Fri 10/12/12        | 10        |
| 12                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | <b>Making prototype</b>                                                     | <b>15 days</b> | <b>Mon 10/1/12</b>  | <b>Fri 10/19/12</b> | <b>4</b>  |
| 13                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Circuit design of modulator                                                 | 10 days        | Mon 10/1/12         | Fri 10/12/12        | 4         |
| 14                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Circuit design of demodulator                                               | 10 days        | Mon 10/1/12         | Fri 10/12/12        | 4         |
| 15                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Demodulator circuit building on protoboard                                  | 5 days         | Mon 10/15/12        | Fri 10/19/12        | 14        |
| 16                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Modulator circuit building on protoboard                                    | 5 days         | Mon 10/15/12        | Fri 10/19/12        | 13        |
| 17                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Preparing technical lecture                                                 | 9 days         | Mon 10/29/12        | Thu 11/8/12         |           |
| 18                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | <b>PCB fabrication</b>                                                      | <b>21 days</b> | <b>Mon 10/15/12</b> | <b>Mon 11/12/12</b> | <b>13</b> |
| 19                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Refining modulator circuit                                                  | 3 days         | Mon 10/15/12        | Wed 10/17/12        | 13        |
| 20                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Refining demodulator circuit                                                | 3 days         | Thu 10/18/12        | Mon 10/22/12        | 19        |
| 21                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Designing PCB layout for both circuit                                       | 5 days         | Tue 10/23/12        | Mon 10/29/12        | 20        |
| 22                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Fabrication by ECE shop                                                     | 2 days         | Tue 10/30/12        | Wed 10/31/12        | 21        |
| 23                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Soldering electronic components                                             | 3 days         | Thu 11/1/12         | Mon 11/5/12         | 22        |
| 24                                                                                                                                                                                                                                                                                                                                                                                                                                     | ✓         | Testing PCBs                                                                | 5 days         | Tue 11/6/12         | Mon 11/12/12        | 23        |
| <div> <div>Task</div> <div>Split</div> <div>Milestone</div> <div>Project Summary</div> <div>External Tasks</div> </div> <div> <div>External Milestone</div> <div>Inactive Task</div> <div>Inactive Milestone</div> <div>Manual Task</div> <div>Duration-only</div> </div> <div> <div>Manual Summary Rollup</div> <div>Manual Summary</div> <div>Start-only</div> <div>Finish-only</div> <div>Deadline</div> <div>Progress</div> </div> |           |                                                                             |                |                     |                     |           |

| ID | Task Mode                                                                             | Task Name                                  | Duration      | Start               | Finish                 | Precedence |
|----|---------------------------------------------------------------------------------------|--------------------------------------------|---------------|---------------------|------------------------|------------|
| 25 |    | <b>Testing and casing</b>                  | <b>7 days</b> | <b>Tue 11/13/12</b> | <b>Wed 11/21/12 18</b> |            |
| 26 |    | Testing entire project                     | 2 days        | Tue 11/13/12        | Wed 11/14/12 18        |            |
| 27 |    | Designing enclosures                       | 3 days        | Thu 11/15/12        | Mon 11/19/12 26        |            |
| 28 |    | Installing PCBs                            | 2 days        | Tue 11/20/12        | Wed 11/21/12 27        |            |
| 29 |    | Thanksgiving holiday                       | 2 days        | Thu 11/22/12        | Fri 11/23/12           | 28         |
| 30 |    | <b>Final preparation of the Design Day</b> | <b>9 days</b> | <b>Mon 11/26/12</b> | <b>Thu 12/6/12</b>     | <b>29</b>  |
| 31 |   | Writing final report                       | 9 days        | Mon 11/26/12        | Thu 12/6/12            | 29         |
| 32 |  | Perparing Design Day presentation          | 4 days        | Mon 12/3/12         | Thu 12/6/12            |            |
| 33 |  | Delivery of project                        | 0 days        | Fri 12/7/12         | Fri 12/7/12            |            |

Task

Split

Milestone

Summary

Project Summary

External Tasks

External Milestone

Inactive Task

Inactive Milestone

Inactive Summary

Manual Task

Duration-only

Manual Summary Rollup

Manual Summary

Start-only

Finish-only

Deadline

Progress













Project: Project1

Date: Sun 12/2/12



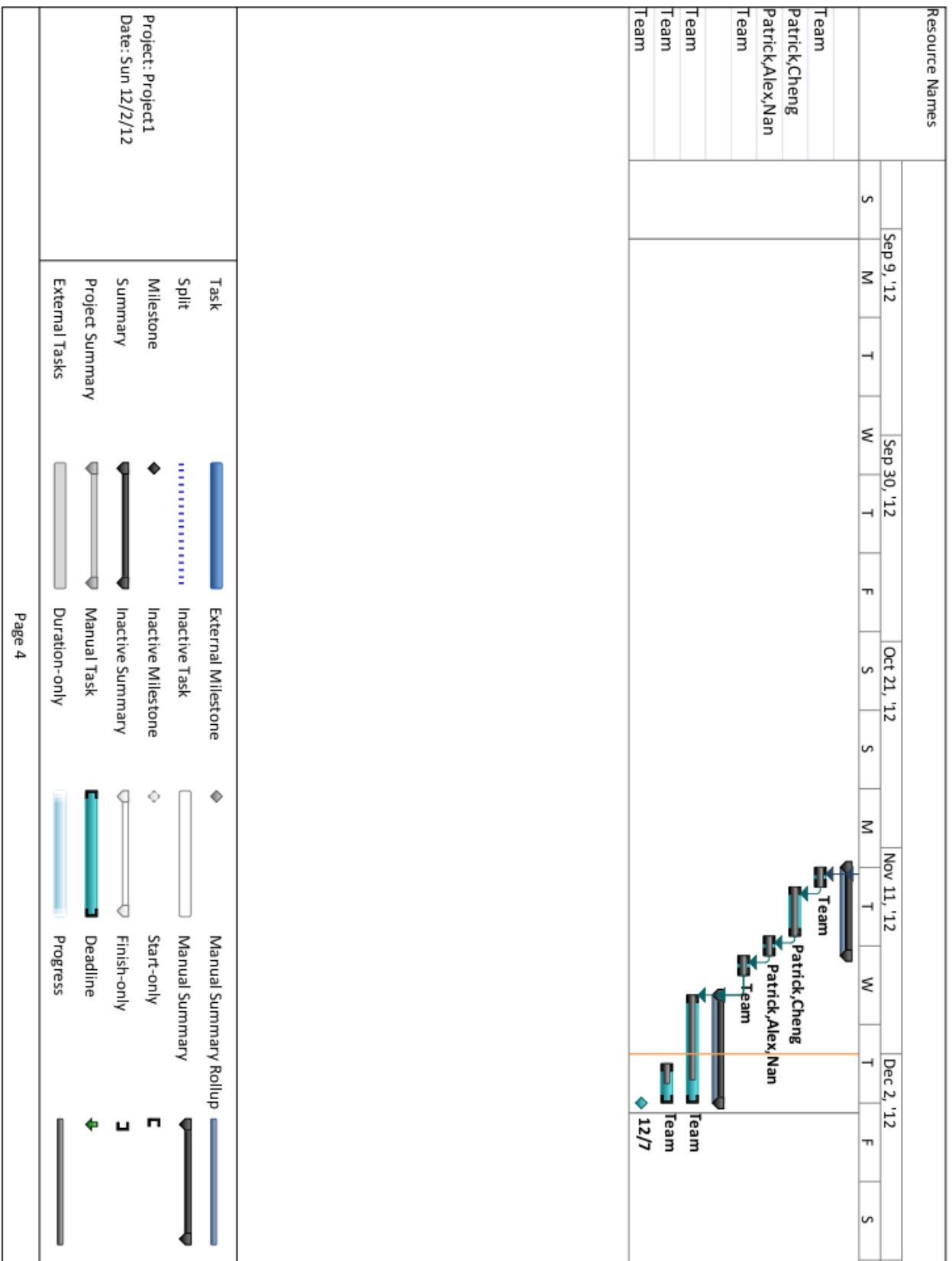


**FIGURE 43**

## Linear Ramp PSPICE Simulation

A PSPICE simulation of the linear ramp wave generator was performed using the circuit shown in Figure 47. Vpulse represents the output of the LM555 at pin three. Vpulse is a one percent duty cycle 1kHz pulse with peak of one volt. The transient response of the circuit is shown in Figure 48, the upper graph displays the voltage at node six which represents a pulse train from the LM555 output. The lower graph displays the capacitor voltage at node four is the ramp waveform.

The simulation shows that adjusting the potentiometer R3 to be 26.5K ohms results in a peak ramp voltage of 2.00 volts. The simulation also shows that the minimum voltage of the ramp waveform is 24.5mV in a 2.00 volt peak configuration. The minimum voltage of the ramp waveform does not go all the way to zero volts because of the collector to emitter saturation voltage of transistor T1. Laboratory results from testing the linear ramp generator matched closely with the predicted PSPICE simulation results with the minimum ramp wave voltage being observed to be approximately 20mV.

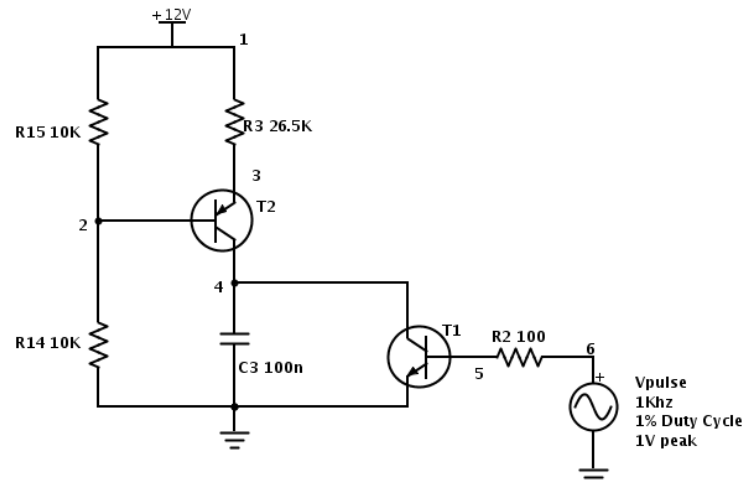


FIGURE 44

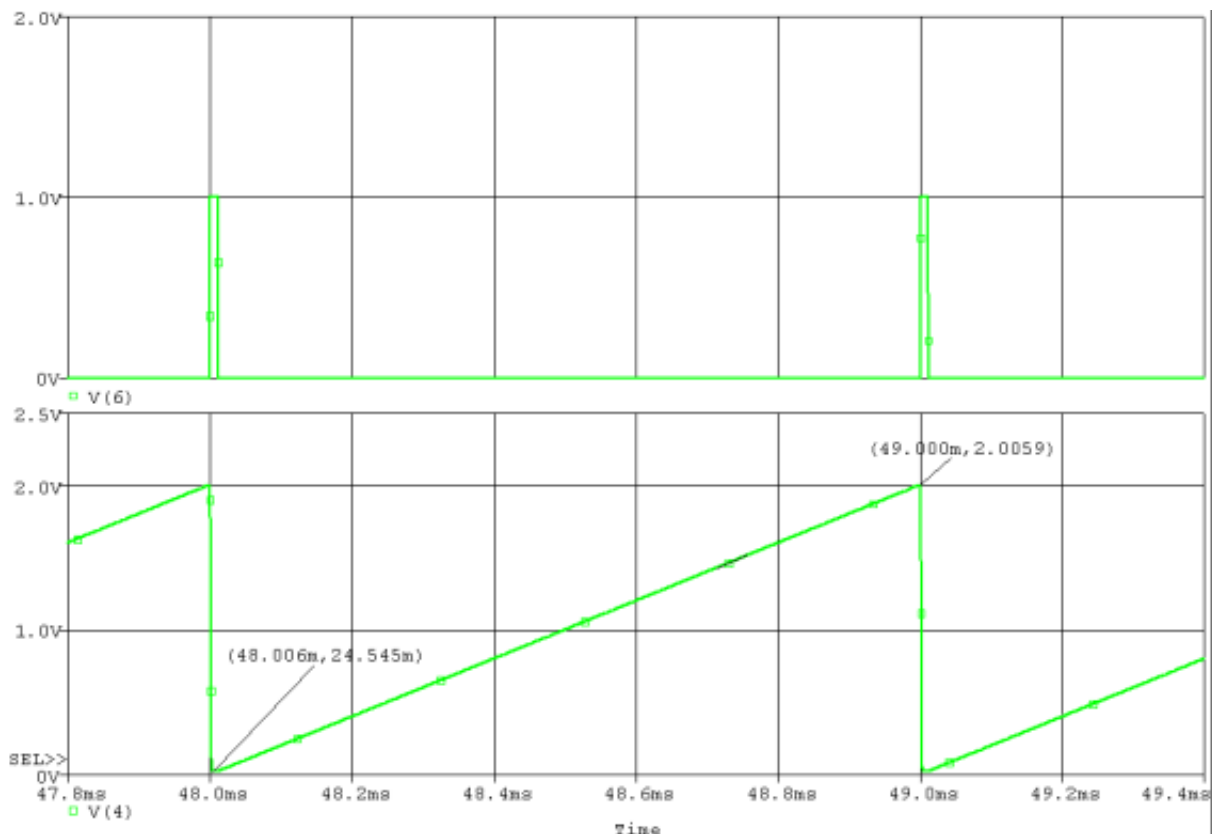


FIGURE 45

## NON-INVERTING SUMMER

A non-inverting summer is shown in Figure 51. A DC offset can be added to a waveforms simply by applying the waveform to R1 as voltage V1 and applying the DC offset voltage to R2 as voltage V2.

For a non-inverting summer with two input voltages the transfer function can be derived as follows

$$V_+ = (V_2 - V_1) \left( \frac{R1}{R1 + R2} \right) + V_1$$

$$V_- = V_{out} \left( \frac{R4}{R3 + R4} \right)$$

Since a non-inverting summer has negative feedback  $V_+ = V_-$ .

$$(V_2 - V_1) \left( \frac{R1}{R1 + R2} \right) + V_1 = V_{out} \left( \frac{R4}{R3 + R4} \right)$$

$$V_{out} = \left[ (V_2 - V_1) \left( \frac{R1}{R1 + R2} \right) + V_1 \right] \left( \frac{R3 + R4}{R4} \right)$$

$$V_{out} = \left[ V_2 \left( \frac{R1}{R1 + R2} \right) + V_1 \left( \frac{R2}{R1 + R2} \right) \right] \left( 1 + \frac{R3}{R4} \right)$$

For the non-inverting summer in Figure 51 with two inputs if  $R1=R2=R3=R4$

$$V_{out} = V_1 + V_2$$

An example of the output of a non-inverting summer with a 0 to 5v pulse signal on  $V_1$  and +2v DC on  $V_2$  can be seen in Figure 52. The output waveform will be the sum of  $V_1 + V_2$  which is a 2 to 7v pulse.

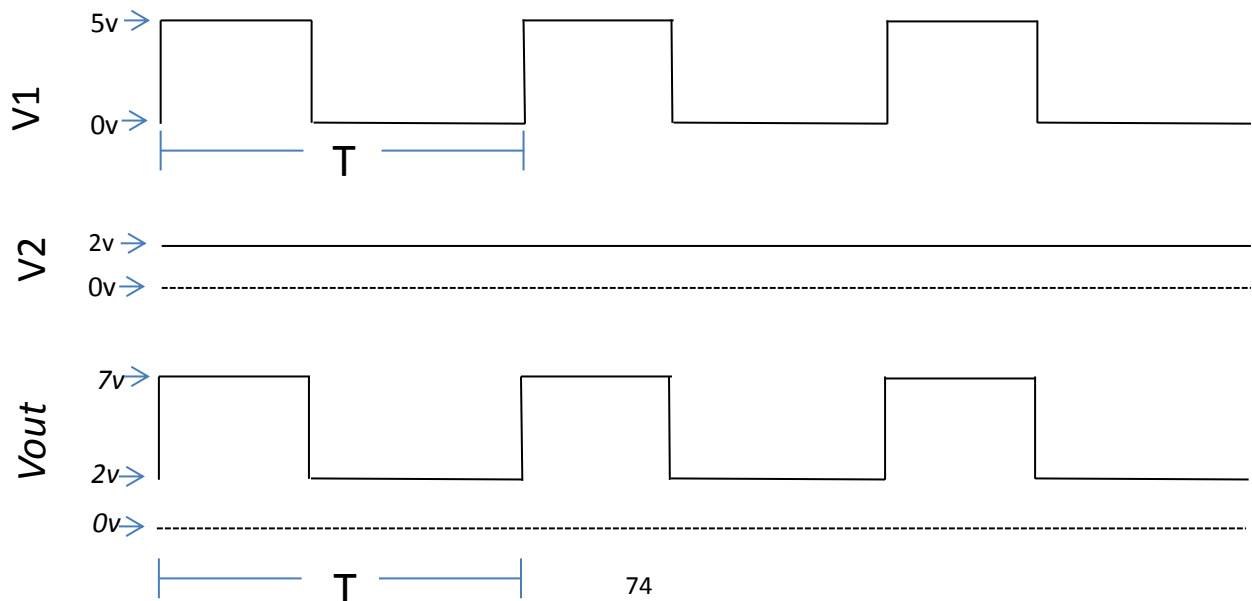


FIGURE 47

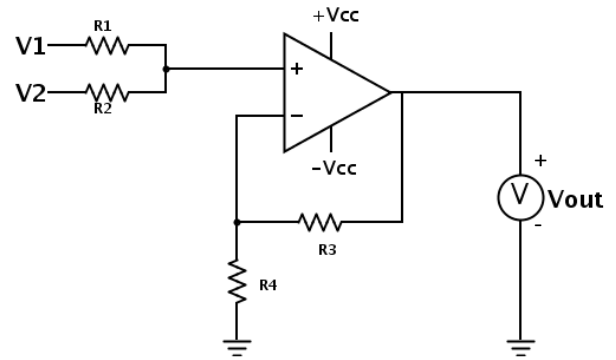


FIGURE 46

## BESSEL LOW-PASS FILTER DESIGN USING FILTER PRO™

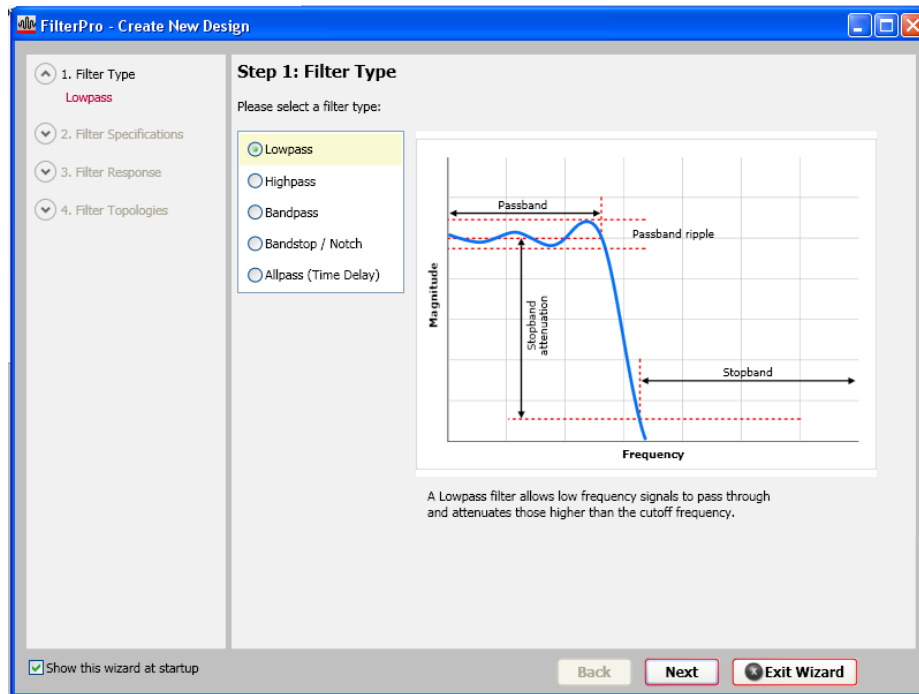


FIGURE 48

Step 1: Filter Type –“Lowpass” was chosen as required for PWM demodulation at the receiver.

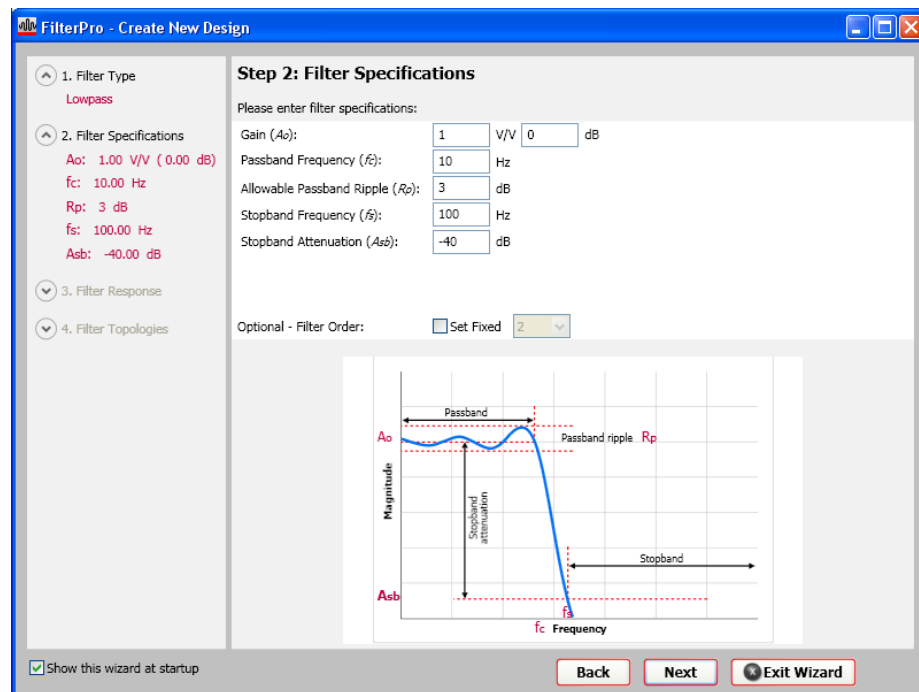


FIGURE 49

Step 2: Filter Specifications – Certain default values were available at this step. “Passband Frequency” was changed to 10 Hz to be the desired corner frequency. As with most filters that are not Butterworth filters, some ripple can be expected. “Allowable Passband Ripple” was selected to be 3 dB. At least a second-order filter was desired, therefore an approximate attenuation rate of -40 dB/decade was expected. This selection coincided with a “Stopband Attenuation” of -40 dB at the next decade beyond the 10 Hz, which was the “Stopband Frequency” of 100 Hz.

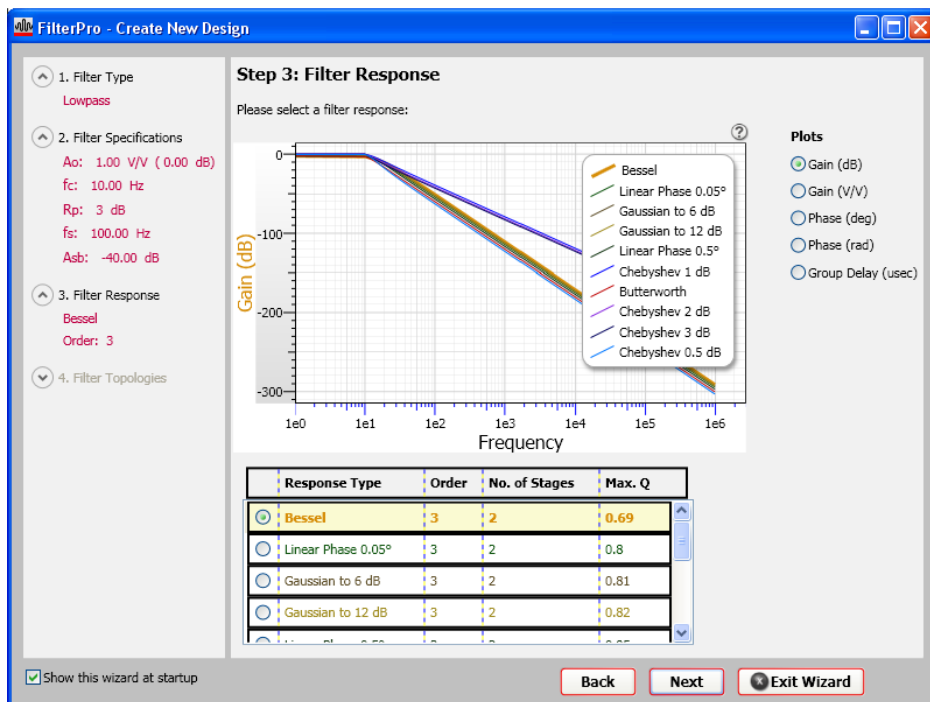


FIGURE 50

Step 3: Filter Response – A Bessel-type filter response was desired for its phase response that represented a longer group delay.

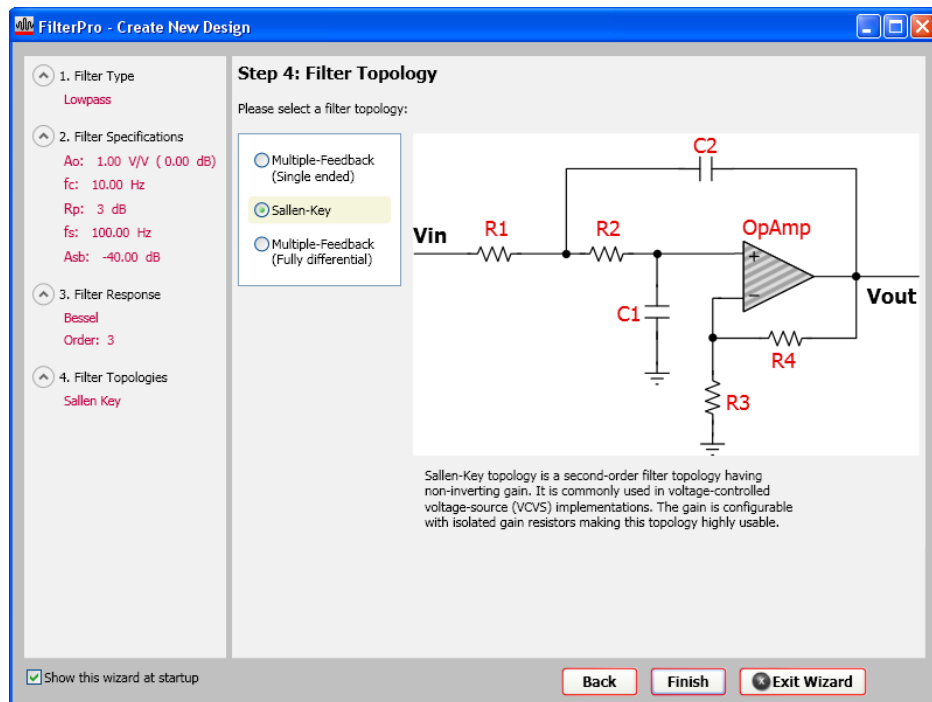


FIGURE 51

Step 4: Filter Topology – Sallen-Key utilized non-inverting gain which allows the use of single-ended power supply.

Finish: Resultant Circuit

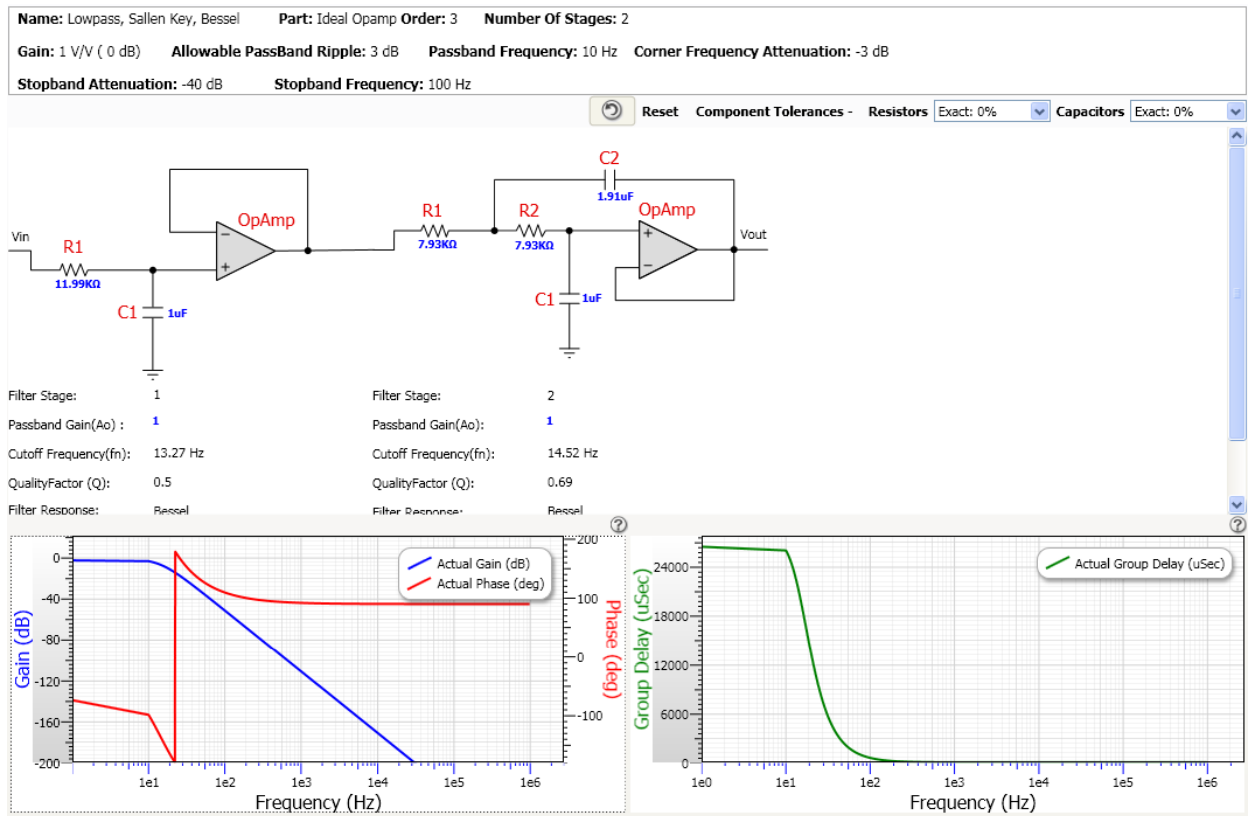


FIGURE 52

## PRINTED CIRCUIT BOARD DESIGN IN EAGLE

The printed circuit boards of the project were designed in the Eagle program by Cadsoft. To minimize the cost of the project, having the PCBs fabricated by the ECE shop was a good solution. However, the ECE shop is only capable of fabricating single layer PCBs. Moreover, the freeware of Eagle program is only capable of design 3.2in by 3.9in PCBs. To make a bigger PCB requires an additional cost of a software license. Thus it was initially decided to fabricate a total of four PCBs. However, during the design process, it was discovered that the way that the ECE shop fabricates the PCB was to drill and mechanically etch a single sided copper plate. While only the traces were etched, the rest of the copper plate was left. It was determined then the copper plate could be used as the ground plate and the ECE shop is not capable of fabricating a ground plate. That eliminates the needs for a lot of traces and the project was eventually designed to have only two PCBs, one for transmitter and the other for receiver.

The first step of design the PCB layout was to draw the schematic in Eagle program. All the elements were to be chosen during the process of drawing the circuit schematic. It was very important to choose the elements with correct type and package. The correct package of each element is even important because the program will build the PCB layout based on the package that was chosen. After the schematic is done, an error check of the circuit can be performed. In our circuit schematic there were several errors due to the fact that the output of the transmitter and the input of the receiver are transmission line which cannot be analyzed by the software. After the schematic was completed, the software could automatically transfer the schematic into a brief layout. The brief layout is not really a layout. It is a layout with all the elements on it but in very random order. At this point, an autorouting can be performed, but that turned out to be not very ideal. Thus, the arrangement and routing of the PCBs were completed by hand. The biggest trick of routing the traces was that the board can only be fabricated as a single layer PCB. That means a crossover of the traces was not acceptable. It was discovered later that because of the relatively big size of the elements the traces could cross under the elements instead of routing around.

After the PCB layout was done, a CAM process was performed according to the tutorial given by the ECE shop. Then the CAM files were sent to the ECE shop for fabrication. After the fabricated PCBs were received, the soldering would be done by the team. Due to the time and cost constrain, it was decided the project will not use surface mount elements. Using surface mount elements would have given the PCB a much smaller size. However, to use surface mount elements would mean the team needed to find a company to do the fabrication. This would cost money as well as time. It was determined that even though the size does matter the devices of the project were not going to be portable. Thus, regular size elements can be used without any problems.

To do the project with a limited time and cost, ECE shop fabricated PCBs were considered good choices. However, those fabricated PCBs don't have acceptable consistency if they were to be used made in production of the product. During the soldering process, it was discovered that several traces on the PCBs were not very well etched and there were hairline shorts between the traces and the ground plate. The flaw was fixed by mechanically clearing the traces by hand. It is recommended that the PCBs be fabricated and soldered by machine to achieve greater consistency and reliability.