

ECE480

Team 4

LabVIEW and FPGA Time Synchronization



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Topics

- Overview
- Data Acquisition Hardware
- Field Programmable Gate Arrays
- Synchronization
- LabVIEW Fundamentals
- LabVIEW Demo



Introduction

- Many systems deal with real-world signals
 - Audio
 - Video
 - Biomedical
- Require a way to capture and process them with precise timing



The Challenge

- Find a way to achieve precise sampling rates for data acquisition
- Achieve time synchronization between multiple data acquisition tasks
 - Many time-critical tasks happening simultaneously
- Concerns:
 - Hardware
 - Synchronization





Data Acquisition Hardware

- Multiple hardware solutions capable of acquiring samples
 - Microcontrollers
 - ASIC - Application specific integrated circuit
 - FPGA - Field programmable gate array



Data Acquisition Hardware

■ Microcontrollers

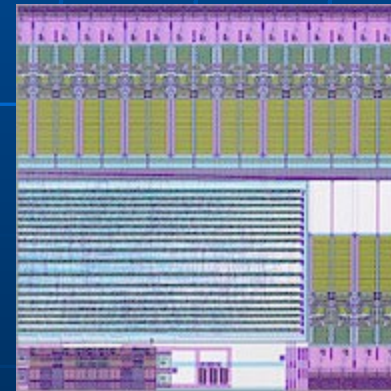
- Poor timing characteristics
- Sequential tasking not conducive to juggling multiple tasks while maintaining precise timing
 - Possible, but difficult





Data Acquisition Hardware

- Application-Specific Integrated Circuits (ASICs)
 - Tailored to the application
 - Precision timing
 - Not reconfigurable
 - Expensive

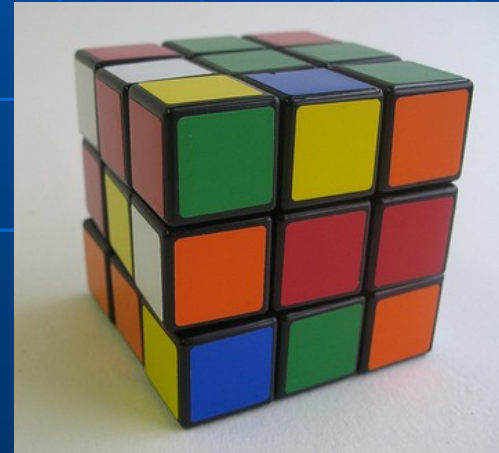




Data Acquisition Hardware

■ FPGA

- Tailored to the application
 - Precision timing
- **Reconfigurable**
- **Inexpensive**





Common FPGAs

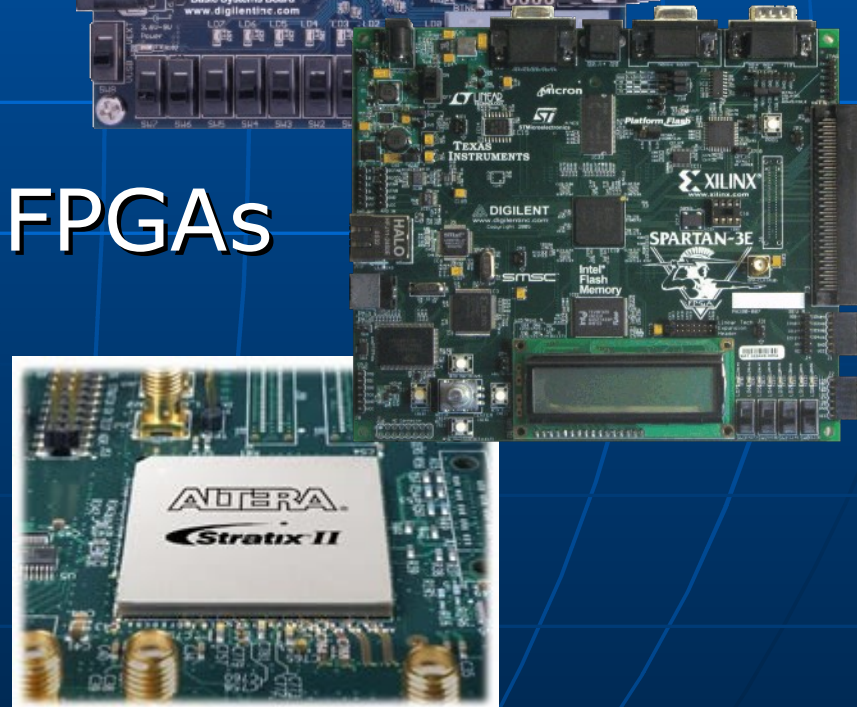
■ Low-Cost FPGAs

- Spartan-3 - Xilinx
- Cyclone - Altera
- Arria - Altera



■ High Performance FPGAs

- Virtex-4/5 - Xilinx
- Stratix - Altera





FPGA Fundamentals

■ Programmable Hardware

- Adapt quickly to design changes
- Realize a variety of hardware
- Reuse, reduce, recycle



■ Inherent parallelism

- Multiple hardware modules realized at once on the same FPGA



FPGA Programming

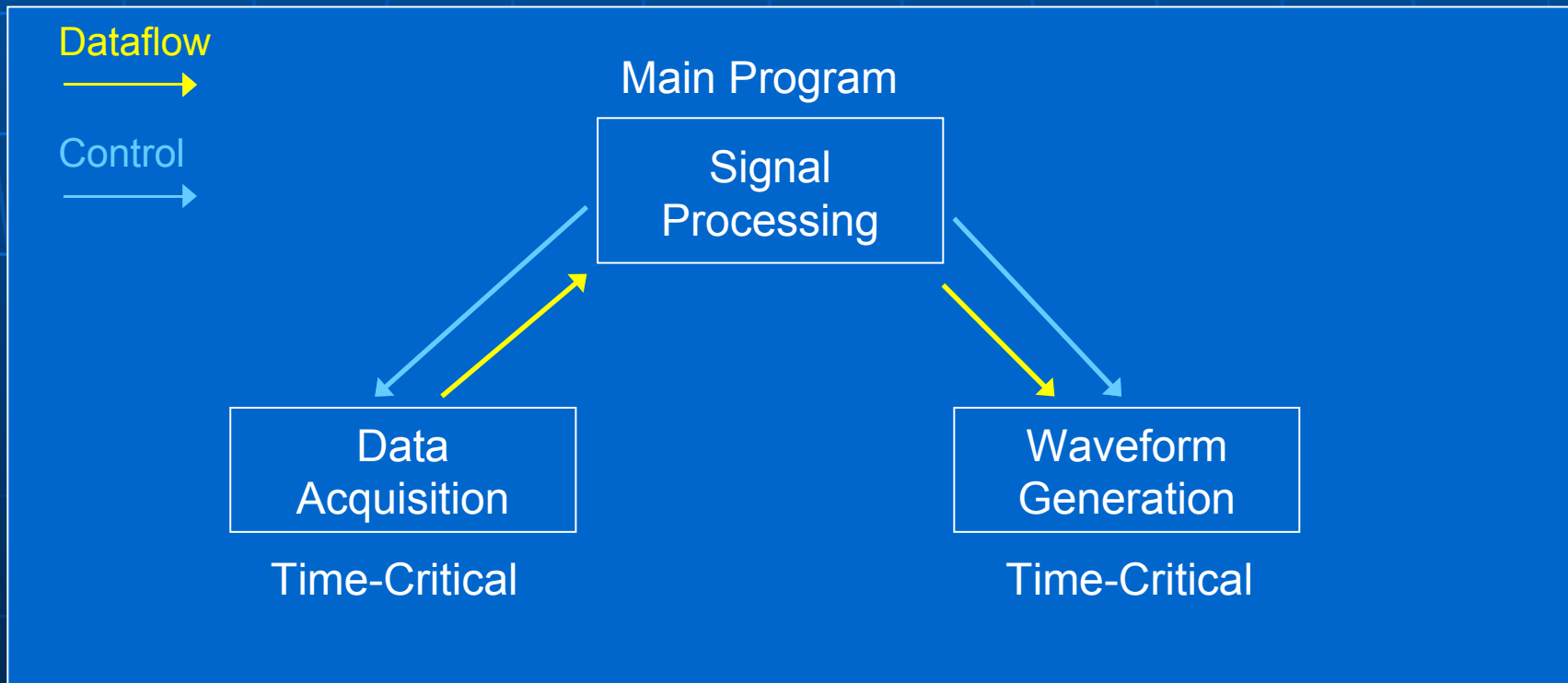
- Hardware Description Languages (HDL)
 - VHDL
 - Verilog
- Code can become complicated
- LabVIEW (Alternative)
 - Modular design





Synchronization

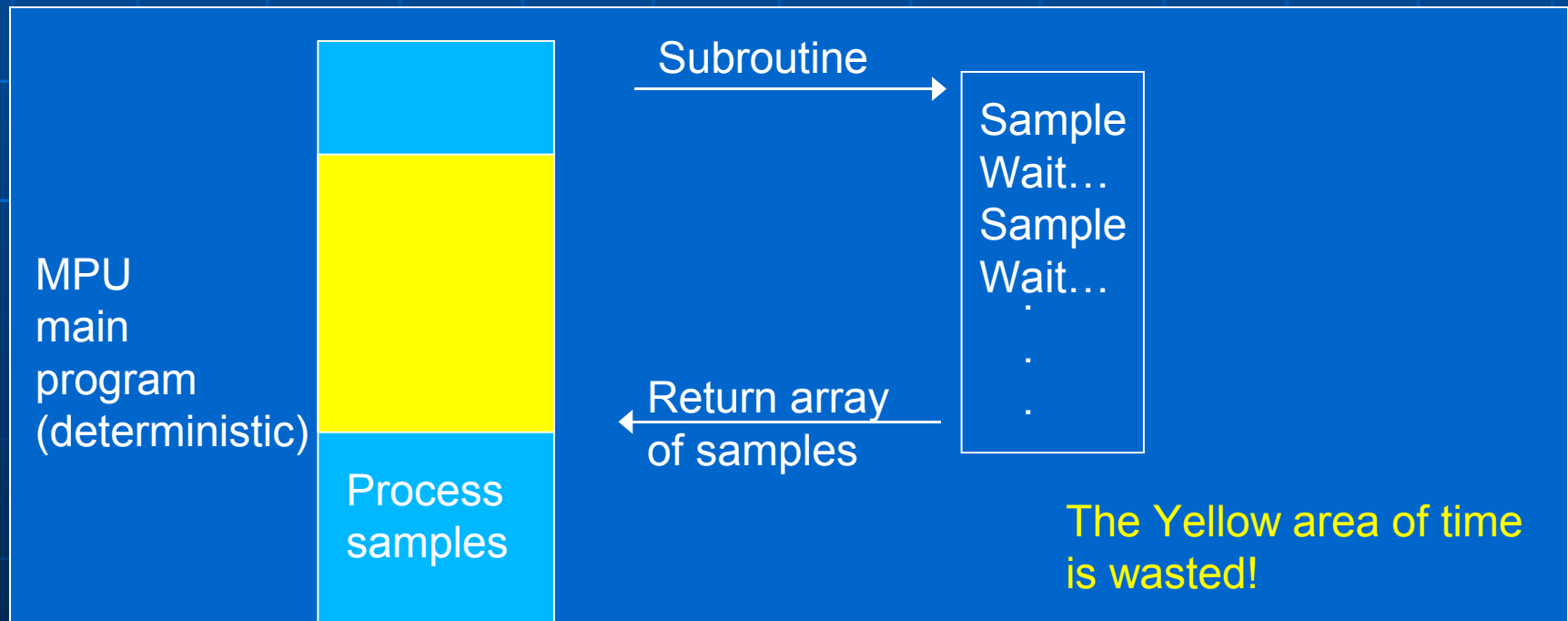
- Two time-critical tasks (signal acquisition/generation)
- One less time-critical task (signal processing)
 - We have in effect three "processes"





Synchronization

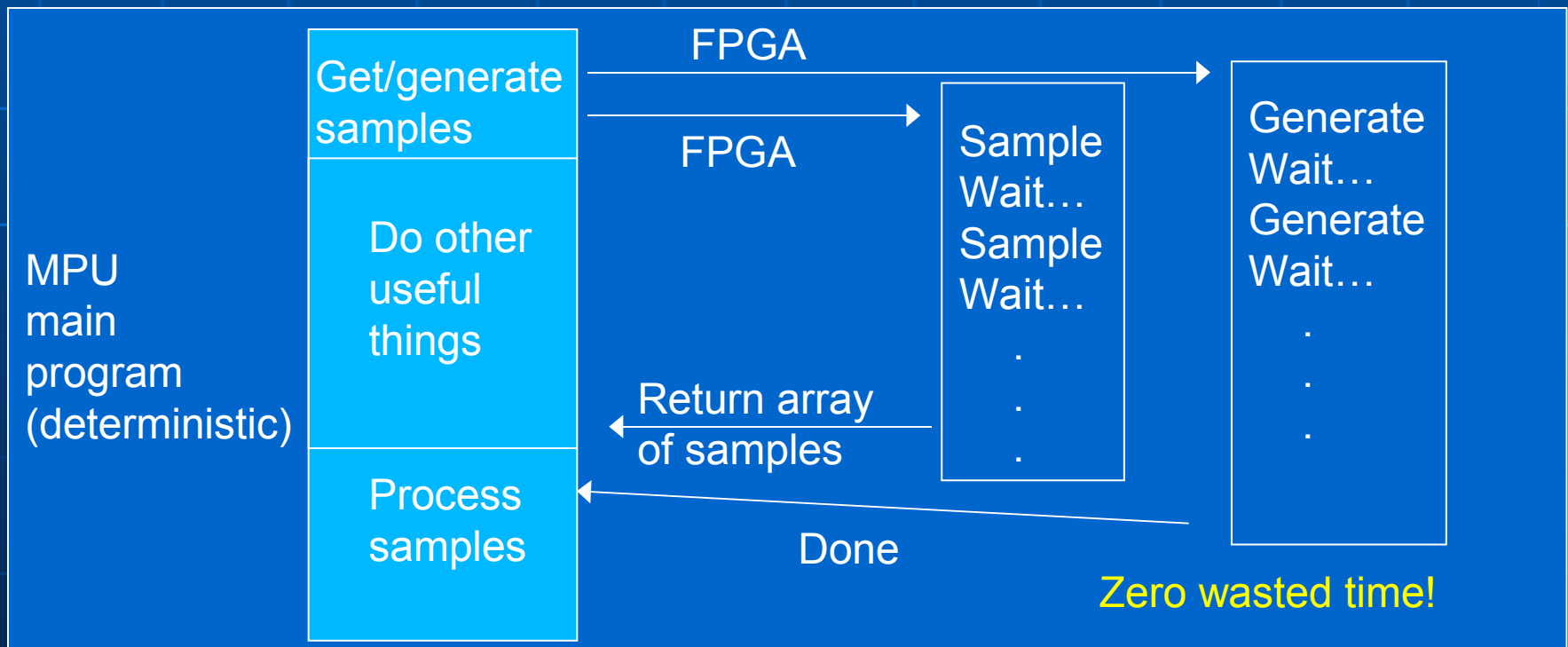
- Need precise timing (for signal acquisition & generation)
- MPU: Can only do one (precisely timed) thing at a time!





Synchronization

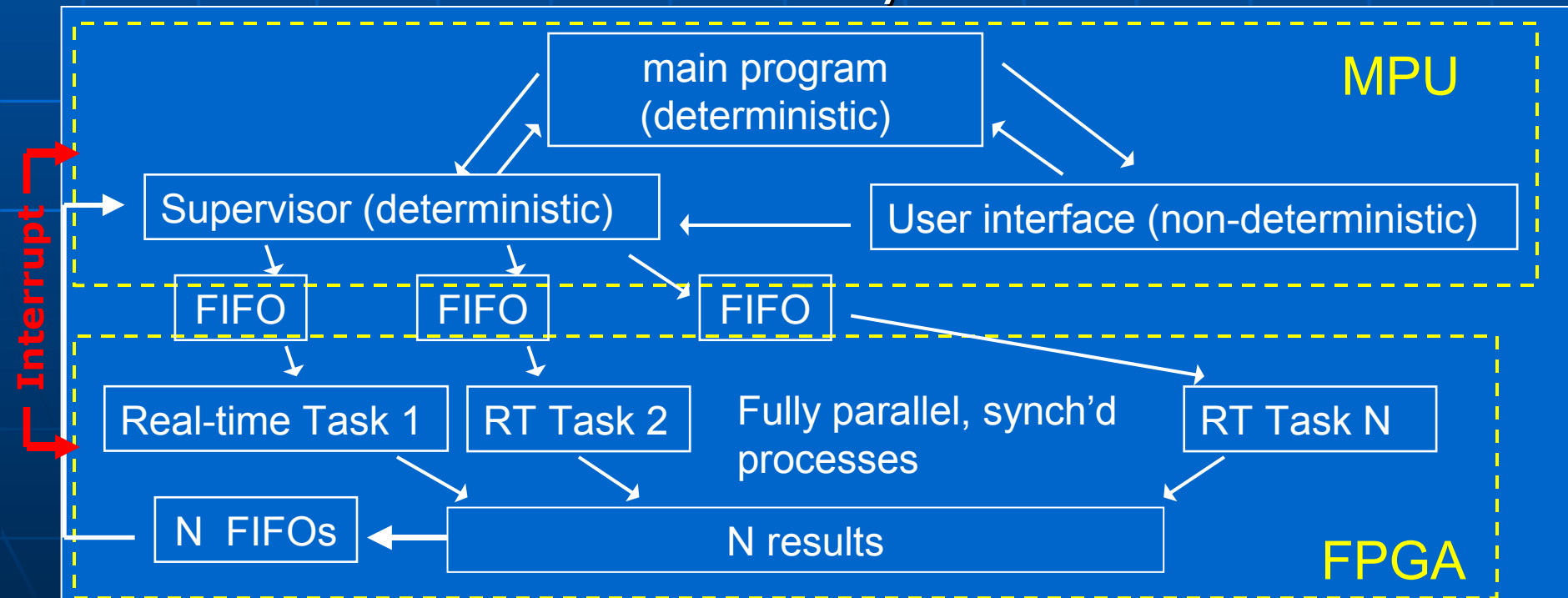
- Need hardware to perform precision tasks under the direction of a third, master process
- MPU can perform other actions while waiting for paralleled tasks





Synchronization

- Shared FIFO, First In First Out, memory buffers are used to transfer data between the two processes
- Interrupts are used to enforce mutually exclusive access to the FIFO memory





LabVIEW Fundamentals

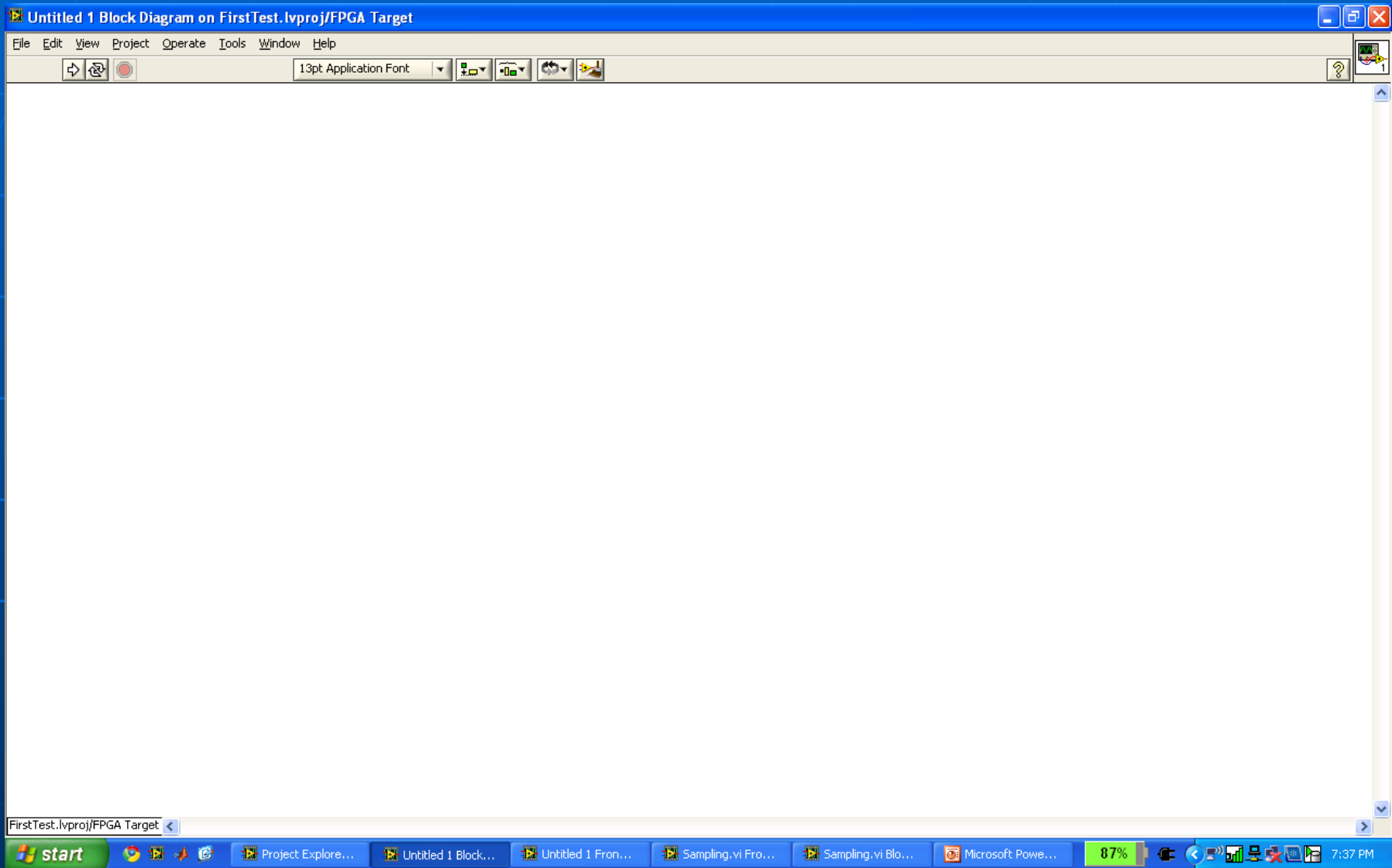
- Popular development environment for rapid prototyping
- Graphical programming language
 - Development conducted through functional “blocks”
- Designed to work with a wide variety of data acquisition devices

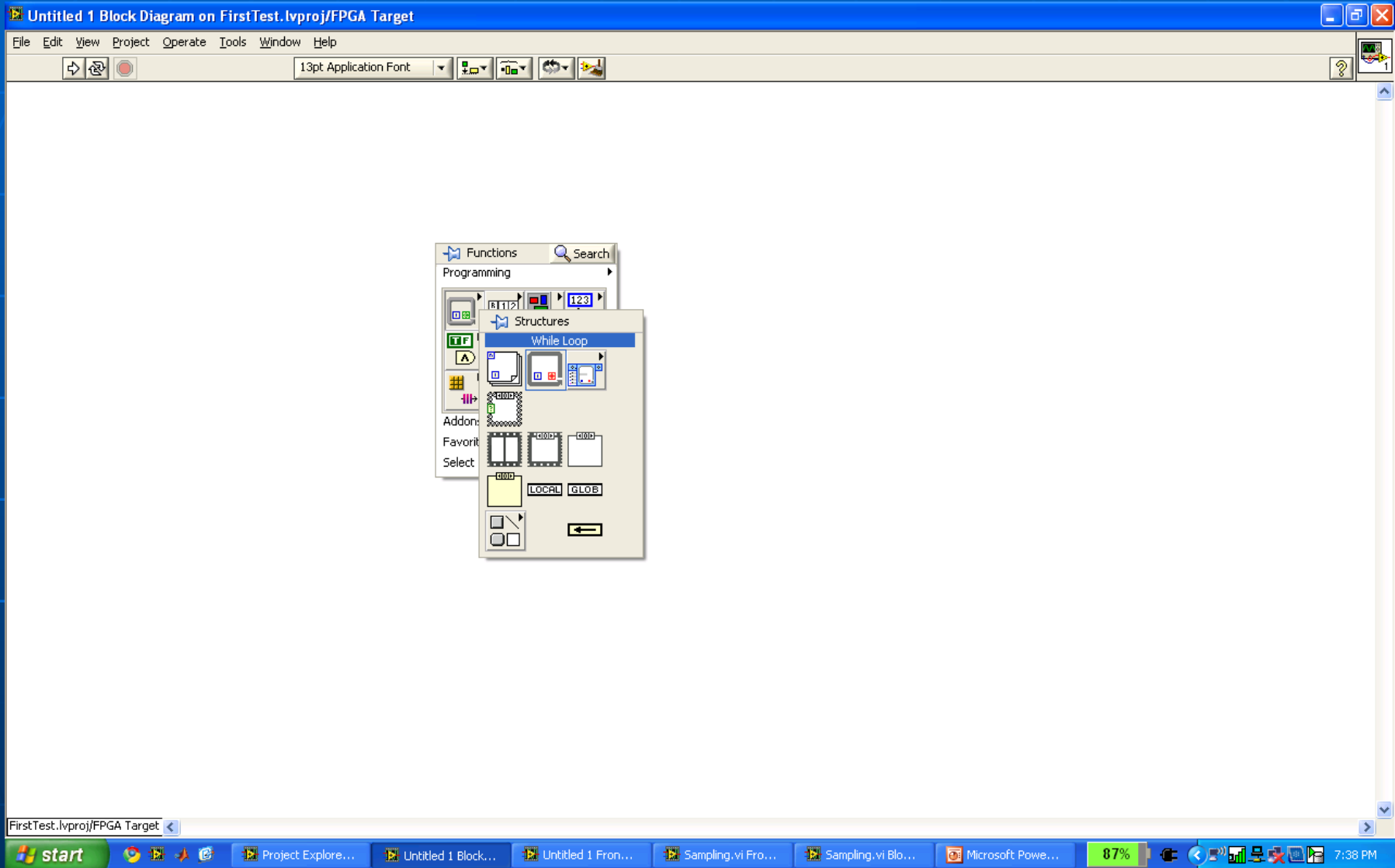


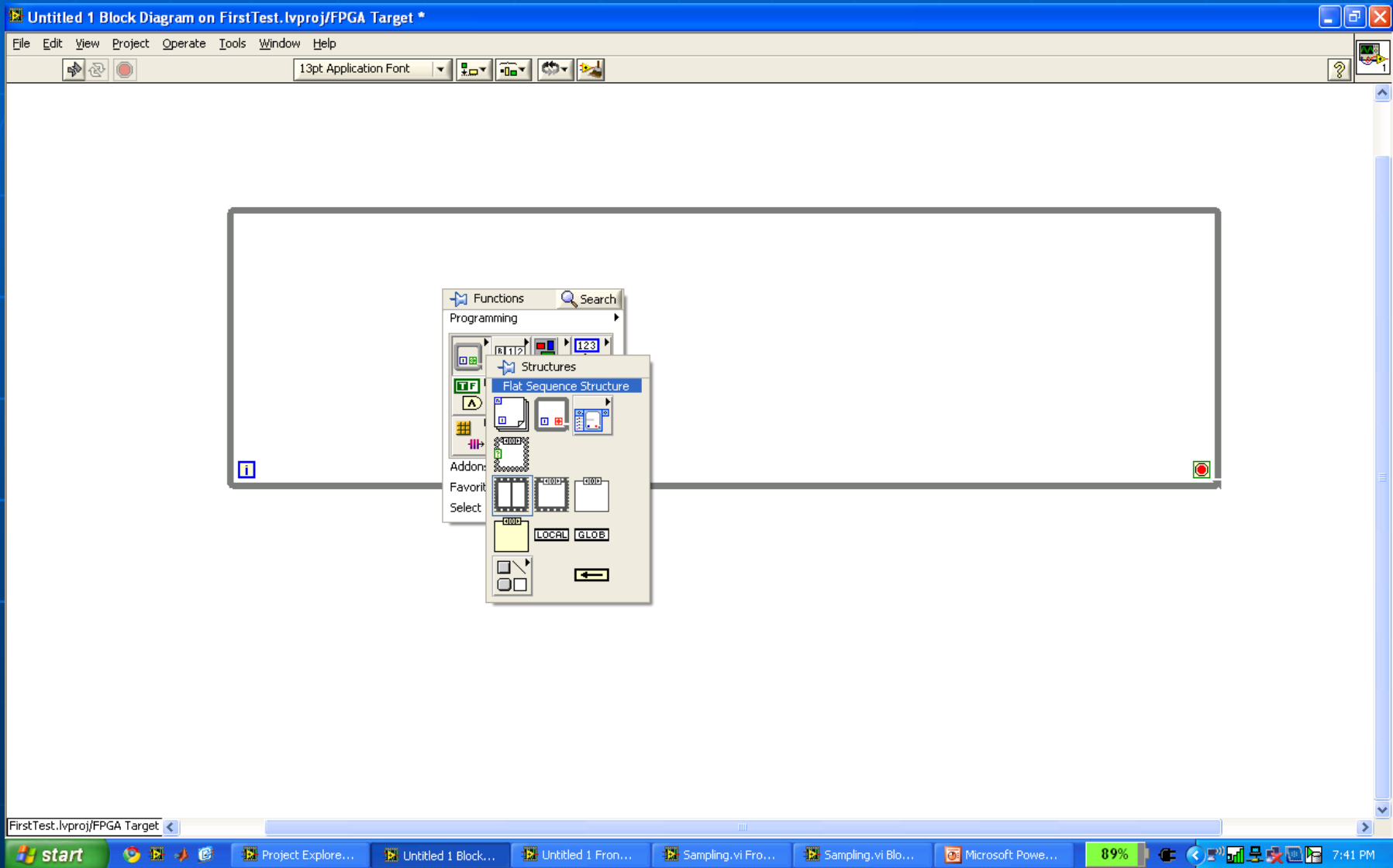
LabVIEW and FPGAs

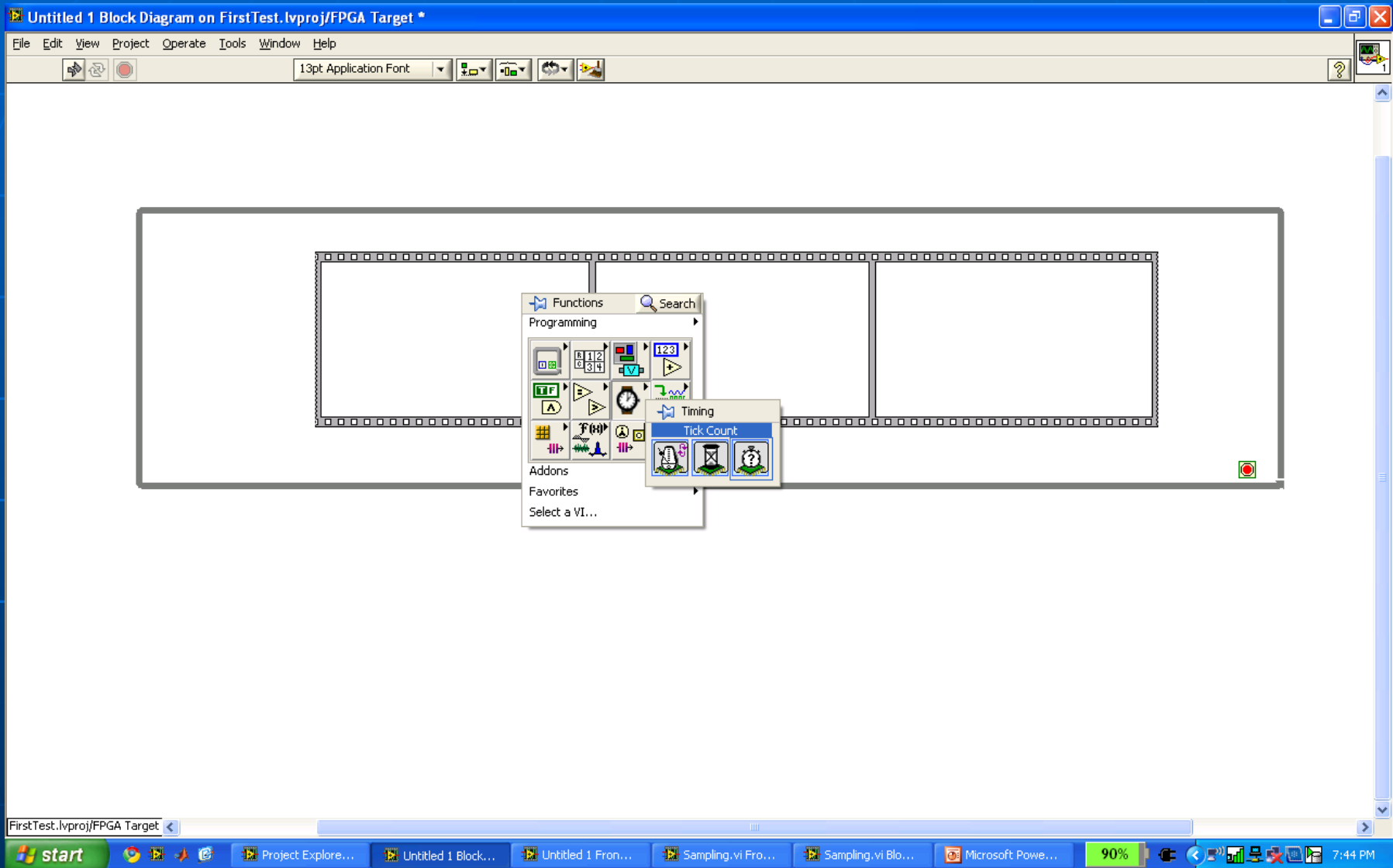
- LabVIEW determines FPGA gate utilization
 - Which portions of code can operate as concurrent hardware
- Provides a variety of software modules used to interface with FPGAs

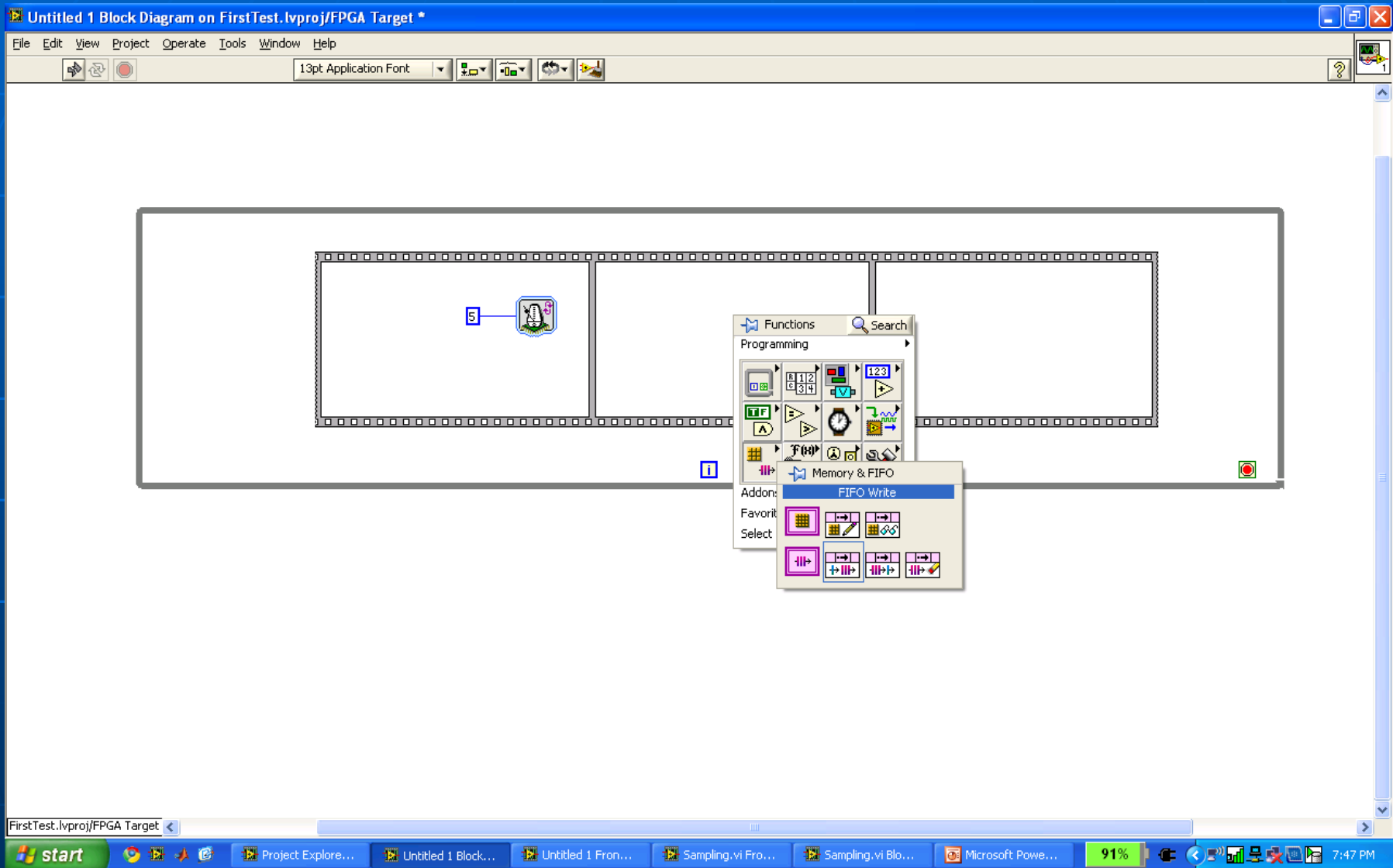
LabVIEW Demo









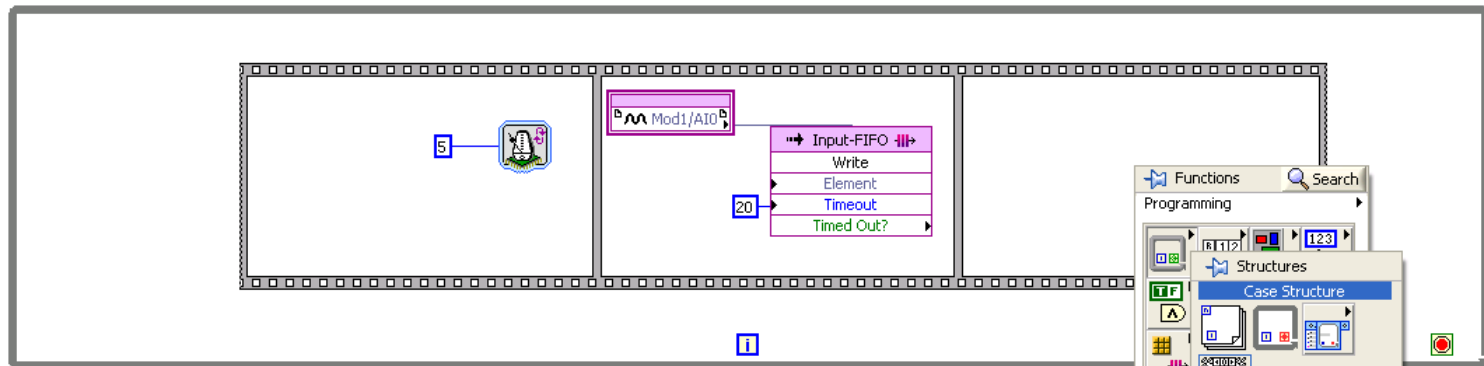


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Functions Search

Programming

Structures

Case Structure

LOCAL GLOB

FirstTest.lvproj/FPGA Target

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Mod1/AIO

Input-FIFO
Write
Element
Timeout
Timed Out?

20

True

Functions

Search

Programming

Addons

Favorites

Select a VI...

Synchronization

Interrupt

IRQ

FirstTest.lvproj/FPGA Target

start



5 LabVIEW 8.6 Dev...

Microsoft PowerPoint ...

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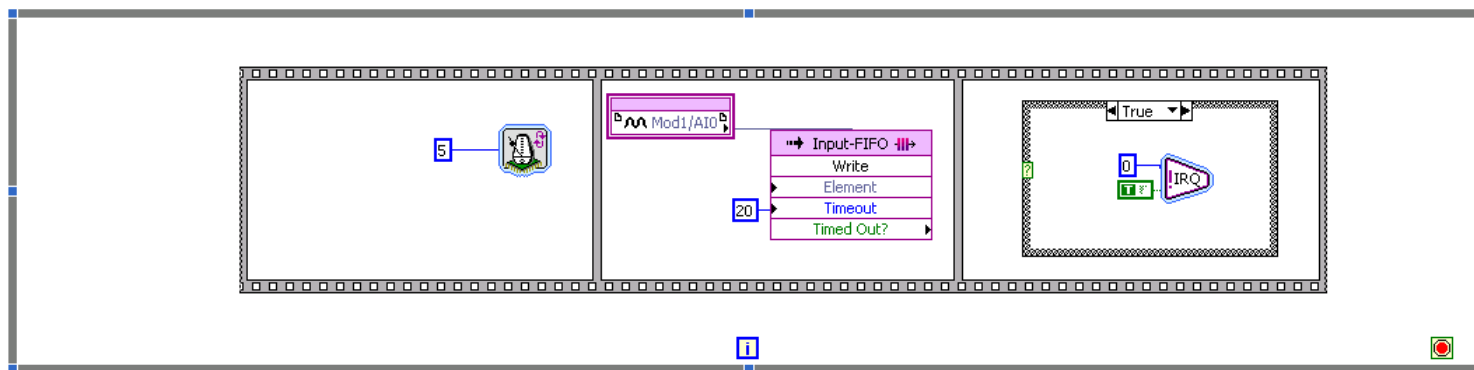
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FirstTest.lvproj/FPGA Target



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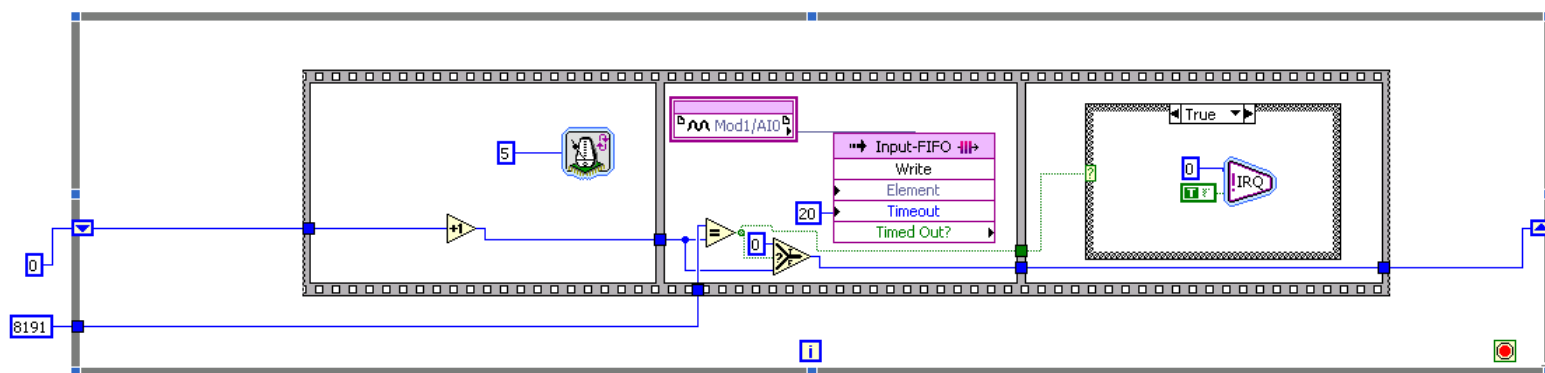
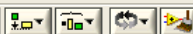
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FirstTest.lvproj/FPGA Target

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Questions

