

United States Naval Research Laboratory

Inexpensive Radar for Through-Object Viewing

Progress Report 1

Team 4

Ali Aqel

Michael Volz

Garrett Warnell

Scott Warren

Michael Weingarten

Facilitator

Dr. Terence Brown

Summary

Though only halfway through the semester, Team 4 has made tremendous progress. The core radar hardware and software are each nearing completion. The early stages of the hardware/software integration have begun. We are currently within our budget, and estimate a preliminary system will be online by Week 11.

Task Progress

Software

The software required for the radar system has been progressing rapidly. The analog input and output module is complete, and the core functionality of the signal processing software is nearing completion.

Currently, the analog input/output module that runs on the FPGA is complete and its synchronous functionality has been verified. This means that the analog input module is sampling during a specified time period that is in synch with the analog output. A screenshot of a LabVIEW front panel demonstrating this is shown below. Here, the analog output was connected directly to the analog input. The captured waveform in Figure 1 shows the complete waveform output by the analog output, verifying synchronous input and output operation.

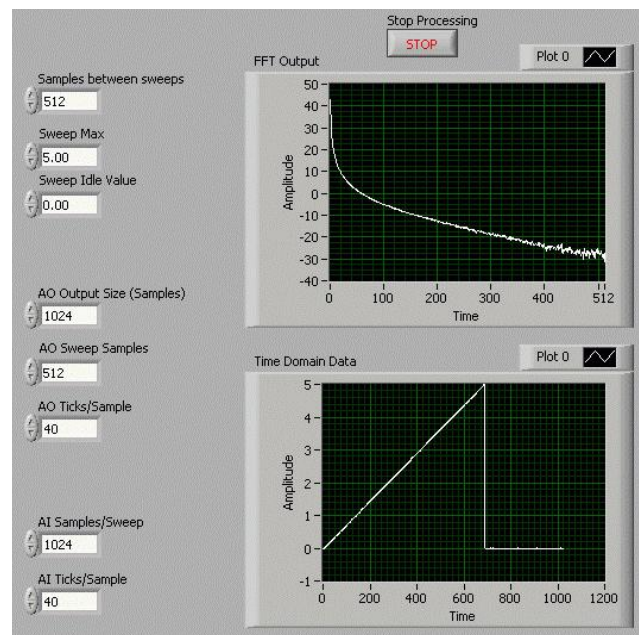


Figure 1: Synchronous Analog Input and Output Functionality

Significant progress has also been made on the signal processing software that runs on the embedded host microprocessor. In its current state, this software is able to perform the core functionality needed to build the more advanced features. First, it has the ability to drive a linear FMCW radar system. The

software generates a ramp waveform, which is transferred to the FPGA through FIFO memory. The FPGA then sends the waveform to the radar hardware through the analog output module. The software concurrently commands the FPGA to collect the received waveforms from the radar hardware via the analog input module. The sampled receive waveforms are transferred from the FPGA via FIFO memory to the embedded host processor. The precise timing needed for proper transmit and receive waveform generation and acquisition is handled by the analog input/output module described above.

For each sweep, the signal processing module converts time domain data to the frequency domain. The magnitude of the frequency domain output is displayed to the user on the laptop PC. Additionally, the signal processing module thresholds this data given a threshold value in dB. The threshold can be used for target discrimination by eliminating the display of weak, nuisance targets. The signal processing module also performs background subtraction to remove clutter from the received signal. This background subtraction can be calibrated during operation, which provides a way to adapt to a new environment.

Research is currently in progress for the moving target indicator (MTI) functionality. The team is currently evaluating two-pulse and three-pulse approaches. The goal of this module is to allow only moving targets to be displayed.

Hardware

The hardware development necessary to the project has also been moving quickly. System components have been designed and purchased, and the team is selecting enclosures and mounting methods with a balance between economy and aesthetics.

The team currently has virtually all the components necessary for the core radar functionality. The components are being integrated into enclosures, and the custom interconnecting cables are being fabricated. There will be three enclosures, for the power supplies, RF hardware, and CompactRIO respectively. This division of functionality between enclosures is common in the radar industry, and helps avoid interference between sections of the radar system. An overview of the system topology is shown in Figure 2.

The basic op amp designs have been tested with the radar hardware and software, and with minor modifications, are anticipated to work well to interface the software and hardware components. The power supplies have been selected, and their initial interconnecting wiring has been largely completed. A solution for mounting the antennas alongside the radar RF hardware has been devised. A sketch of the RF enclosure with antenna mounting is shown in Figure 3.

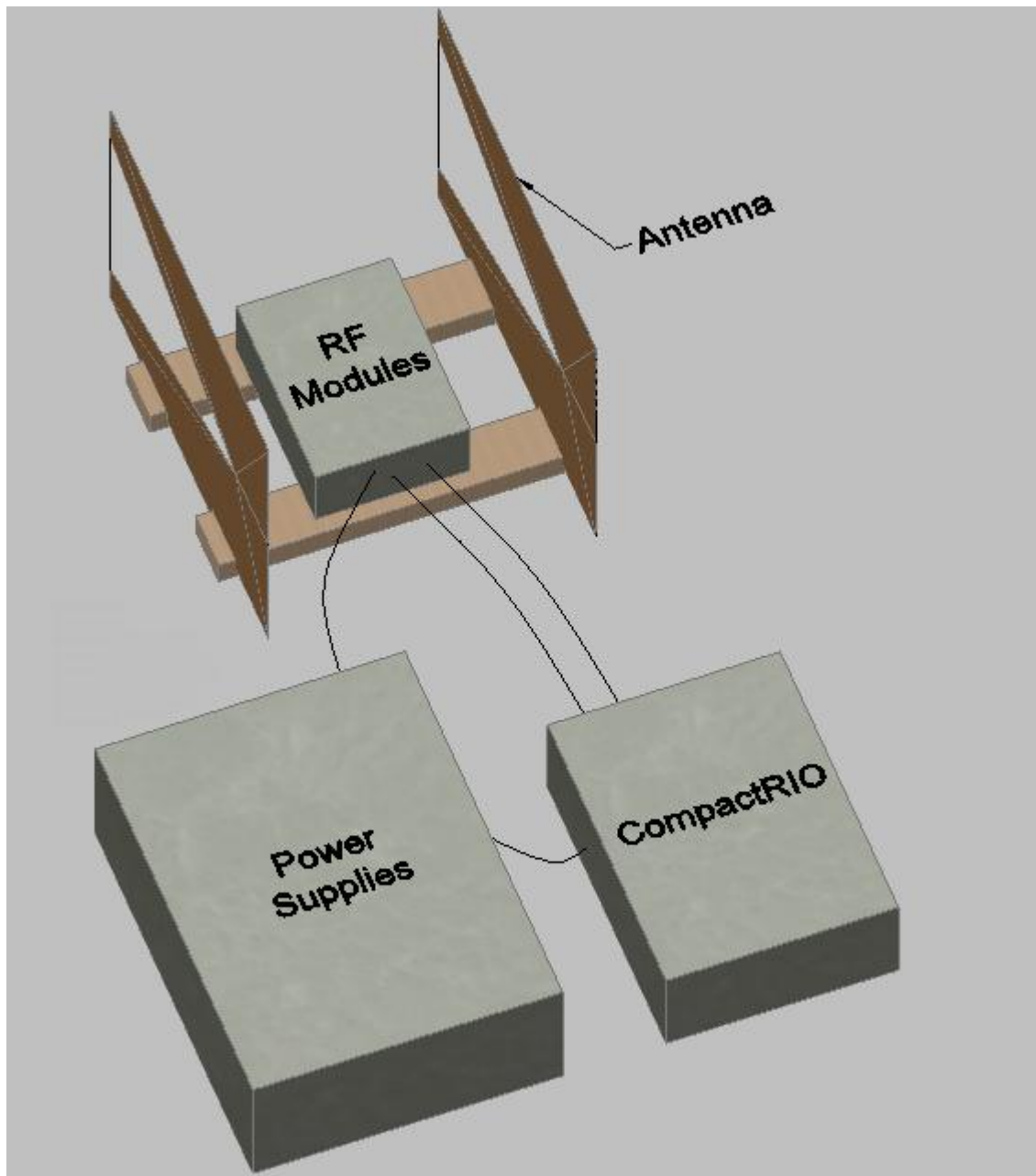


Figure 2: Overview of system enclosures

The antenna design chosen is of the LTSA (linear tapered slot antenna) type. It allows for broad bandwidth with relatively simple construction. A disadvantage of this antenna type is its relatively large size. Smaller broadband horn antennas would have cost at least \$2000, well exceeding the project budget. Because mechanically durable antennas are not a focus of the project design, the team will use the LTSA design and make it reasonably mechanically robust.

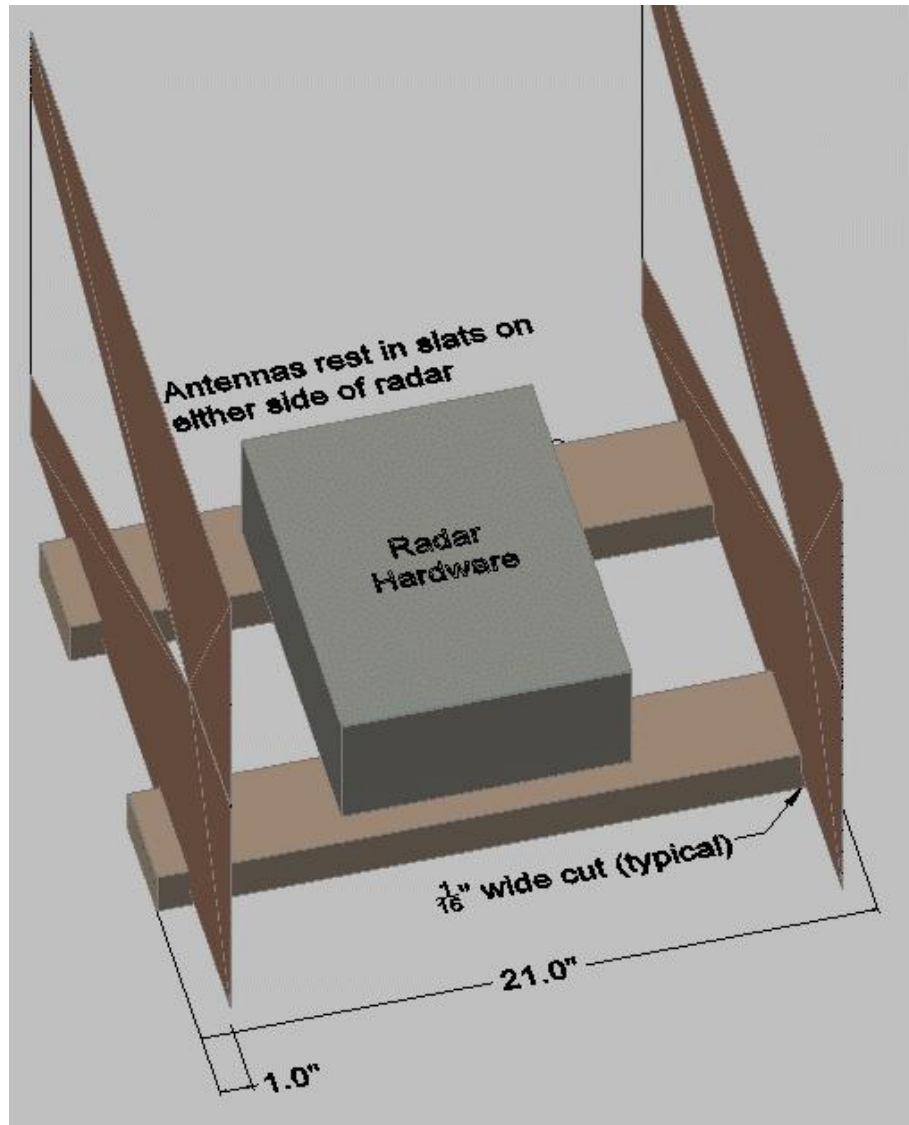


Figure 3: Overview of RF enclosure and antenna mounting

Summary

Project progress is summarized in Figure 4. The team is rapidly approaching the point where software and hardware can be integrated and the system can be tested and modified as a single system.

Section	Task	% Complete	Status
Hardware	Attain and Connect Required Components	100%	Complete
	Mount and Package Hardware	60%	In Progress
	Op Amp Design and Fabrication	75%	In Progress
	Antenna Design and Test	20%	In Progress
Software	FPGA Software (AI/AO)	100%	Complete
	Basic Signal Processing	95%	In Progress
	MTI Algorithm	25%	In Progress
	Implementation		
Integration/Test	Basic Hardware and Software Integration	75%	Pending
	Software Parameter Calibration	0%	Pending
	Basic Target Detection Test	0%	Pending
	MTI Test	0%	Pending

Figure 4: Task Progress Summary

Budget

The team has remained on-budget. In fact, the budget has changed very little from the project proposal, differing only in the addition of shipping costs and the purchase of packaging for the hardware system. A table of the current budget is given in Figure 5.

Qty.	Model	Description	Cost
1	ZX73-2500-S	Variable Attenuator	\$49.95
3	LM741 & parts	Amplifier	\$15.00
1	JSPHS-2484	Phase Shifter	\$32.95
1	ZX95-2800	Voltage Controlled Oscillator	\$49.95
2	ZX60-33LN-S	RF Amplifier	\$79.95
1	ZX05-30W-S	Mixer (S-band to RF baseband)	\$37.95
1	595-THS4021EVM	TI High-Speed Amplifier	\$55.67
1	ZAPD-30-S	2 Way Splitter	\$84.95
1	PE2202-6	2.0-4.0GHz -6dB Directional Coupler	\$261.20
1	cRIO-9072	Compact RIO (FPGA and Microprocessor)	\$1,999.00
1		NI LabVIEW w/FPGA and Real-Time Modules	\$9,097.00
1	NI9263	cRIO Analog Output Module	\$329.00
1	NI9201	cRIO Analog Input Module	\$349.00
1		RF connectors	\$86.19
1		Capacitors/resistors for op amps	\$10.48
		Misc. Costs	\$12.88
1	CU1124	Steel Cabinet 12"x7"x6"	\$58.50
Total Cost			\$12,609.62
Loaned Parts			\$12,082.47
Cost to Team			\$527.15

Figure 5: Current Budget

Forward Plan

Software

There is remaining software work to be done with regard to the MTI algorithm. The team plans to implement both the two-pulse and three-pulse methods and evaluate them after the software and hardware have been integrated.

Display work also remains. The software will need to turn frequency-domain data into a distance and display this information to the user in a relevant and easy-to understand fashion. The team has researched an equation in order to achieve this conversion and will add this to the software in the near future.

Hardware

The forward plan for the hardware involves completing the custom op amps required for the radar system. The design and pre-prototype have been tested, and fabrication and system integration remain.

Once the antennas have been tested, it is intended to create a new set of slightly more compact antennas using a similar design. These smaller antennas will eliminate wasted height, potentially increasing mechanical durability of the antenna system.

The power supplies are currently being mounted. Provision has been made to provide power to the RF and CompactRIO enclosures via mechanically robust Amphenol circular connectors.

The RF modules are having a new mounting plate made to improve the neat appearance of the RF enclosure. The RF connectors will be mounted, and the antenna mounting system will be mechanically and electrically connected to the RF enclosure.

Outlook

The team hopes to have a preliminary integrated system by the end of Week 11. This will involve connecting the hardware system to the software system and ensuring that the complete system functions as planned. The software will need to be calibrated, and basic tests and characterizations will be done for the system.