Due: Monday Oct 22

1. Using the amplifier circuit shown below, determine the values of Cf, Rf, and Ri for a low pass filter with a cutoff (-3dB) frequency of 50kHz and a DC gain of 50 (~34dB).
   Choose values of R and C that are "reasonable" for practical use, that is
   R = {100Ω – 10MΩ}, C = {1pF – 1μF}

For this structure, DC gain = Rf / Ri. If we pick Ri = 100Ω, then Rf = 50 Ri = 5,000Ω.
The -3dB frequency is $(Rf \cdot Cf)^{-1} = (2\pi)50k \rightarrow Cf = 1 / (Rf \cdot 50k(2\pi)) = 6.37x10^{-10}F = 0.64nF$.
Thus the final parameters are: **Ri = 100Ω, Rf = 5,000Ω, Cf = 0.64nF**.

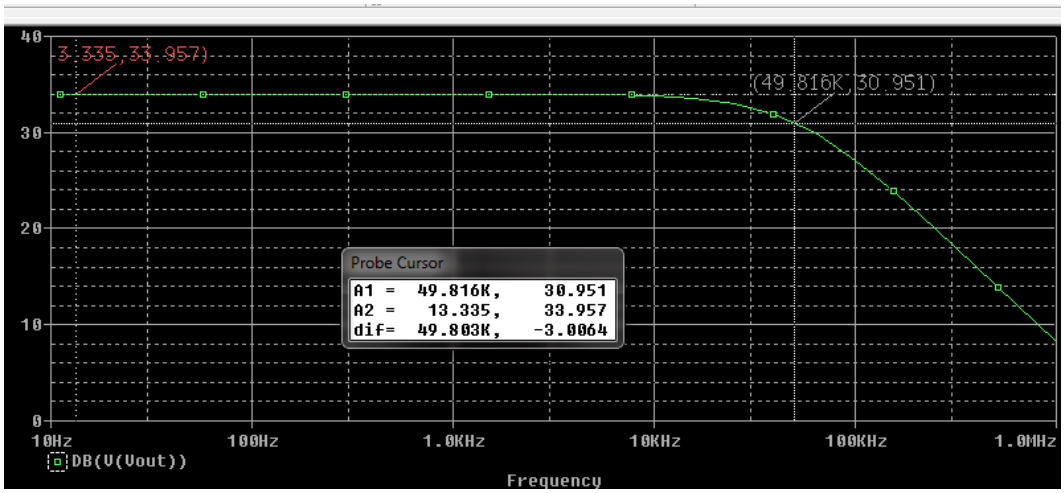
2. Use a SPICE simulator to simulate your circuit from Problem 1. Plot the frequency response (v_o/v_i) for a 1mV sinusoidal input ranging from 1Hz and 100kHz with the amplitude (y-axis) in dB scale. Measure the passband gain and the -3dB frequency and comment on how well they compare to your goals from Problem 1. What is the unity gain (0dB) frequency of your final design? Print a plot of the frequency response.
   For the opamp, use the subcircuit model below for the OP467. You may want to start with the example netlist .txt file from Lab 6 that includes the subcircuit model. Use a power supply of 10V (either ±5V or 0 to 10V), but be sure to set your analog ground –the "ground" point in the schematic above- to the middle of the supply voltages. The example netlist below creates a 10V single supply system with a 5V analog ground.

The netlist is almost exactly the same as the provided example. Only the resistance values are changed and a feedback capacitor is added.

```
XOP467 Vpos Vneg VDD GND Vout OP467
Ri Vin Vneg 100
Rf Vneg Vout 5k
Cf Vneg Vout 0.64n
```

For the calculated values from Problem 1, PSpice simulations show
DC gain = 33.96db ~= **49.89**, which is very close to the design goal of 50.
-3dB frequency at **44.8kHz**, which is a bit lower than the goal of 50kHz.
The unity gain (0dB) frequency was 2.5MHz, which requires expanding the .AC analysis stop frequency to a higher value than the example netlist used.

The design goals can be achieved by lowering the feedback capacitance to 0.57nF. With this value, the DC gain remains the same but the -3dB frequency increases to 49.8kHz, as shown in the frequency response plot below. This step is not required but show how easy it is to tweak designs once you have them entered into SPICE.



3. Using the bandpass amplifier circuit shown below, calculate the values of C_i, C_f and R_f that will give a low pass cutoff at 80kHz, a high pass cutoff at 60Hz, and a DC gain of 40 (~32dB). For hand calculations, assume the high and low cutoffs are determined entirely by R_fC_f and R_iC_i, respectively and that the gain is determined by R_f/R_i. To begin, use the value **R_i = 500Ω.** Like in Problem 1, choose values of R and C that are reasonable for practical use

For this structure, DC gain = Rf / Ri. With Ri = 500Ω, then Rf = 40 Ri = **20,000Ω**. The high cutoff frequency is $(Rf \cdot Cf)^{-1} = (2\pi)80k \rightarrow Cf = 1 / (Rf \cdot 80k(2\pi)) = 9.95\times10^{-11}F$ = **99.5pF**. The high cutoff frequency is $(Ri \cdot Ci)^{-1} = (2\pi)60 \rightarrow Ci = 1 / (Ri \cdot 60(2\pi)) = 5.31\times10^{-6}F$ = **5.31μF**.

Thus the final parameters are: **Ri = 500Ω, Rf = 20,000Ω, Cf = 99.5pF, Ci = 5.31μF.**

4. Using the subcircuit and power supply setup described in Problem 2, construct a SPICE simulation of the bandpass filter in Problem 3. Simulate and plot the frequency response using the circuit values you calculated in Problem 3. Measure the passband gain and the high and low -3dB frequencies and comment on how well they compare to your goals from Problem 3. Turn in your simulation plot, but you do not need to turn in the netlist.

For the calculated values from Problem 3, PSpice simulations show

DC gain = **39.9** ~= 32dB, which is very close to the design goal of 40.

As noted in the plot above, -3dB frequencies (gain = 28V/V) at **59.8 Hz**, which is very close to design value of 60Hz, and **71.97** kHz, which is a bit lower than the goal of 80kHz.