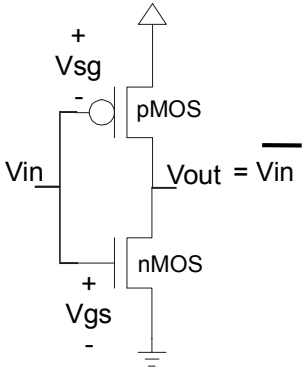
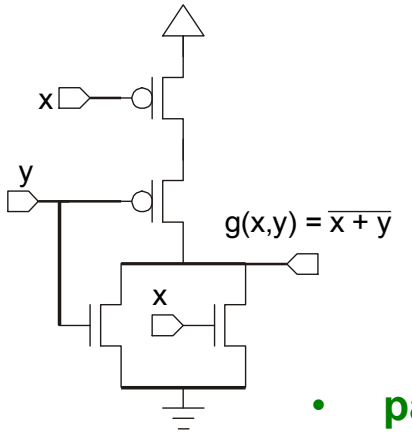
Review: CMOS Logic Gates

- INV Schematic



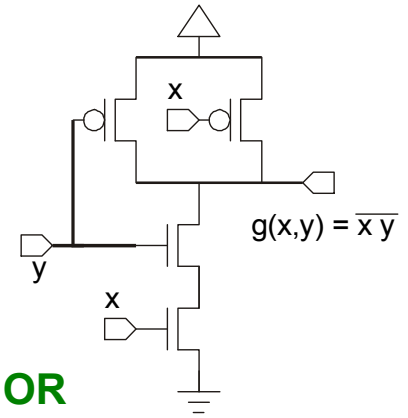
  - CMOS inverter functions

- NOR Schematic



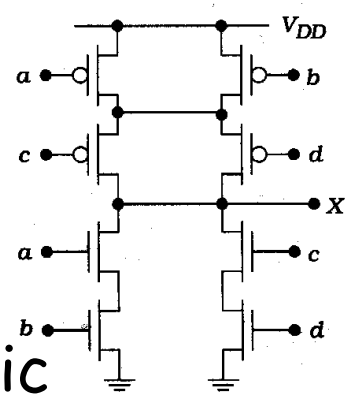
  - parallel for OR

- NAND Schematic

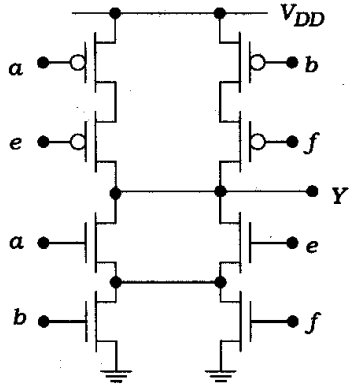


  - series for AND

- CMOS Combinational Logic
  - use DeMorgan relations to reduce functions
    - remove all NAND/NOR operations
  - implement nMOS network
  - create pMOS by complementing operations
- AOI/OAI Structured Logic
- XOR/XNOR using structured logic



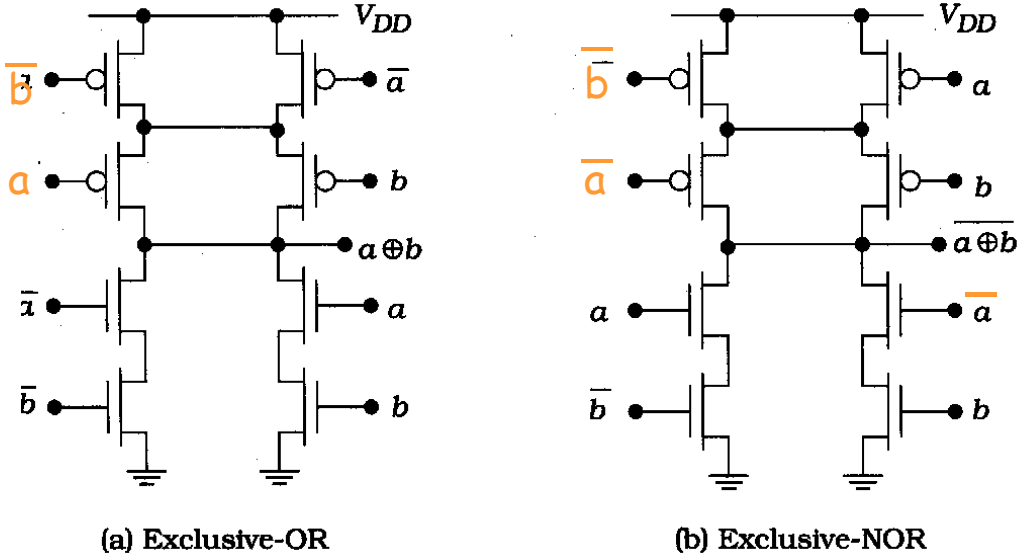
(a) AOI circuit



(b) OAI circuit

Review: XOR/XNOR and TGs

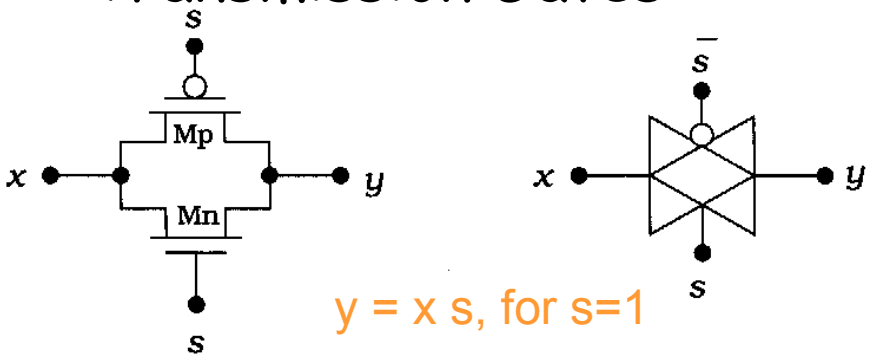
- Exclusive-OR (XOR)
  - $a \oplus b = \overline{a} \cdot b + a \cdot \overline{b}$
- Exclusive-NOR
  - $\overline{a \oplus b} = a \cdot b + \overline{a} \cdot \overline{b}$



(a) Exclusive-OR (b) Exclusive-NOR

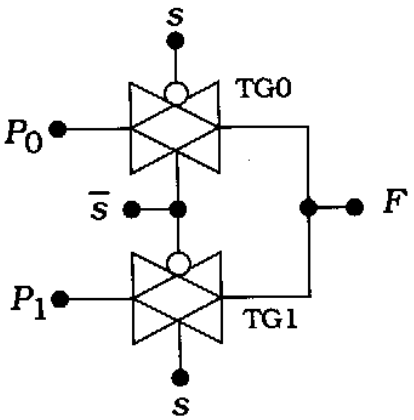
XOR/XNOR in AOI Form

- Transmission Gates



y = x s, for s=1

- MUX Function using TGs

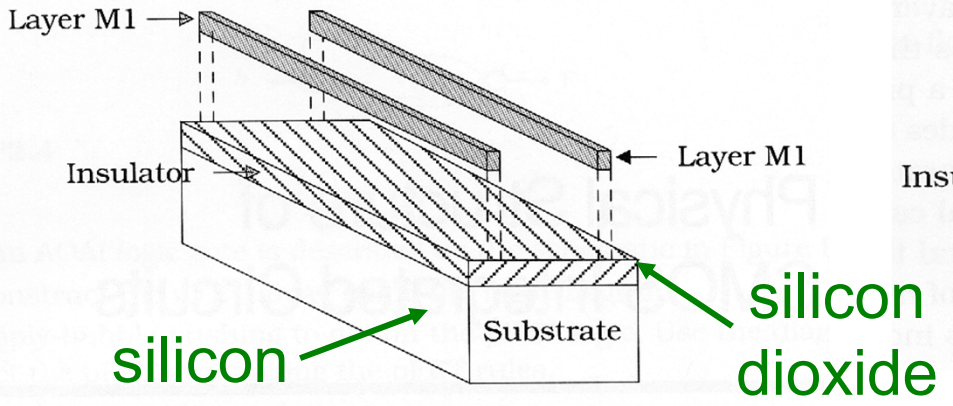


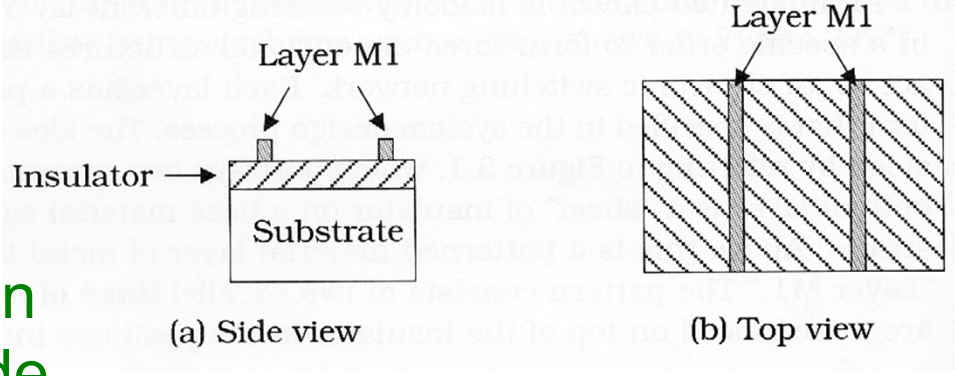
s	TG0	TG1	F
0	Closed	Open	P_0
1	Open	Closed	P_1

$F = Po \cdot \overline{s} + P1 \cdot s$

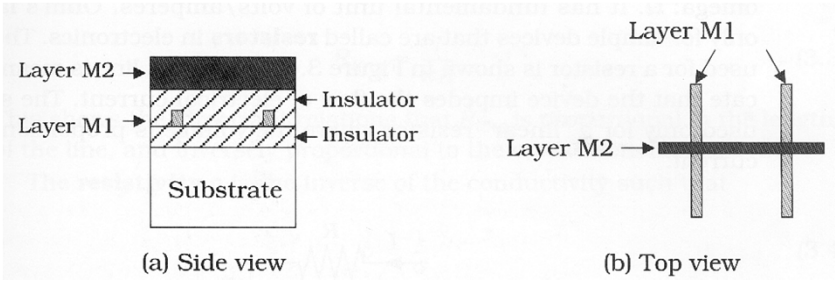
Integrated Circuit Layers

- Integrated circuits are a stack of patterned layers
  - **metals**, good conduction, used for interconnects (was Al, now copper)
  - **insulators** (silicon dioxide, High K-dielectric), blocks conduction
  - **semiconductors** (silicon), conducts under certain conditions
  - Polysilicon, resistive element, forms tx gates.
- Stacked layers form 3-dimensional structures



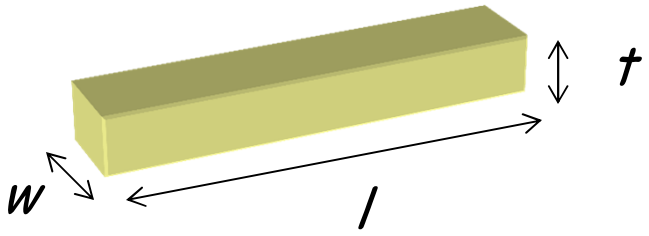


- Multi-layer metals
  - background assumed to be silicon covered by silicon dioxide



Interconnect Parasitics

- Parasitics = unwanted natural electrical elements
- Metal Resistance
  - metals have a linear resistance and obey Ohm's law
    - V = IR
  - generate parasitic interconnect resistance, R_{line}
    - $R_{line} = \frac{l}{\sigma A} = \frac{\rho\, l}{A}$
      - $A = wt$
      - ρ = resistivity, σ = conductivity

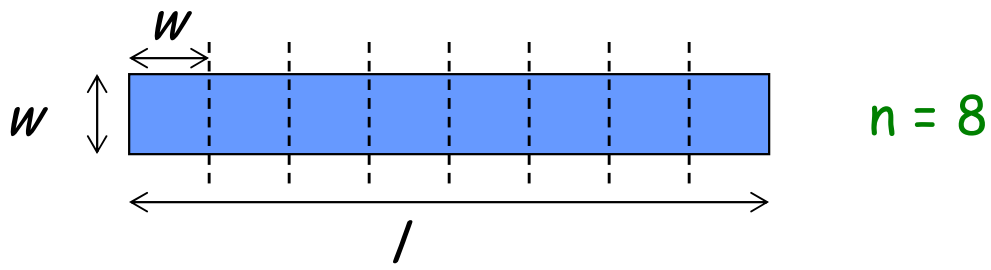


  - defined by **sheet resistance**
    - $R_s = \frac{1}{\sigma t} = \frac{\rho}{t}$, resistance per unit square [ohms, Ω]
    - $R_{line} = R_s \frac{l}{w}$, R_s determined by process, l & w by designer

$R_{line} = R_s$ when $l = w$

Metal Resistance: Measuring 'squares'

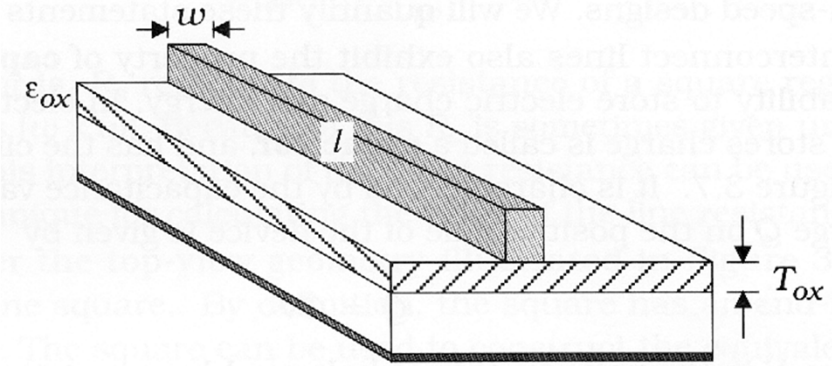
- From top view of layout, can determine how many '**squares**' of the layer are present
  - 'square' is a unit length equal to the width

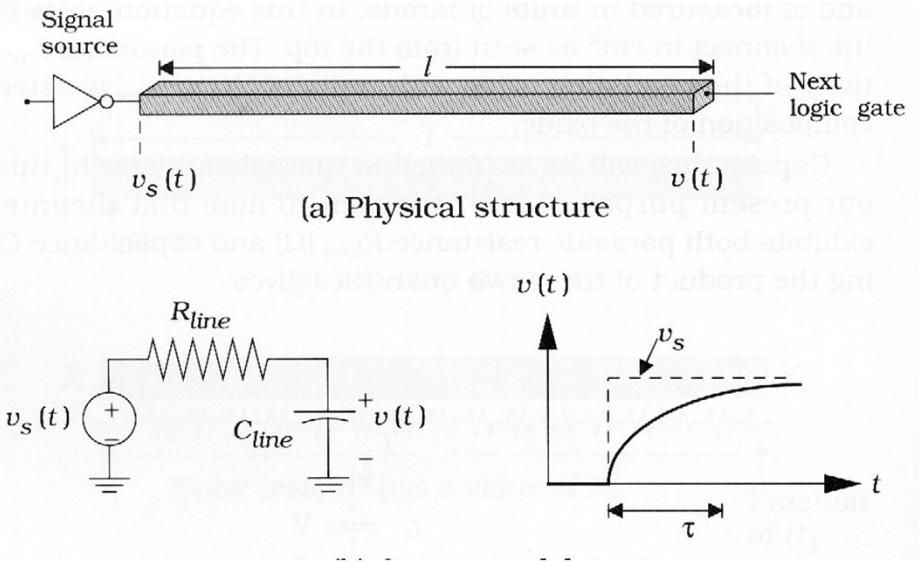


  - R_{line} = Rs n, where n = $\frac{l}{w}$ is the number of 'squares'
  - Get a unit of resistance, Rs, for each square, n.

Parasitic Line Capacitances

- Capacitor Basics
  - $Q = CV$, C in units of Farads [F]
  - $I = C\, dV/dt$
- Parallel plate capacitance
  - $C_{line} = \dfrac{\varepsilon_{ox}\, w\, l}{t_{ox}}$ [F], w l = Area
  - ε_{ox} = permittivity of oxide
- RC time constant of an interconnect line
  - $\tau = R_{line}\, C_{line}$





Intrinsic Silicon Properties

- Read textbook, section 3.2.1, 3.2.2, 3.2.3
  - Won't have time to cover this in detail in lecture, but it's <u>important to understanding how transistors work</u>
  - We'll cover some more of the physics later on
- Intrinsic Semiconductors
  - undoped (i.e., not n+ or p+) silicon has ***intrinsic*** charge carriers
  - electron-hole pairs are created by thermal energy
  - **intrinsic carrier concentration** ≡ $n_i = 1.45 \times 10^{10}\ cm^{-3}$, at room temp.
  - function of temperature: increase or decrease with temp?
  - $n = p = n_i$, in intrinsic (undoped) material
    - n ≡ number of electrons, p ≡ number of holes
  - mass-action law, $np = n_i^2$ applies to undoped and doped material

Extrinsic Silicon Properties

- doping, adding **dopants** to modify material properties
  - n-type = n+, add elements with extra electrons
    - (arsenic, As, or phosphorus, P), Group V elements
    - $n_n \equiv$ concentration of electrons in n-type material
    - $n_n = N_d$ cm^{-3}, $N_d \equiv$ concentration of donor atoms
    - $p_n \equiv$ concentration of holes in n-type material
    - $N_d\, p_n = n_i^2$, using mass-action law
      - always a lot more n than p in n-type material
  - p-type = p+, add elements with an extra hole
    - (boron, B)
    - $p_p \equiv$ concentration of holes in p-type material
    - $p_p = N_a$ cm^{-3}, $N_a \equiv$ concentration of acceptor atoms
    - $n_p \equiv$ concentration of electrons in p-type material
    - $N_a\, n_p = n_i^2$, using mass-action law
      - always a lot more p than n in p-type material
  - if both N_d and N_a present, $n_n = N_d - N_a$, $p_p = N_a - N_d$

n+/p+ defines region as heavily doped, typically $\approx 10^{16}$-10^{18} cm^{-3} less highly doped regions generally labeled n/p (without the +)

Example

$n_i^2 = 2.1 \times 10^{20}$



Conduction in Silicon Devices

- doping provides free charge carriers, alters conductivity
- conductivity in semic. w/ carrier densities *n* and *p*
  - $\sigma = q(\mu_n n + \mu_p p)$
    - q ≡ electron charge, $q = 1.6 \times 10^{-19}$ [Coulombs]
    - μ ≡ mobility [cm^2/V-sec], $\mu_n \cong 1360$, $\mu_p \cong 480$ (typical values in ***bulk*** Si)
- in n-type region, $n_n >> p_n$
  - $\sigma \approx q\mu_n n_n$
- in p-type region, $p_p >> n_p$
  - $\sigma \approx q\mu_p n_p$
- resistivity, $\rho = 1/\sigma$
- Can now calculate the resistance of an n+ or p+ region

$\mu_n > \mu_p$

electrons more mobile than holes

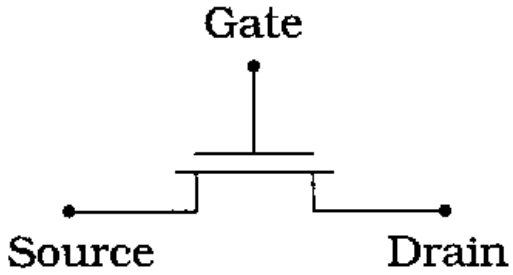
conductivity of n+ > p+

Mobility often assumed constant

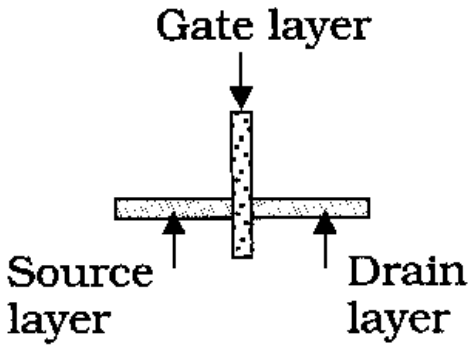
but is a function of Temperature and Doping Concentration

Physical MOSFET Switch

- nMOS Switch Layers

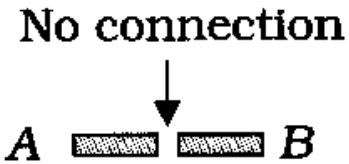


(a) nFET symbol

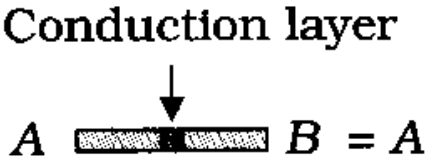


(b) nFET layers

- Physical Switching Operation



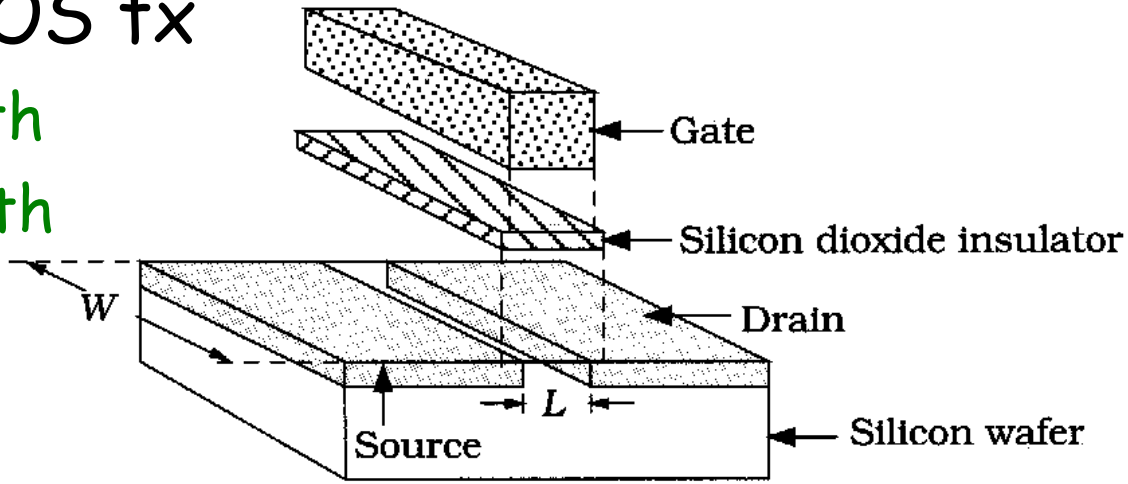
(a) Open switch



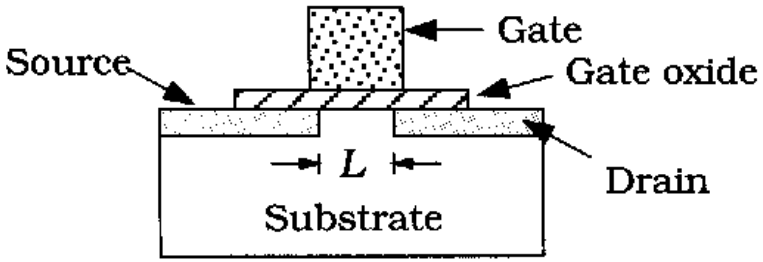
(b) Closed switch

nMOS Layers and Layout

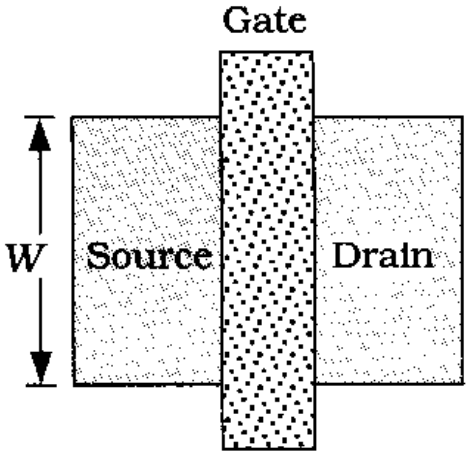
- Layers of an nMOS tx
  - L = channel length
  - W = channel width
  - gate oxide
    - separates gate from substrate



- Side and Top views



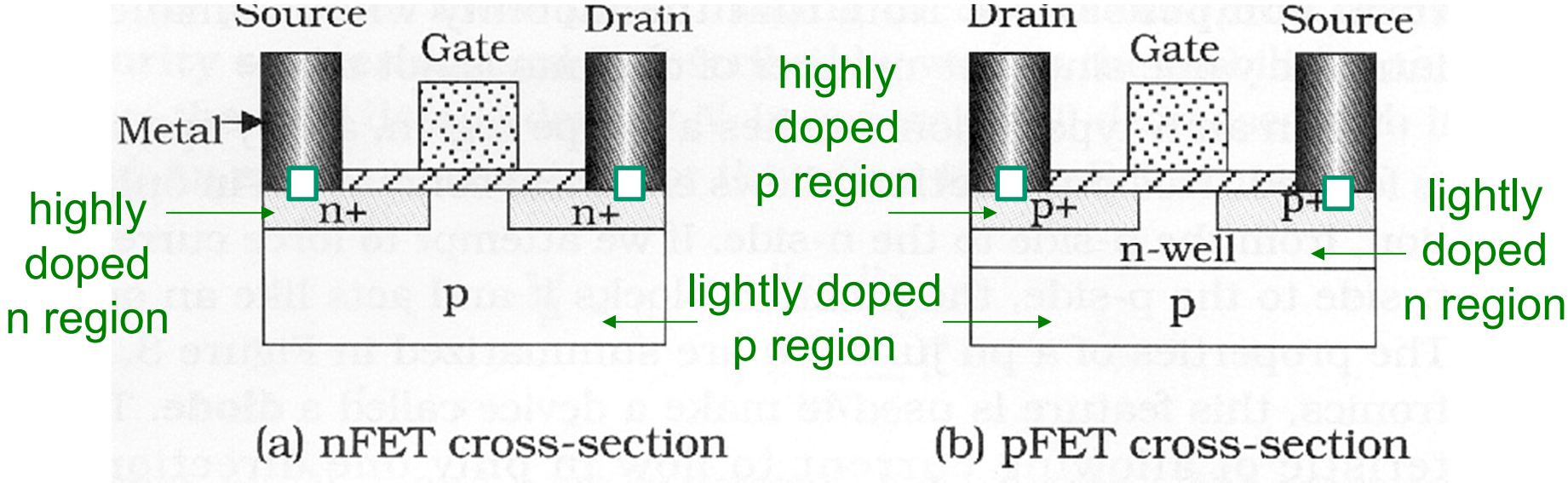
(a) Side view



(b) Top view

Physical n/pMOS Devices

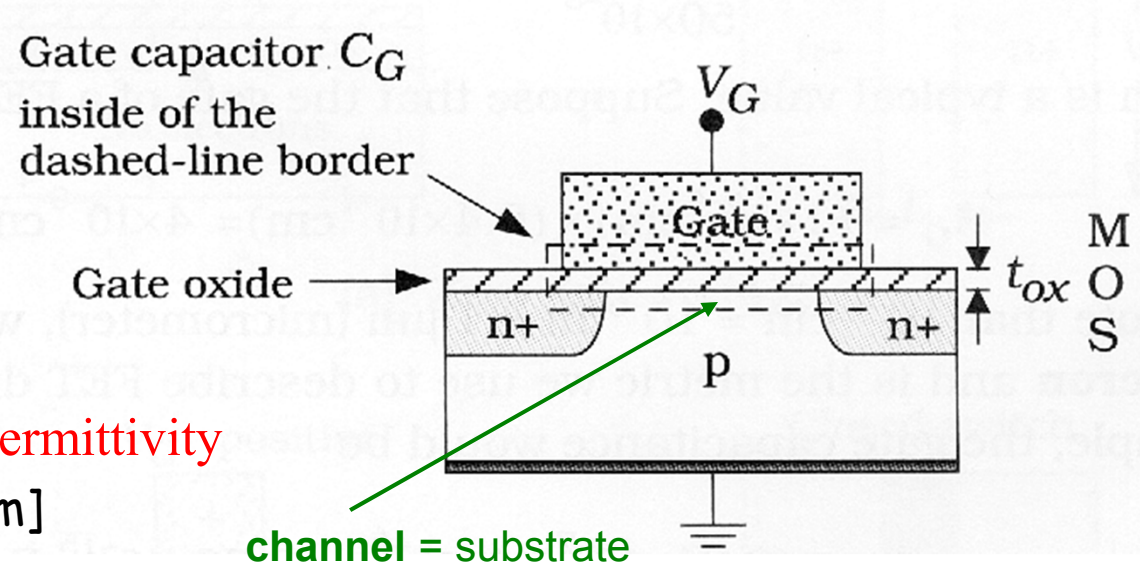
- nMOS and pMOS cross-section



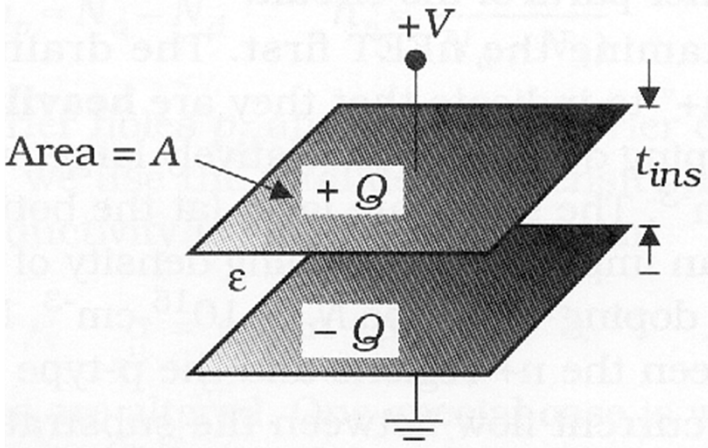
- Layers
  - substrate, n-well, n+/p+ S/D, gate oxide, polysilicon gate, S/D contact, S/D metal
- Can you find all of the diodes (pn junctions)?
  - where? conduct in which direction? what purpose?

MOSFET Gate Operation

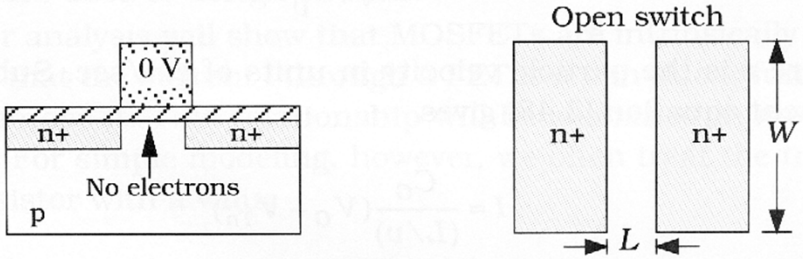
- Gate Capacitance
  - gate-substrate parallel plate capacitor
  - $C_G = \varepsilon_{ox} A / t_{ox}$ [F]
    - $\varepsilon_{ox} = 3.9\ \varepsilon_o$ ← permittivity
    - $\varepsilon_o = 8.85 \times 10^{-14}$ [F/cm]
- Oxide Capacitance
  - $Cox = \varepsilon_{ox} / t_{ox}$ [F/cm^2]
  - $C_G = Cox\ A_G$ [F]
    - A_G=gate area = L·W [cm^2]
- Charge on Gate, +Q, induces charge -Q in substrate channel
  - channel charge allows conduction between source and drain*



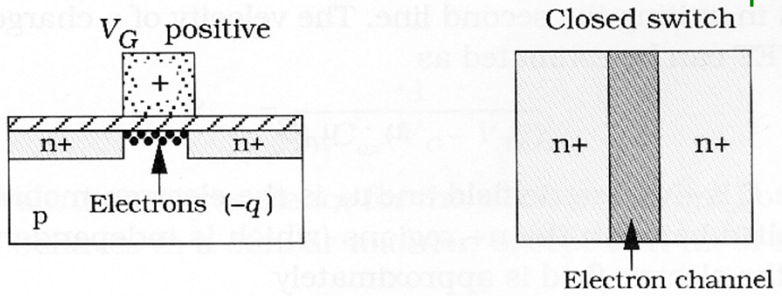
channel = substrate region under the gate, between S and D



Physical Switching in nMOS and pMOS

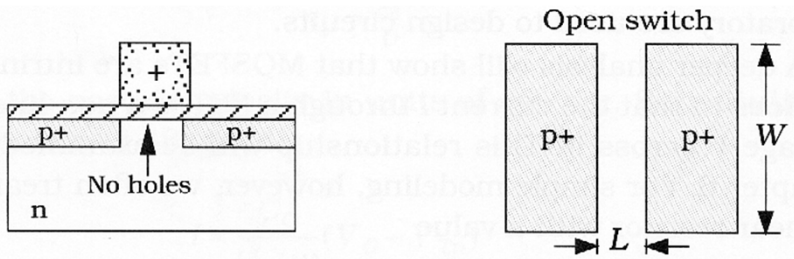


(a) Zero gate voltage

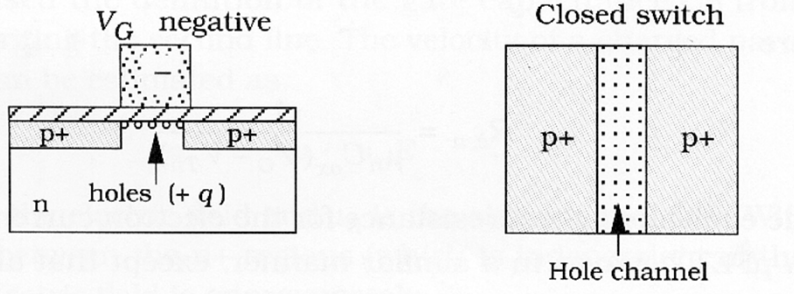


(b) Positive gate voltage

notice,
nMOS in p-substrate,
pMOS in n-substrate



(a) High gate voltage



(b) Negative gate voltage

- nMOS
  - zero or negative Q on gate
    - no charge in channel
  - positive Q on gate
    - negative charge (e^-) in channel
    - conduction path between n+ S/D
- pMOS
  - positive Q on gate
    - no charge in channel
  - negative Q on gate ($V_G < V_S$)
    - positive charge (h^+) in channel
    - conduction path between p+ S/D

Channel Charge and Current

- Threshold Voltage = Vtn, Vtp
  - amount of voltage required on the gate to turn tx on
  - gate voltage > Vtn/p will induce charge in the channel
- nMOS Channel Charge
  - $Qc = -C_G(V_G - Vtn)$, from Q=CV, (-) because channel holds electrons
- nMOS Channel Current (linear model)
  - $I = |Qc| / t_t$, where t_t = *transit time*, average time to cross channel
    - t_t = channel length / (average velocity) = L / v
    - average drift velocity in channel due to electric field E → $v = \mu_n E$
    - assuming constant field in channel due to V_{DS} → $E = V_{DS} / L$
    - → $$I = Qc\frac{\mu_n \frac{V_{DS}}{L}}{L} \qquad C_G = CoxWL \Rightarrow |Qc| = CoxWL(V_G - Vtn)$$
  - $I = \mu_n Cox\,(W/L)\,(V_G - Vtn)\,V_{DS}$ linear model, assumes constant charge in channel

similar analysis applies for pMOS, see textbook

Transconductance and Channel Resistance

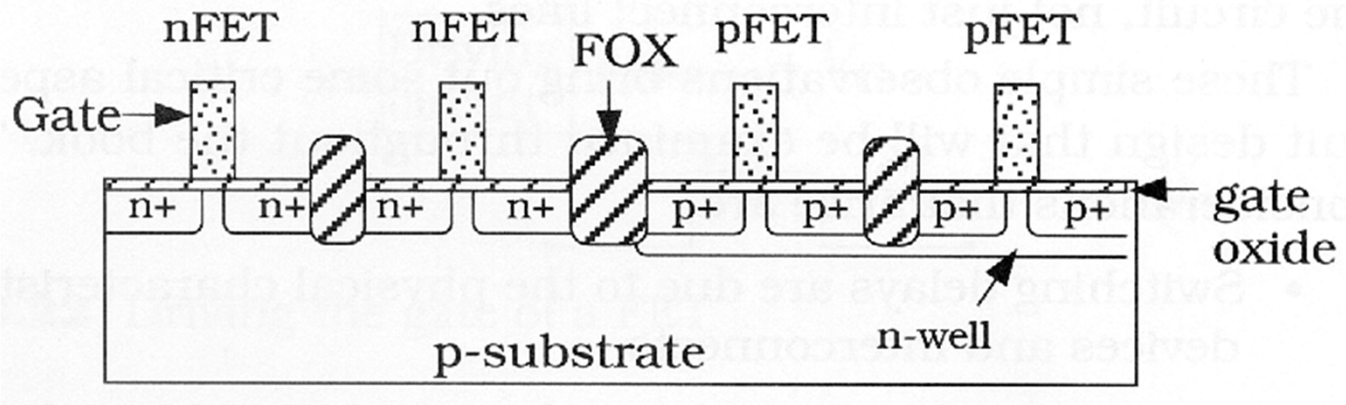
- nMOS Channel Charge: $Qc = -C_G(V_G - Vtn)$
- nMOS linear model Channel Current:
  - $I = \mu_n Cox(W/L)(V_G - Vtn)\, V_{DS}$
    - assumes constant charge in channel
    - valid only for very small V_{DS}
- nMOS Transconductance
  - $\beta_n = \mu_n Cox\,(W/L)\ [A/V^2] \Rightarrow I = \beta_n\,(V_G - Vtn)\, V_{DS}$
  - constant for set transistor size and process
- nMOS Channel Resistance
  - channel current flows between Drain and Source
  - channel resistance = V_{DS} / I_{DS}
  - $Rn = 1/(\beta_n\,(V_G - Vtn))$

$$Rn = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_G - V_{tn})}$$

similar analysis applies for pMOS, see textbook

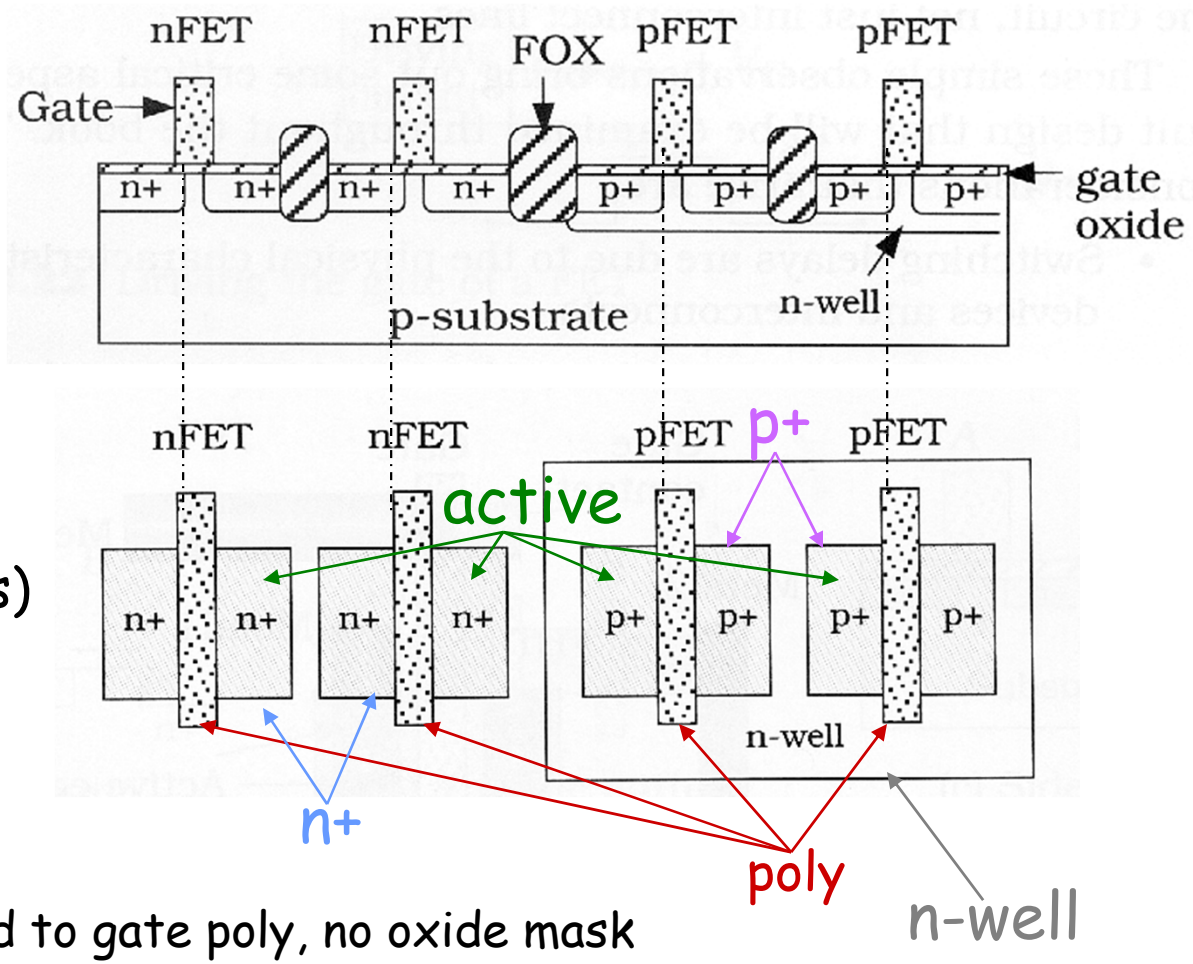
CMOS Fabrication Process

- What is a "process"
  - sequence of steps used to form circuits on a wafer
  - use additive (deposition) and subtractive (etching) steps
- n-well process
  - starts with p-type wafer (doped with acceptors)
    - can form nMOS directly on p-substrate
  - add an n-well to provide a place for pMOS
- Isolation between devices
  - thick insulator called Field Oxide, FOX



Lower CMOS Layers

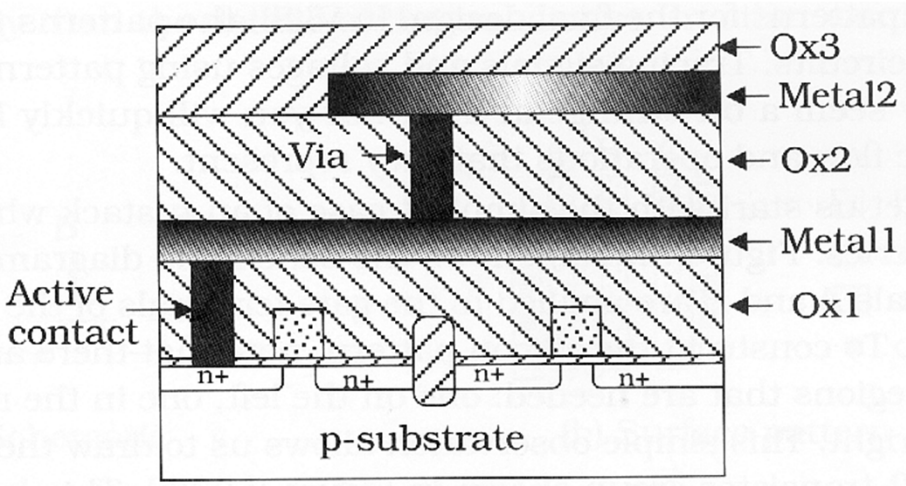
- Visible Features
  - p-substrate
  - n-well
  - n+ S/D regions
  - p+ S/D regions
  - gate oxide
  - polysilicon gate
- Mask Layers
  - n-well
  - active (S/D regions)
    - active = not FOX
  - n+ doping
  - p+ doping
  - poly patterning
    - gate oxide aligned to gate poly, no oxide mask



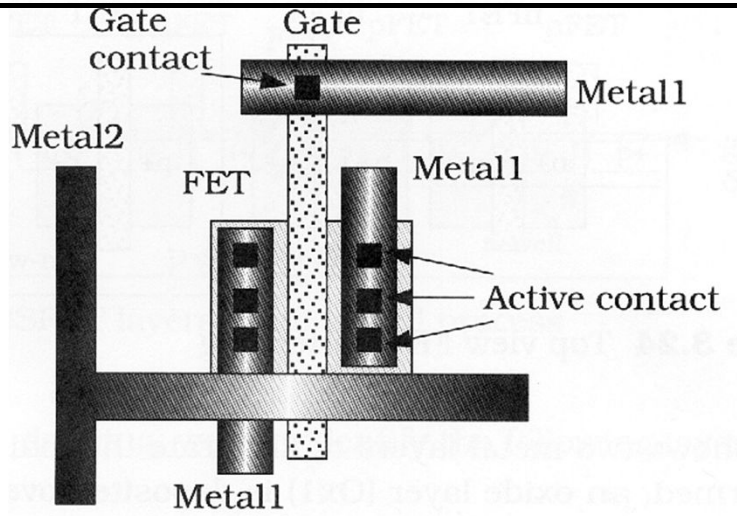
Upper CMOS Layers

- Cover lower layers with oxide insulator, Ox1
- Contacts through oxide, Ox1
  - metal1 contacts to poly and active
- Metal 1
- Insulator Ox2
- Via contacts
- Metal 2
- Repeat insulator/via/metal

only Metal 1 has direct contact to lower layers

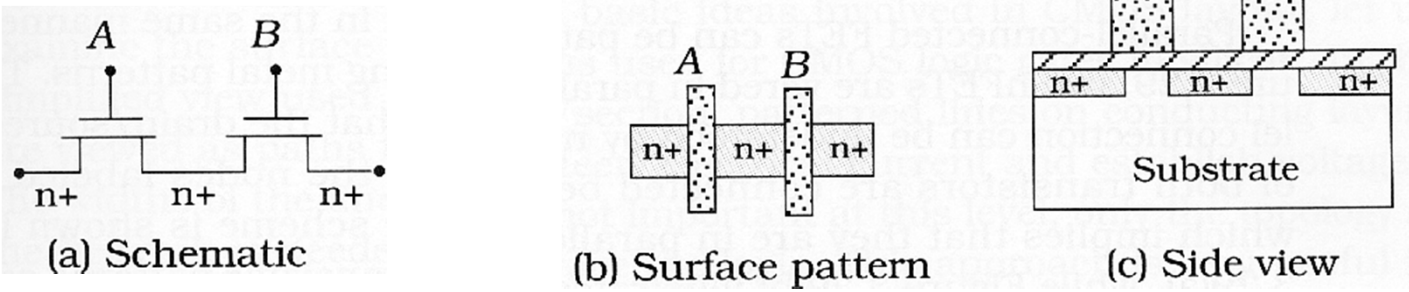


- Full Device Illustration
  - active
  - poly gate
  - contacts (active & gate)
  - metal1
  - via
  - metal2

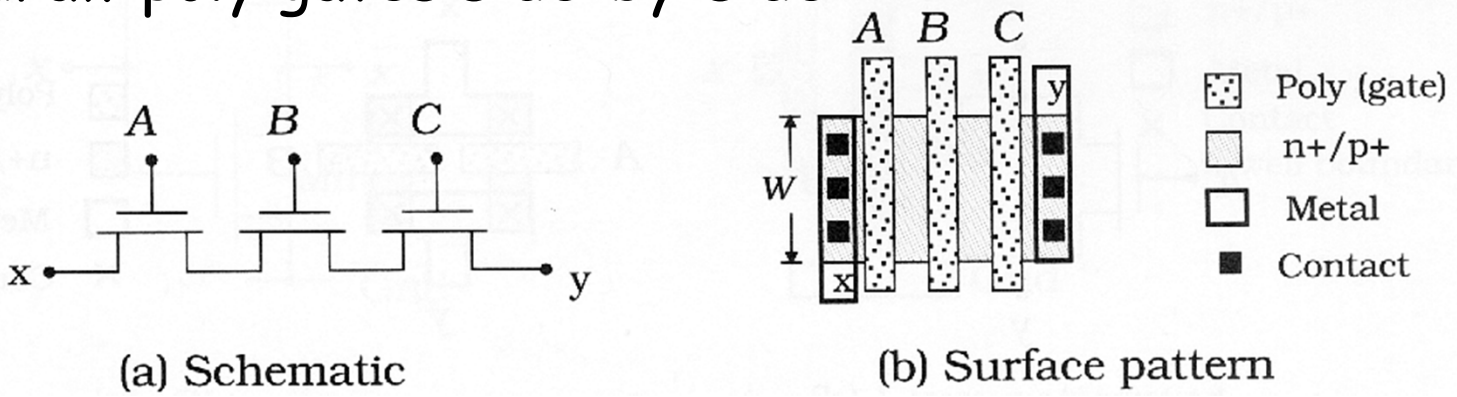


Series MOSFET Layout

- Series txs
  - 2 txs share a S/D junction

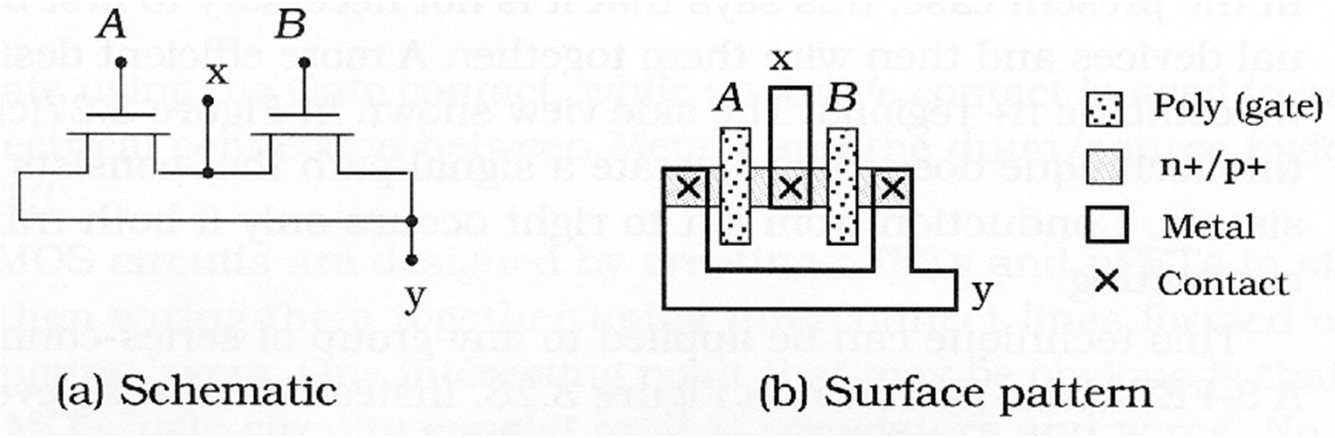


- Multiple series transistors
  - draw poly gates side-by-side

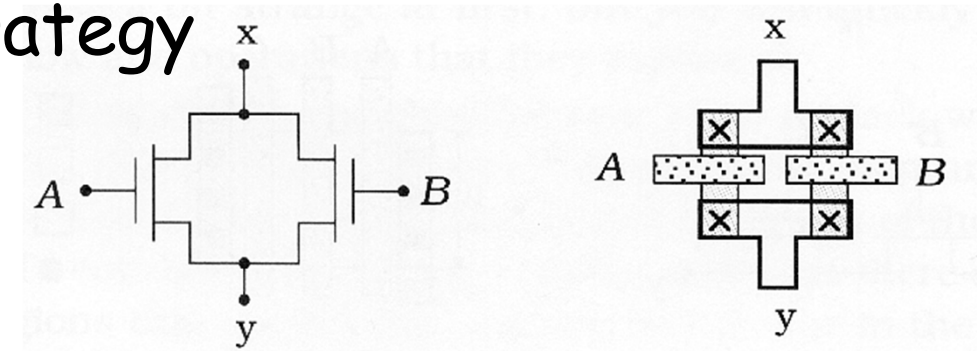


Parallel MOSFET Layout

- Parallel txs
  - one shared S/D junction with contact
  - short other S/D using interconnect layer (metal1)

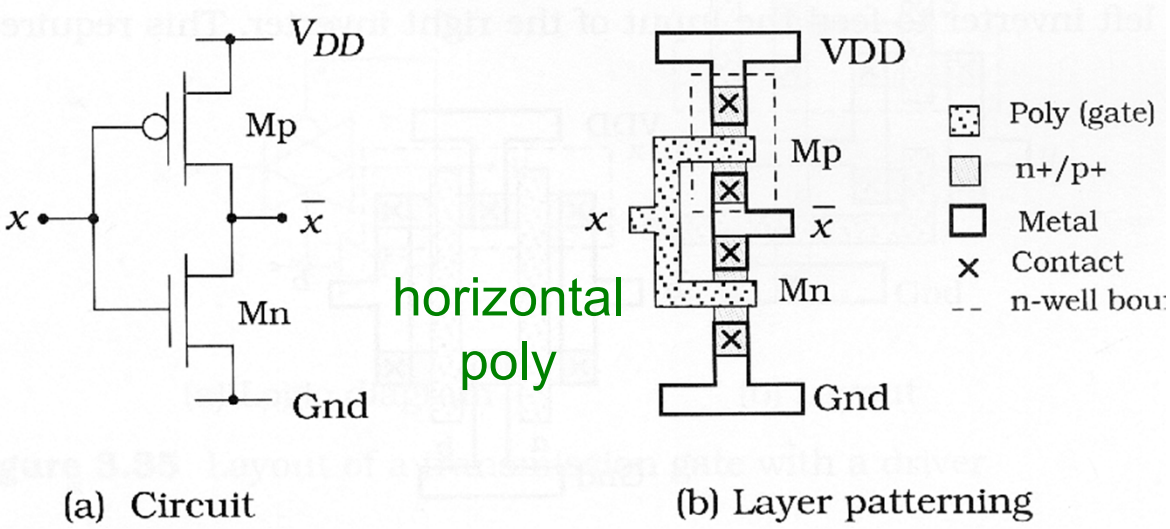


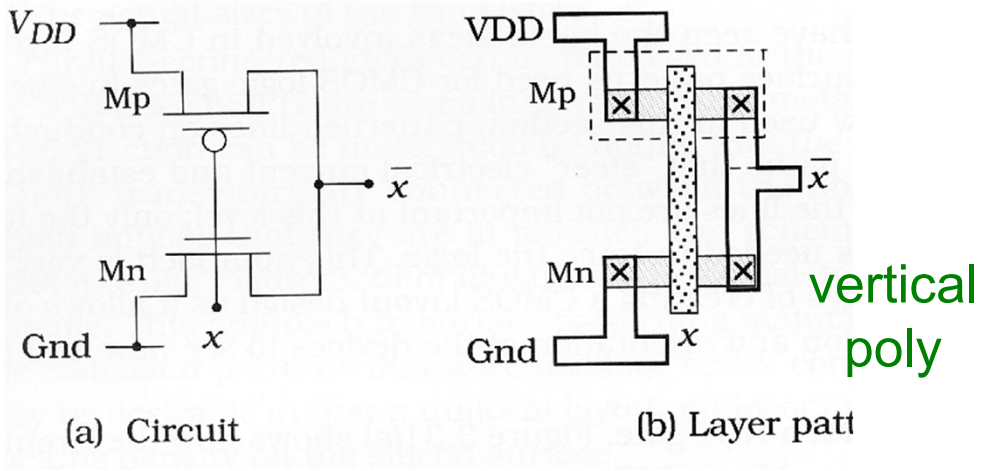
- Alternate layout strategy
  - horizontal gates



Inverter Layout

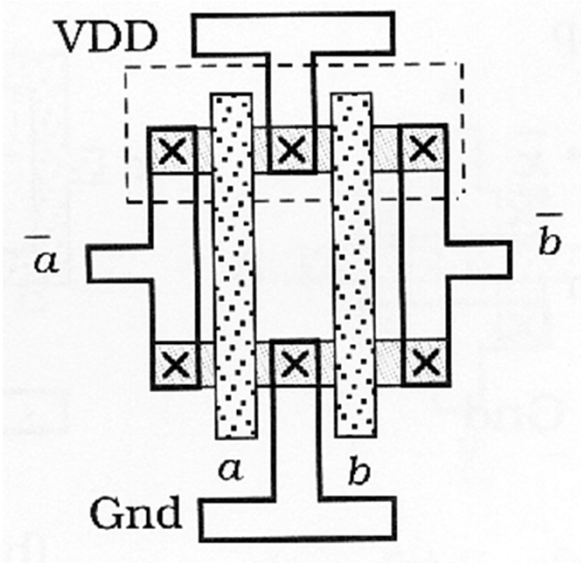
- Features
  - VDD & Ground 'rail'
    - using Metal1 layer
  - N-well region
    - for pMOS
  - Active layers
    - different n+ and p+
  - Contacts
    - n+/p+ to metal
    - poly to metal
- Alternate layout
  - advantage
    - simple poly routing
  - disadvantage
    - harder to make W large



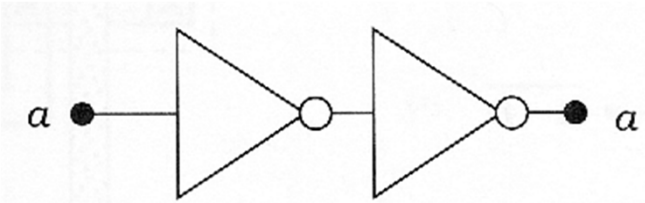


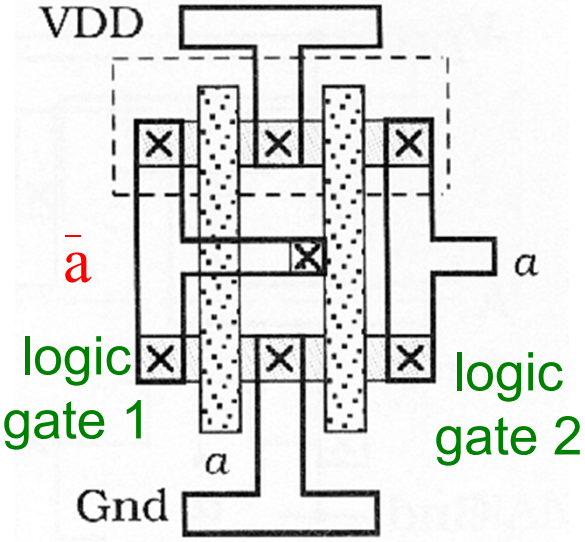
Multiple Gate Layouts

- Sharing power supply rail connections
  - independent gate inputs and outputs
  - shared power supply nodes
  - logic function?



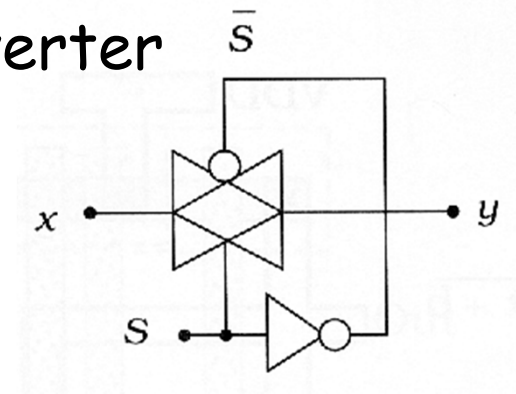
- Cascaded Gates
  - output of gate 1 = input of gate 2
    - g1 output metal connected (via contact) to g2 gate poly
  - shared power supply node
  - function?
    - non-inverting buffer

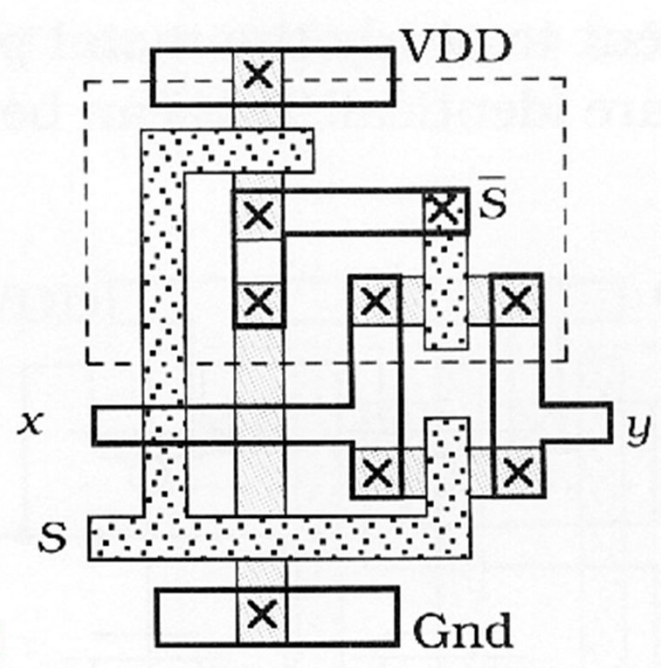




Complex inter-cell routing

- Transmission gate with built-in select inverter
  - one TG gate driven by s at inverter input
  - one TG gate driven by s' at inverter output
  - complicates poly routing inside the cell
    - figures uses n+ to route signal under metal 1
      - not great choice due to higher S/D junction capacitance

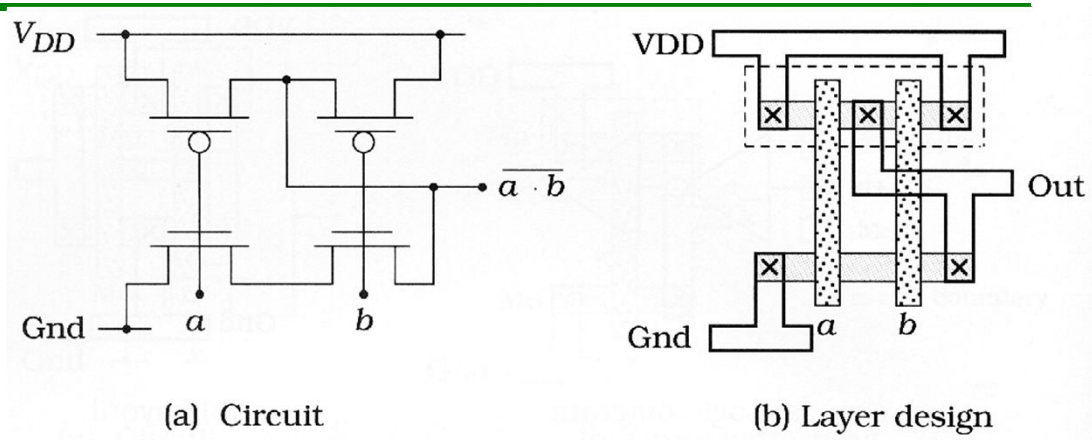




- Routing rules
  - poly can cross all layers except
    - poly (can't cross itself)
    - active (n+/p+), this forms a transistor
  - metal can cross all layers except
    - metal (can't cross itself)

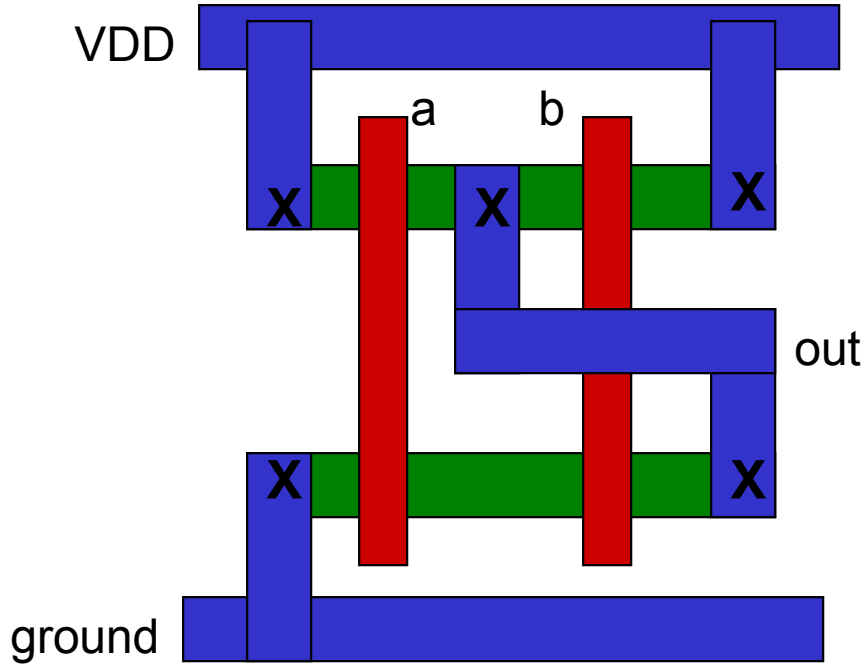
Stick Diagram NAND

- Simplified NAND Layout
  - several layers not shown



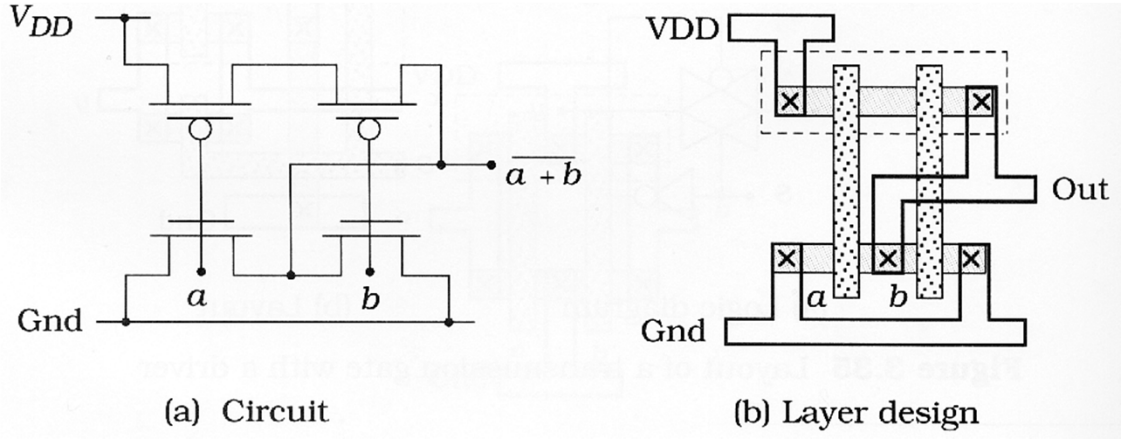
Stick Diagram

- Metal supply rails
  - blue
- n and p Active
  - green
- Poly gates
  - red
- Metal connections
  - supply, outputs
- Contacts
  - black X



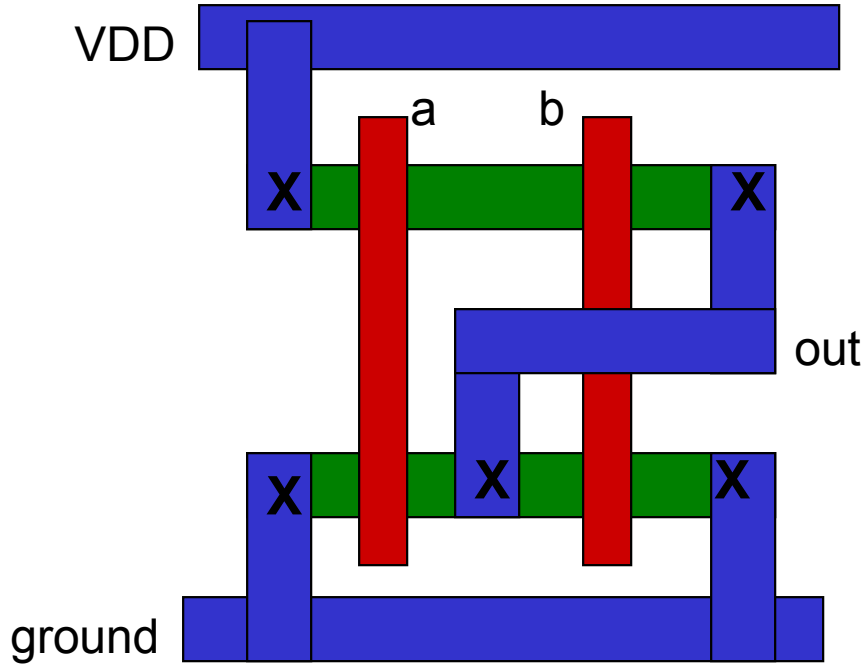
Stick Diagram NOR

- Simplified NOR Layout
  - several layers not shown



Stick Diagram

- Metal supply rails
  - blue
- n and p Active
  - green
- Poly gates
  - red
- Metal connections
  - supply, outputs
- Contacts
  - black X



Stick Diagrams

- Stick Diagram Rules
  - apply to full layout also

•Poly over Active = tx

nMOS unless in n-well

(or near top/VDD--mostly)

•Poly can cross Metal1 and Metal2

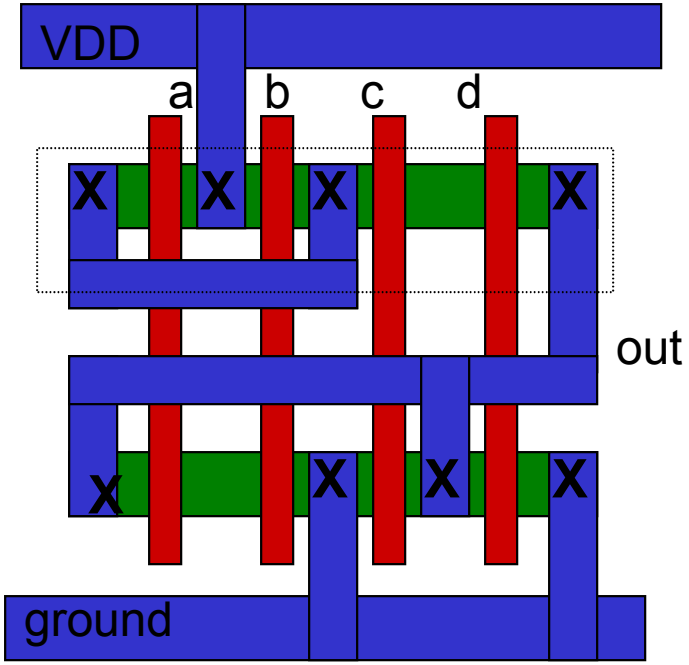
•Metal1 can cross Poly, Active, Metal2

•Metal2 can cross Poly, Active, Metal1

•tx S/D **Contact** must be on Active-Metal1

•(poly) **Contact** must be on Poly-Metal1

•**Via** connects Metal1 and Metal2

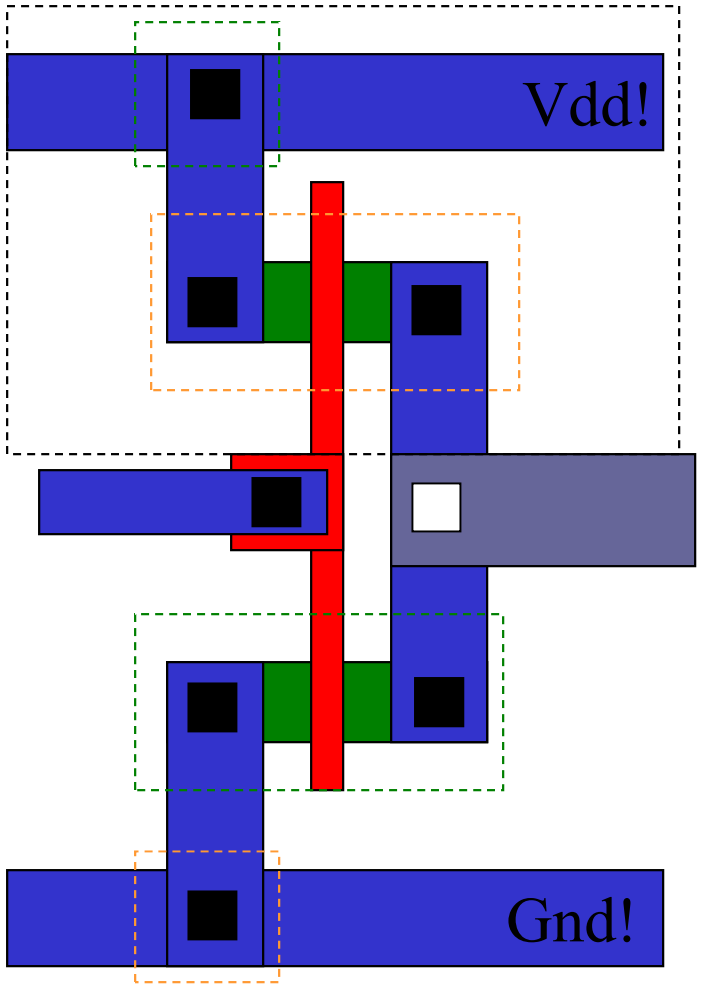


What is this logic function?

MOSFET INV Layout & Masks

Background is the p-substrate/Overglass covers top

- N-well
- Active
- N-Select
- P-Select
- Poly
- Active/Poly Contact
- Metal1 (M1)
- Metal2 (M2
- Via



See an example of the animated **CMOS process flow**– (http://www.silicon-edge.co.uk/swf/cmos.swf)

MOSFET Layout & Masks

Some Layout Cell Definitions

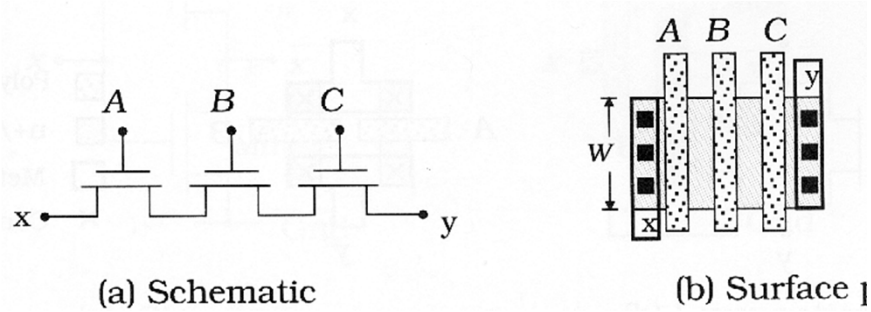
•Cell Pitch = Height of standard cells
Usually, measured between VDD & GND rails

•Cell Boundary
max extension of any layer (except nwell)
–set boundary so that cells can be placed side-by-side without any rule violations
–extend power rails 1.5λ(or 2λto be safe) beyond any active/poly/metal layers
–extend n-well to cell boundary (or beyond) to avoid breaks in n-well

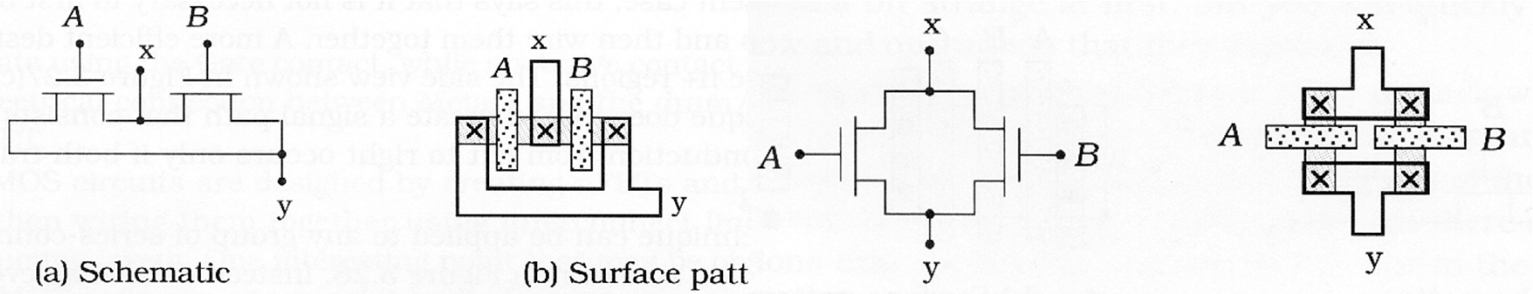


Review: CMOS Physical Design

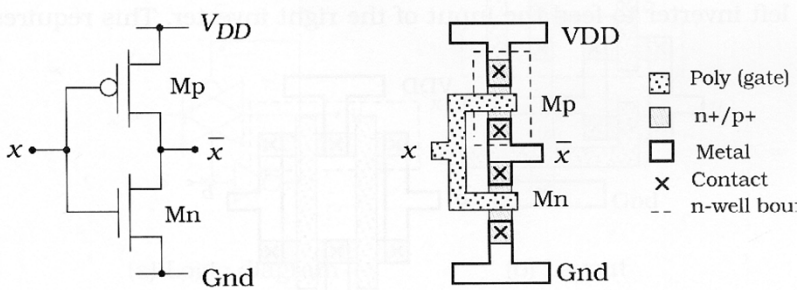
- Series txs
  - 2 txs share a S/D junction
  - can have many txs in series
- Parallel txs
  - one shared S/D junction with contact
  - short other S/D using interconnect layer (metal1)
- CMOS Inverter



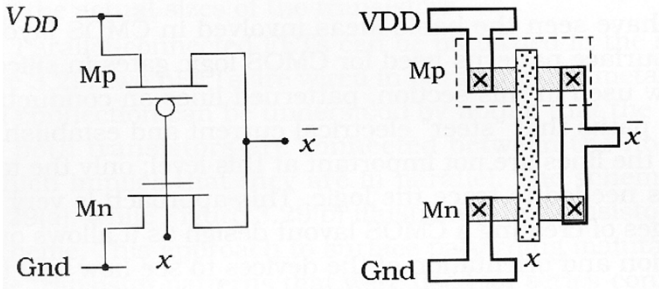
(a) Schematic (b) Surface



(a) Schematic (b) Surface patt



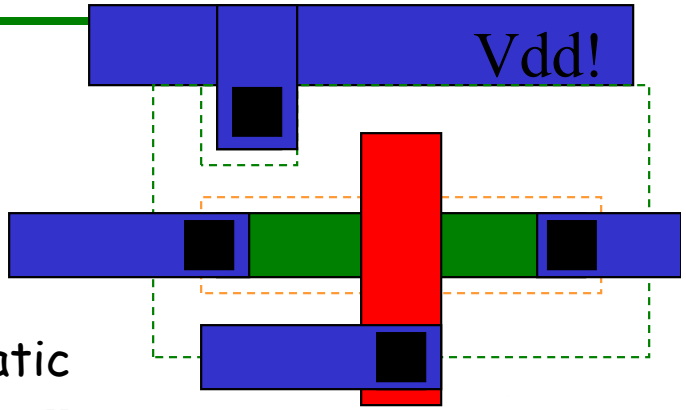
(a) Circuit (b) Layer patterning

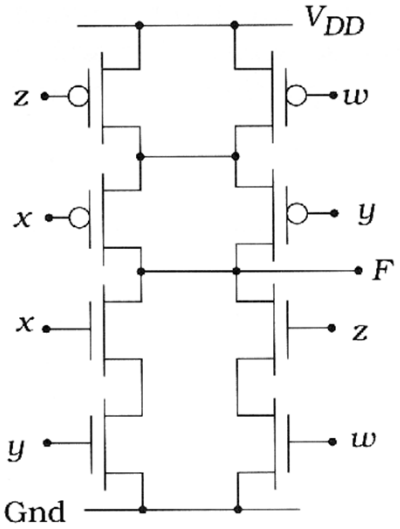


(a) Circuit (b) Layer patt

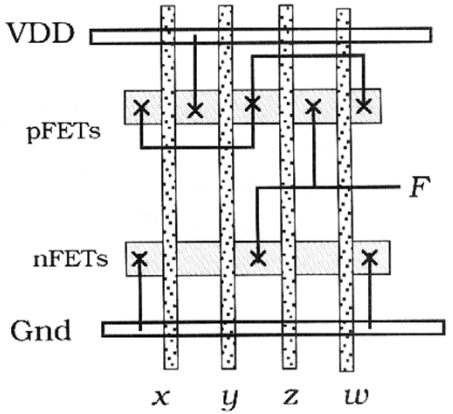
Structured Layout

- General Approach
  - power rails
  - horizontal Active
  - vertical Poly (inputs from top/bottom)
  - Metal1 connects nodes as needed in schematic
- Structured Layout
  - AOI circuit figure
  - useful for many logic functions
  - see examples in textbook
- Disadvantages
  - not optimized for speed
    - large S/D regions = higher capacitance
    - interconnect paths could be shorter
  - not optimized for area/size





(a) Circuit

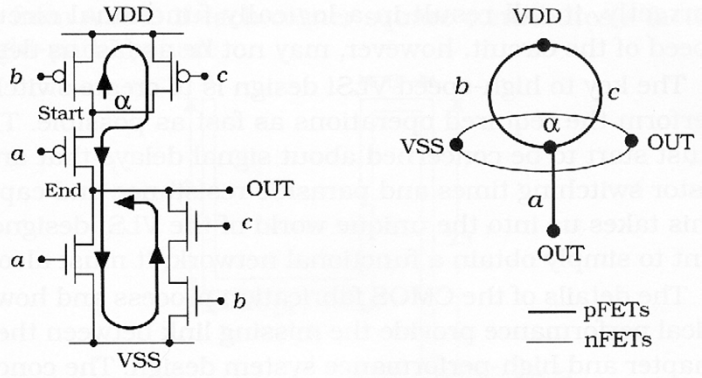


(b) Layout wiring

Note: need room inside cell (between VDD and Ground) to route internal connections

Euler Graphs

- Euler Graph
  - method for determining what order to layout txs
  - assign each circuit node as a point
  - assign each tx as a line between points
- Method
  - locate starting point
  - trace a loop from starting point through each transistor
    - can only re-cross a point once, separate nMOS loop must cross each pMOS
  - if above is possible, all tx can be in same Active
  - if not, will require multiple Active regions



(a) Circuit with path (b) Euler graph

