Cadence Tutorial C: Simulating DC and Timing Characteristics

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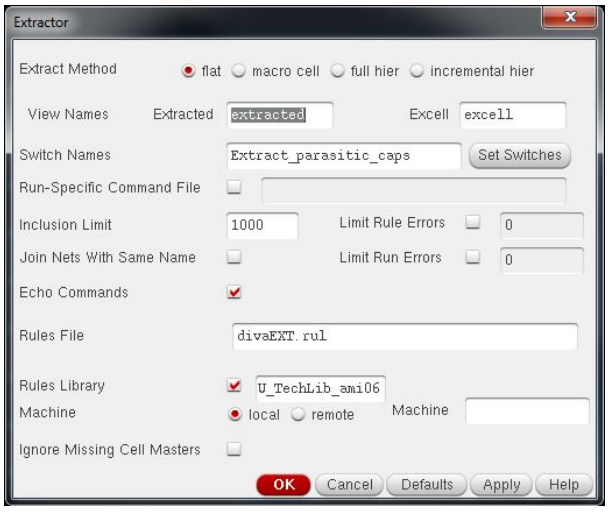
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Introduction

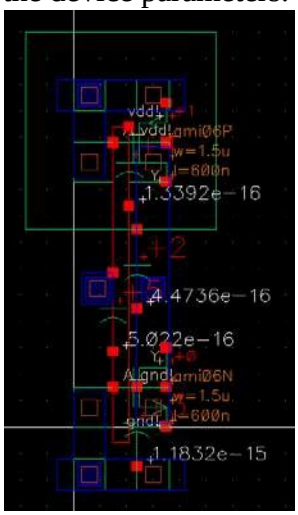
This document is the third of a three-part tutorial for using CADENCE Custom IC Design Tools for a typical bottom-up circuit design flow with the AMI/C5N process technology and NCSU design kit. Tutorial A and B cover the use of the Virtuoso schematic entry tool, Virtuoso analog simulation tool and Virtuoso layout tool. This tutorial covers the timing analysis on the schematic and extracted view. It is assumed you have followed Tutorials A and B and have the schematic and layout views of a CMOS inverter.

Layout Extraction with Parasitic Capacitances

- Launch Cadence and open the layout view for the inverter cell.
- In the Command Interpreter Window (CIW), set the capacitance-ignore-threshold by entering *NCSU_parasiticCapIgnoreThreshold=1e-18* in the prompt at the bottom of the CIW and pressing Enter. Although this was not needed for functional simulations, it will make timing analysis more accurate.
- In the Virtuoso Layout Editing window select **Verify => Extract**. A new window (below) with extraction options will appear.
- Click on **Set Switches** and select ***Extract_parasitic_caps***. Click on **OK** to extract parasitic elements from the layout with the new parasitic capacitance threshold.
- After extraction, check the CIW to make sure there are no errors.
- Load the extracted cellview from the Library Manager window. This will open up a layout should look similar to the one below. Press **shift+f** to see all the device parameters.



Extract Window

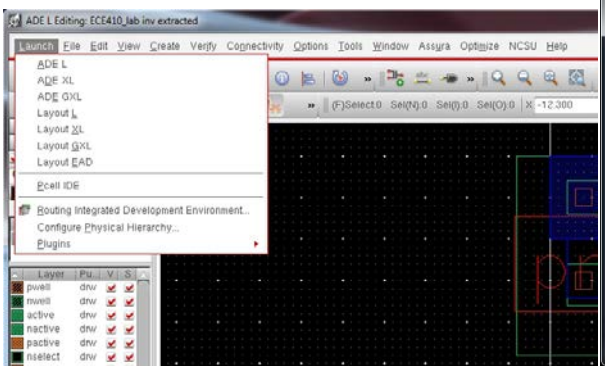


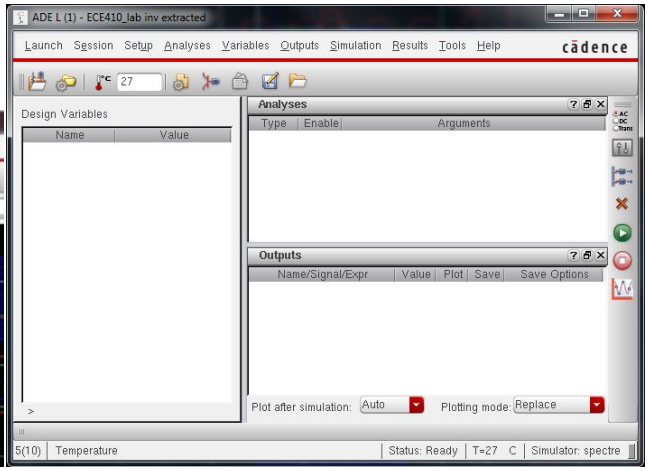
Extracted Layout View

Timing Analysis

STEP 1. Start Analog Environment(ADE L)

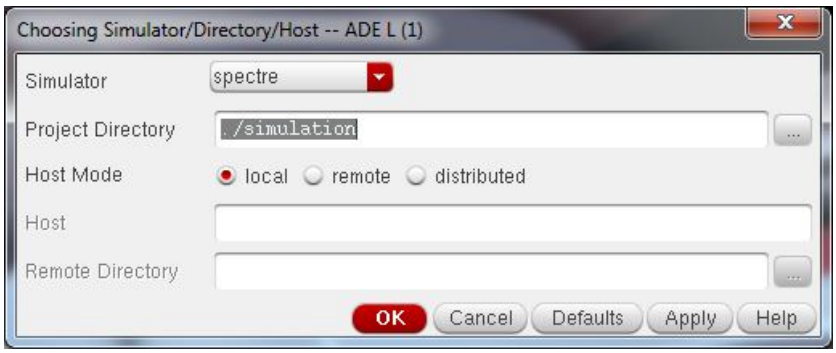
- With the extracted view open, in the Virtuoso Layout Editing window select Launch=> Analog Design Environment(ADE L) to open the Virtuoso Analog Circuit Design Environment window.
  - You can also launch this tool from the CIW by selecting Tools => Analog Environment => Simulation.





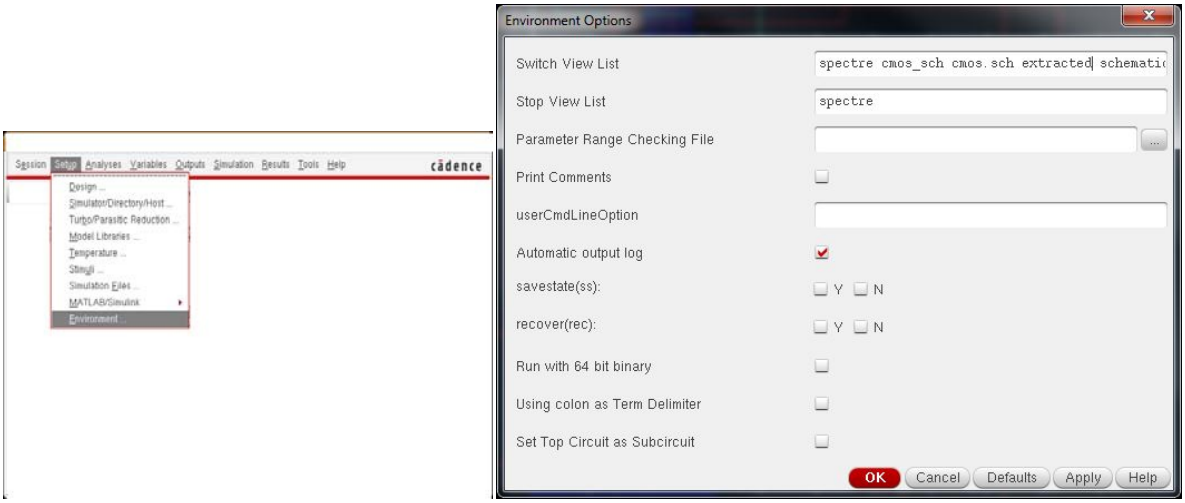
STEP 2. Setup Analog Simulator

- In VirtuosoAnalog Design Environment, click on Setup => Simulator/Directory/Host.
- Choose **spectre** as the Simulator.
- Enter a path for your simulations files and results. You may set this to any valid path, but you might find it useful to keep all simulations in one directory. If you don‟t specify the whole path, the simulation files and results will be created under the directory you launched cadence. The following example saves the simulation file and results at /egr/courses/unix/ECE/410/<username>/simulation assuming you launched Cadence from your root 410 class directory If you need to run multiple simulations on the same cell, you can even use different paths for each simulation.
- When the Virtuoso Analog Circuit Design Environment opens you have click on Setup => Design to specify the library and cell, for example “tutorial” and "inv". Also, make sure that you are opening the extracted view.



STEP 3. Set up Analog Environment to use Extracted View

- In Virtuoso Analog Design Environment, click on **Setup => Environment**. The Environment Options dialog box (below) will pop up.



- In the Environment Options window, under the line *Switch View List*. type the word "**extracted**" before the word "schematic" (see below).

  This entry is an ordered list of cell views which contain information that can be simulated. The simulator (in fact the netlister) will search until it finds one of these cellviews. The default entry does not contain an *extracted* cellview. As a result of this modification, the simulator will use the extracted cellview instead of the schematic cellview to include the effect of parasitic capacitance in the simulation.



- Then click on **OK**.

STEP 4. Set up stimulus file

- Create a new stimulus file by opening any text editor. Make sure to give the file a name either when you create it or when you save it, depending on your text editor ("stimulus.txt", for example).
- Enter the following text, save the file and exit the text editor. (*Note: each circle bulleted item below represents one full line in the stimulus file; be careful if you cut and paste this text. You also need to be sure to hit Enter after the last line to insert a line return in the text file.)*
  - `simulator lang=spectre`
  - `global gnd!`
  - `Vdd (vdd! 0) vsource dc=3`
  - `Gnd (gnd! 0) vsource dc=0`
  - `v1 (A 0) vsource type=pulse val0=0 val1=3 rise=0.05n fall=0.05n width=10n period=20n`
  - `c0 (0 Y) capacitor c=3f`

  This assumes your input and output node are called "A" and "Y" and attaches a load capacitance to the output that simulates the input capacitance of gates attached to the output

node. For additional information about stimulus files, including notes on creating files with multiple inputs, see the *Guide to Writing Stimulus Files*.

- In the Virtuoso Analog Design Environment, include this new stimulus file by clicking Setup => Simulation Files and adding the name of the file in the "Stimulus File" box.

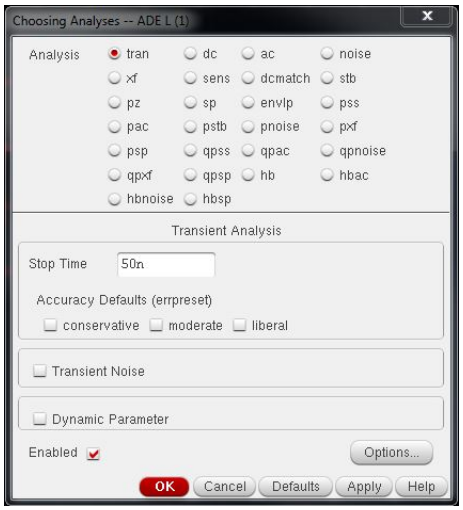
STEP 5. Setup Model Files:

- In Virtuoso Analog Design Environment, click on Setup => Model Libraries…
- If you have correctly set up your ECE410 Cadence environment, one Model Library File should already appear, "allModels.scs". If so, you may exit this dialog by pressing OK.
- You can add the necessary Model Library Files by
  - Click the bottom "Model Library File" box
  - Type "/opt/soft/NCSU-CDK-1.6.0.beta/MSU/allModel.scs"
  - Click the "Add" button. This should add the model to the Model Library File list and clear the Model Library File box
  - Your Model Library Setup dialog box should look like the one below. Once it does, you can click "OK" to close the dialog.
  - Alternatively, you could add the "ami06N.m" and "ami06P.m" model manually by typing "/opt/soft/NCSU-CDK-1.6.0.beta/models/spectre/nom/ami06N.m" and repeating the process for "/opt/soft/NCSU-CDK-1.6.0.beta/models/spectre/nom/ami06P.m"



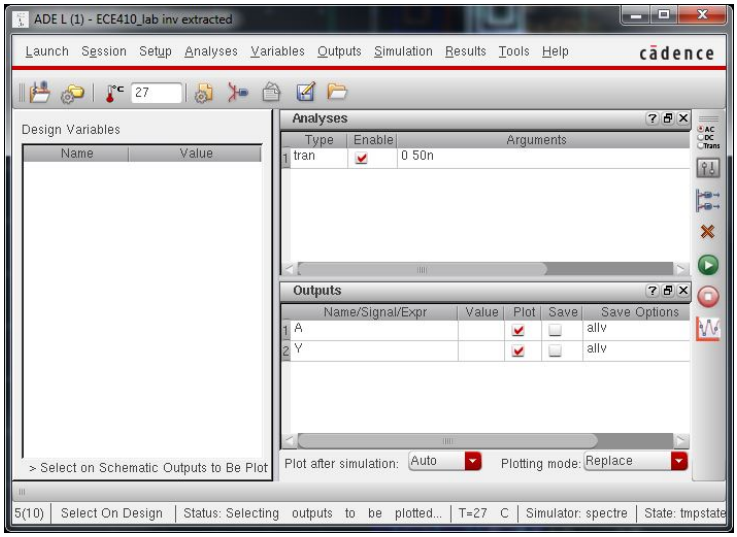
STEP 6. Setup Analysis

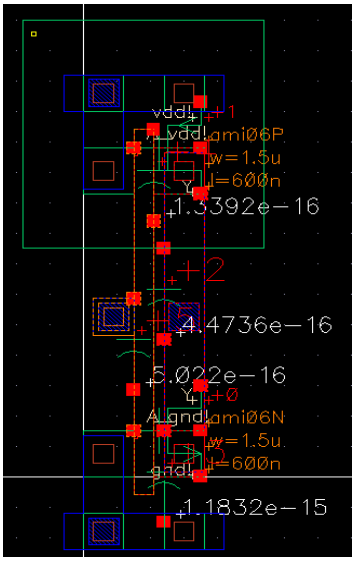
- In Virtuoso Analog Design Environment window, select Analyses => Choose.
- In the window that pops up, select **tran** to choose a transient analysis.
- Enter the time limits for simulation: Set the *Stop Time* to "**50n**".
- Choose Enabled at the bottom of the screen and press OK.



STEP 7. Setup output traces

- In Virtuoso Analog Design Environment window, select Outputs => to be plotted => Select on Schematic. This will activate the Layout Editing window with the extracted view of the inverter, allowing you to pick which signals (nets/wires) you would like to have plotted during the simulation.
- In the Layout Editing window select input gate poly and output metal1 (see example below).
- This will complete the simulation setup. Now your Virtuoso Analog Design Environment window should look as follows (*names may vary*):

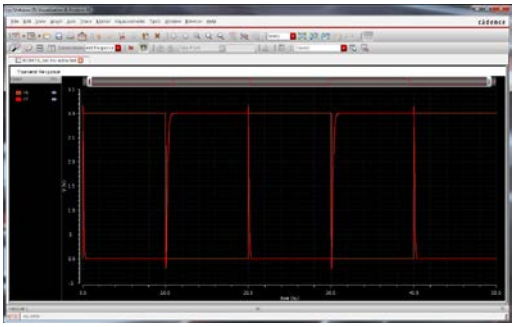




STEP 8. Run Simulation

- In the Virtuoso Analog Design Environment window select Simulation => Netlist and Run.
- When the simulation is complete, the CIW should show "Reading Simulation Data ..... Successful". If the simulation was not successful, go to Simulation => Output Log in your Virtuoso Analog Design Environment to find out what the problem was.

After a successful simulation, an output signal plot will pop up. As shown in the plot below, you should now see delays in the output signal due to the parasitics. If the simulated output waveform looks like the function you are expecting, you have probably done everything correctly. If not, check your steps and repeat until the correct output is obtained.

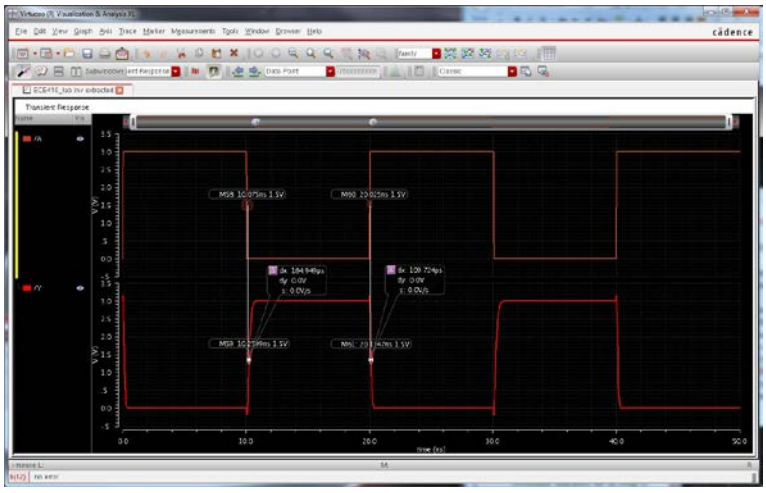


STEP 9. Measure Propagation Delay

- In the Waveform Window click on Graph => Split All Strips to separate input and output signals.
- Click on Marker => Create Marker (hotkey: m) and use them to measure the rising propagation delay and falling propagation delay.
- To obtain a plot with higher resolution, you can run the simulation again showing only 1 or 2 cycles, say with a stop time of 25nsec. Note: you can also use the Zoom tool to focus in on an area of interest in the plot.
- To make measurements with the markers, first you should locate where input signal (A) rises to 1.5V (half of VDD), move your cursor there and then press the "m" key. This creates a marker under your curser. Double click on the marker and change the Position to byYMode and change the value to 1.5V and click OK. Then move your cursor to where the output signal (Y) falls to 1.5V, and press "d". Double click on the marker and change the Position to byYMode and change the value to 1.5V and click OK. The delta value shown is the falling propagation delay time of your inverter. Use same method find out what the rising propagation delay time is. Record these values and use them to calculate the total propagation delay.

STEP 10. Measure Rise and Fall Times

- Measure and record the output rise time and fall time using the crosshair markers as in Step 8.



Rise time of the output is defined as the time taken for the output to rise from 10% of the final value to 90% of the final value (If the output rises from 0v to 3v, then rise time is the time for the voltage to change from 0.3v to 2.7v). Similarly the fall time of the output is defined as the time for the output signal to fall from 90% of the final value to 10% of the final value (If the output falls from 3v to 0v, then fall time is the time for the voltage to change from 2.7v to 0.3v).

DC Analysis

STEP 11. Setup Simulation

- Open a new text file (any file name is fine). Enter the following text, save the file and exit the text editor.

```
o  simulator lang=spectre
o  global gnd!
o  parameters vs=0
o  vdd (vdd! 0) vsource dc=3
o  Gnd (gnd! 0) vsource dc=0
o  v1 (A 0) vsource dc=vs
o  dcs dc param=vs start=0 stop=3 step=0.01
```

This assumes your input node is called "A". Note an output capacitance is not needed since we are doing a DC analysis and timing will not be considered. Instead a DC statement is needed.

line 2: the "parameters" statement declares a simulation variable called "vs", which is initialized to 0. This parameter will be used to sweep the dc value of the voltage at input node A. You can give this any name and starting value.

line 3: the standard definition of dc voltage "vdd!"

line 5: definition of a voltage source at the input node A. Notice that the dc voltage value is set to the variable "vs" as defined in line 2. This allows the value to be swept instead rather than being constant.

line 6: the DC sweep statement. The first field "dcs" is the name of the dc sweep (can be any alphanumeric name). The second field "dc" is required to specify the command. The third field "param=vs" specifies the parameter to be swept; in this case, it is the voltage at the inverter input. The fourth and fifth fields ("start" and "stop") specify the bounds of the sweep. The sixth field "step=0.01" specifies the sweep step interval. Decreasing/increasing this value will increase/decrease the dc operating point precision, but take more/less time to simulate.

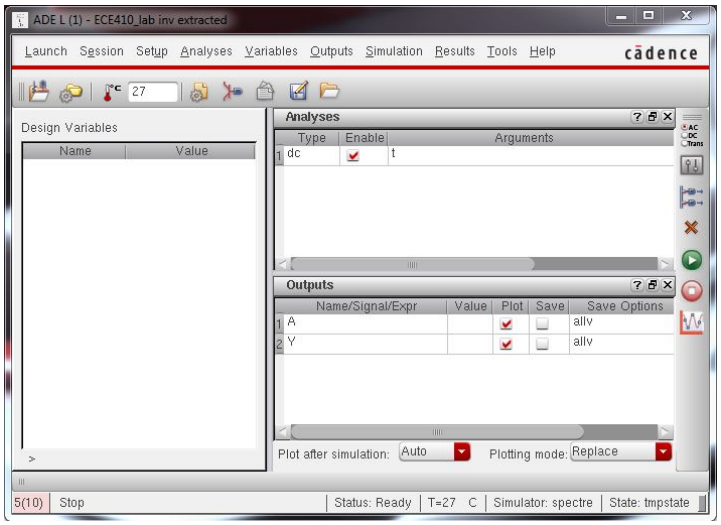
- In the Virtuoso Analog Design Environment, include this new stimulus file by clicking Setup => Simulation Files. If a file exists in the "Stimulus File" box, delete it. Then add the name of the new file in the "Stimulus File" box.

STEP 12. Setup Analysis

- In Virtuoso Analog Design Environment window, select Analyses => Choose.
- In the window that pops up, select **dc** to choose a DC analysis.
- Choose Save DC Operating Point and press OK.
- In the Virtuoso Analog Design Environment window, uncheck the "tran" Enable box.

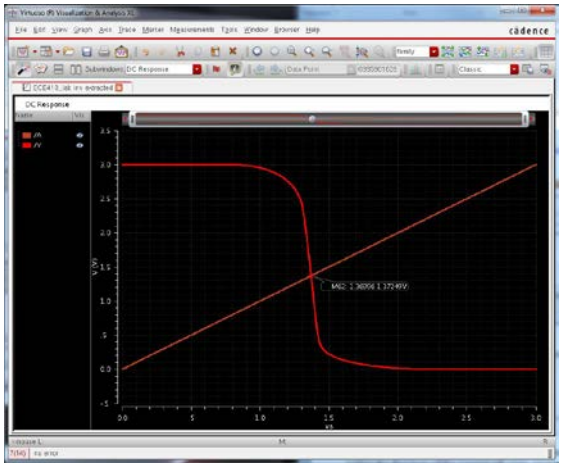
STEP 13. Setup Output Traces

- In Virtuoso Analog Design Environment window, (if necessary) select Outputs => to be plotted => Select on Schematic and pick the input and output nets again as you did for the transient analysis above. This will complete the simulation setup. Now your Virtuoso Analog Design Environment window should look like the window below.



<u>STEP 14.</u> Run Simulation

- In the Virtuoso Analog Design Environment window select Simulation => Netlist and Run.
- When the simulation is complete, the CIW should show "Reading Simulation Data ..... Successful". If the simulation was not successful, go to Simulation => Output Log in your Virtuoso Analog Design Environment to find out what the problem was.



After a successful simulation, an output signal plot will pop up showing the ***voltage transfer curve***. If the plot does not look like you would expect, check your steps and repeat until the correct output is obtained.

<u>STEP 15</u>. Measure DC Parameters

- Using the crosshair markers, measure the <u>switching threshold</u> (midpoint voltage), where the input voltage is equal to the output voltage.
- Measure the highest input voltage where the output voltage is high (3V) and the lowest input voltage where the output is low (0V).

<u>OPTIONAL</u>. Saving Simulation State

The Analog Design Environment state can be saved so that the settings do not need to be manually entered each time a design is simulated.

- To save the simulation state, in the Virtuoso Analog Circuit Design Environment window select Session => Save State



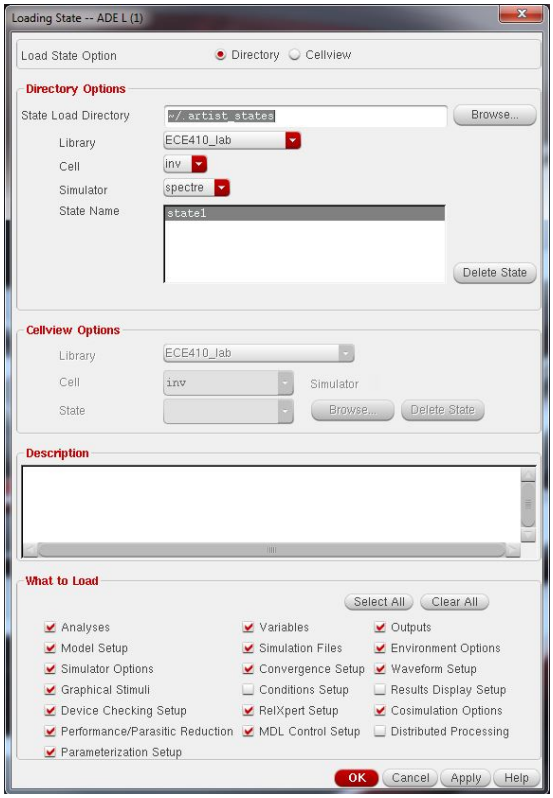
The "Save As" field does not have to be a unique name for all designs; the state is saved within the directory of the current cell view, so you can use the same Save As name for multiple cells without overwriting each other.. For example, cells named inv and nand2 can both independently have the state "state1" saved.

- Enter a Save As name, e.g., "state1" and click on "OK".

  Saving all simulation data can take a lot of memory so you may find it useful to alter the What to Save parameters to save only the items you need to run future simulatoins. Saving outputs from complex cells with multiple plotted node waveforms can generate very large files.

<u>OPTIONAL</u>. Loading Simulation State

- To load the saved state, after opening a specific cell, in the Virtuoso Analog Circuit Design Environment window select Session => Load State



- Select the desired State Name and click on "OK".

THE END