ECE410 Design Project-2014

- Deadlines & Milestones:
  - "Lab 8": (in lab progress check & proposal discussion).
  - Draft Proposals: Monday April 7, 2014 (in class)
  - Proposals: Wednesday, April 9th (in class) (final Proposal due)
  - Lab 9: by Friday April 11th (in lab check off, Phase 1)
  - Lab 10: by Friday April 18th (in lab check off, Phase 2)
  - Final Demo: by Thurs April 24 (in lab final project demo(s))
  - Teams: 15 min Design Project Presentations– Monday April 28th (starts at 10am, report due by 5pm)—Final Exam Day.
- submit reports electronically, in ms-word, file size less than 3MB. Final project (include all files) submission on a CD.
- Online Resources
  - Project Guide: Report and grading guidelines, etc.
  - Project Description: Design specifications.
- Extra Lab Time
- -no class on Fridays starting April 11th to allow more time for lab



Design Project Grading

- The combined components of the Design Project are worth 25% of your overall class grade.

- Design Project grade will be broken down as:
  - 10% Quality of Proposal (details)
  - 30% "Lab 8-10" Milestones Evaluations
  - 25% Final Project Demo Evaluation
  - 20% Report Quality (details)
  - 15% Individual Effort in the project/presentations



Project Proposal

- What is it?
  - A plan of action and organization of labor for the design project
- What's in the proposal
  - Description of design concept
    - show you have studied and planned the project
  - Division of labor
    - who will do what –specifically!
  - Work plan schedule –deadline for each task
- When do I start?
  - NOW! Read the project description, meet with your group, and start planning
  - Draft proposal due in 5 days
  - Start designing immediately. By the time the proposal is turned in, you should be well into the design phase (~20% done with whole project)



Project Proposal

- What to do for Labs 8-10
  - layout and final timing simulations will take a lot of time
    - don't leave all layout Lab 10!
  - example rough organization of tasks
    - planning and initial design approach, layout floorplan — **Proposal**
    - lower level cell design — **Labs 8-9**
      - schematic entry and functional simulation
      - layout, DRC, and LVS
    - higher level cell design
      - schematic entry and functional simulation
      - layout, DRC, and LVS
    - final cell layout/routing/LVS — **Lab 10**
    - final timing analysis — **Demo**
- General Comments
  - for a well-rounded experience, don't make one person do all of one thing, e.g., a layout guy.
  - simulations always take more time than you expect –plan on it!

Common Design Issues

- design hierarchy
  - not much transistor-level design required for design projects
    - should design at tx-level if you can save area and delay
  - MUST use instantiated cells at higher level
- instruction/function decoding
  - must use only the specified input control signals for all functions
- size/power/speed tradeoff 
  - make [redacted] the priority, discuss specific tradeoffs in report
- simulating worst case delays
  - measure from clock edge to mid-point of last output to change
- simulating power consumption
- LVS
  - passing LVS on all smaller cells will make final LVS much easier

Group Lab Comments

- Teamwork "professional skill"
  - valued by employers
- Organizing your team/group
  - divide and conquer to get started
    - plan who will do what, organize by email to reduce in-person demand
  - work together to learn from each other
    - after individual effort, meet as pairs or as 3 and have fun learning
- Dividing Work Load
  - divide by cells
  - divide by software tools
  - * don't assign report to one person
    - all should contribute, everyone needs experience writing
- Directory Permissions
  - anyone having trouble with permission issues?

