A programmable FIR Filter

Problem Statement:

Students in ECE 410 class, they will be challenged to design the schematic and physical layout of a programmable FIR filter. FIR "Finite Impulse Response" filters are one of two main types of digital filters used in Digital Signal Processing (DSP) applications (the other type being IIR). So, in this semester, a FIR filter will be designed and constructed in terms of power, area and also delay. The elementary structures of an FIR filter are a combination of multipliers and delays, which represent the combination of adders. However, adders serve as the basic components in the implementation of an FIR filter. Moreover, it is one of the fundamental arithmetic operations, used extensively in many VLSI systems such as microprocessors and application specific DSP architectures. It participates in many other useful operations such as subtraction, multiplication, division etc. Thus, a programmable FIR Filter will be implemented including “programming” (e.g. download/upload) memory tapes using CMOS circuitry and Cadence VLSI design tools.

Their Results will be judged on their ability to satisfy several competing goals:

1. Minimization of the total area
2. Power
3. Speed

Building Blocks

\[ y[n] = x[n] - n_d \]

\[ y[n] = x_1[n] + x_2[n] \]

\[ y[n] = B \cdot x[n] \]
\[ x[n] \xrightarrow{w_0} \]

Unit Delay

\[ x[n - 1] \xrightarrow{w_1} \]

Unit Delay

\[ x[n - 2] \xrightarrow{w_2} \]

Unit Delay

\[ x[n - n_d] \xrightarrow{w_{n_d}} \]

\[ y[n] = \sum_{k=0}^{n_d} w_k x[n - k] \]

Block Diagrams