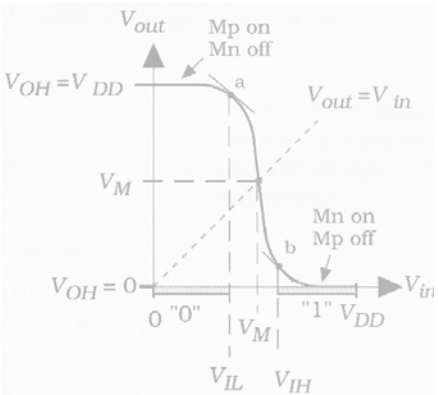
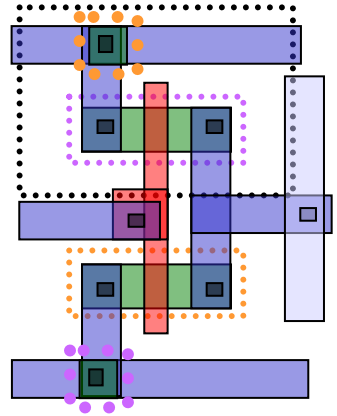
$$(a+b)\cdot(a+c) = a+a\cdot b+a\cdot c+b\cdot c$$
$$= a\cdot(1+b)+a\cdot c+b\cdot c$$
$$= a\cdot(1+c)+b\cdot c$$
$$= a+b\cdot c$$

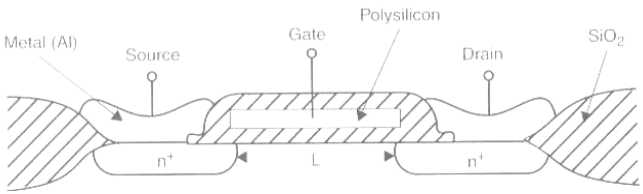


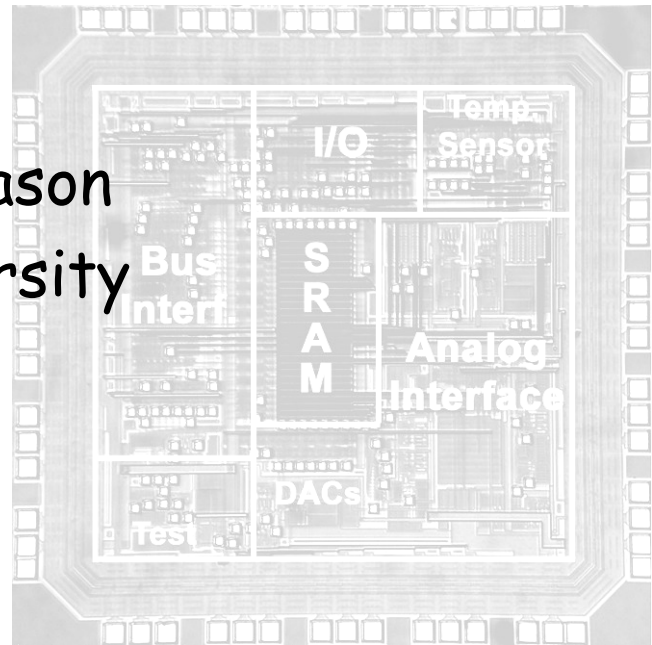


ECE 410: VLSI Design Course Introduction

Professor Andrew Mason
Michigan State University

Spring 2008





Electronics Revolution

- Age of electronics
  - microcontrollers, DSPs, and other VLSI chips are everywhere
- Electronics of today and tomorrow demand…
  - higher performance (speed) circuits
  - low power circuits for portable applications
  - more mixed signal emphasis
    - wireless hardware
    - high performance signal processing
    - sensors and microsystems

Digital Camera

PDAs

Camcorder

MP3/CD Player

Laptop

Cell phone

Handheld Games & Video Players

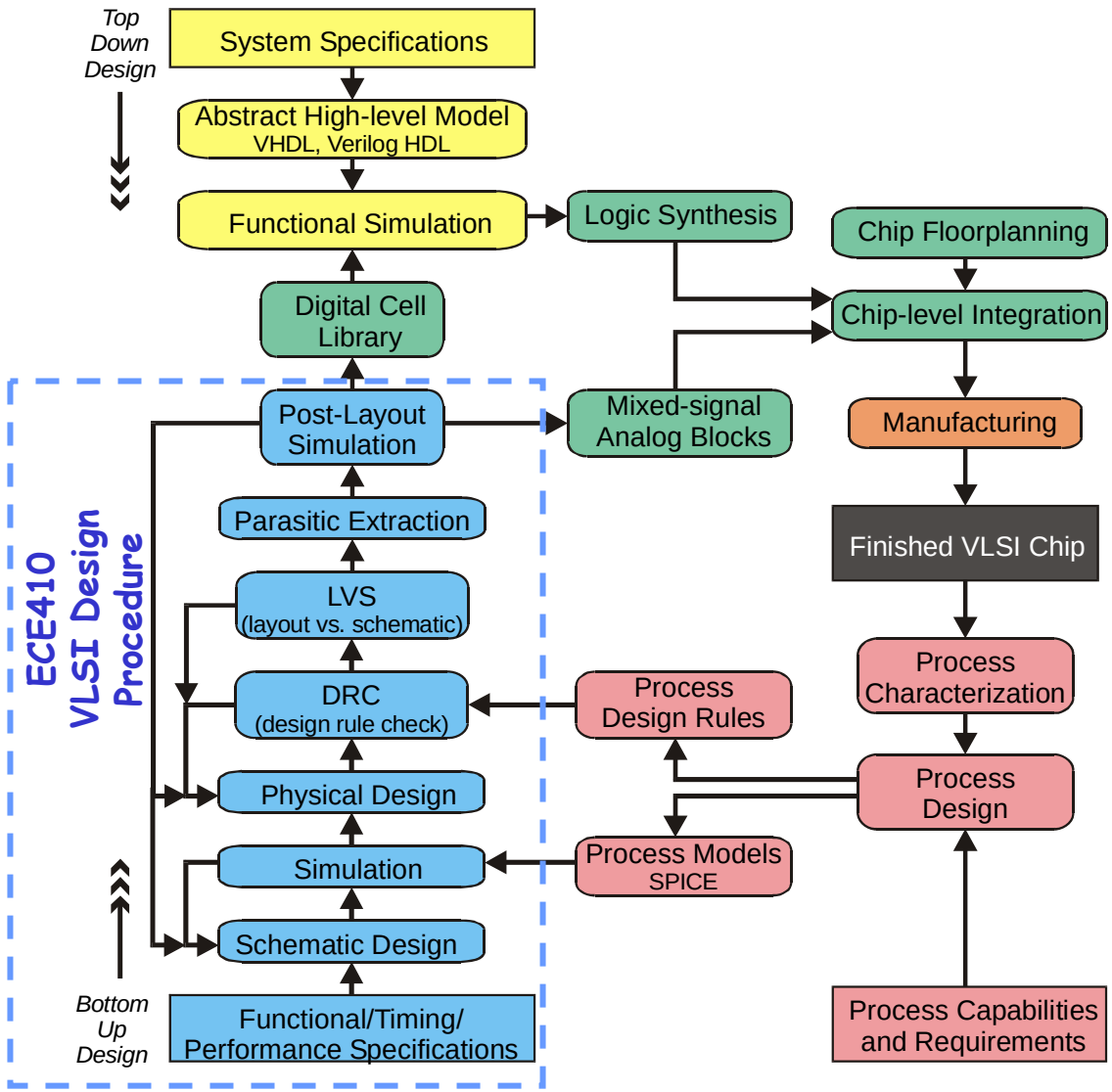
VLSI Design Flow

VLSI = very large scale integration
- lots of transistors integrated on one chip

Chip Development Cycle

Design Methodologies

- Top Down Design
  - coded circuit functionality for rapid design
  - digital only
  - covered in ECE 411
- Bottom Up Design
  - transistor-level design with focus on circuit performance
  - digital & mixed signal
  - covered in ECE 410



410 Course Objectives

- Understand and Experience VLSI Design Flow
- Learn Transistor-Level CMOS Logic Design
- Understand VLSI Fabrication and Experience CMOS Physical Design
- Learn to Analyze Gate Function and Timing Characteristics
- Study High-Level Digital Functional Blocks
- Visualize CMOS Digital Chip Design

410 Syllabus

- **Instructor**: Dr. Andrew Mason, EB 1217, mason@egr.msu.edu
- **Lecture:** MWF, 11:30 12:20, 1145 Engineering Bldg
- **Office Hrs.**: Wed: 10-11:30, or send email for an appointment
- **Lab:** Labs are open; you will not be "attending" a lab at the lab time you enrolled up for
- **Lab TA/Instructor Email:** ece410ta@egr.msu.edu
  This email alias for the instructor and TAs should be used for all general lab/project questions so that the first person available can answer your question.
- **Lab/TA Hours:**
  You may work on your assignments in any available PC lab any time you wish. TAs will be available to answer questions at designated times that will be posted on the class website.
- **Course Website:** www.egr.msu.edu/classes/ece410/mason/
- **Email:** Please check/forward your EGR email

410 Syllabus

- **Textbook:**
  J. Uyemura, Introduction to VLSI Circuits and Systems, Wiley, 2002. ISBN 0-471-12704-3
  - textbook has good examples; some homework problems from textbook

- **Attendance and Conduct in Class:**
  Students are expected to attend class and be bright and cheerful with lots of questions. It will be difficult to perform well in this class without attending the lectures. It is the student's responsibility to get notes and handouts for any missed class.

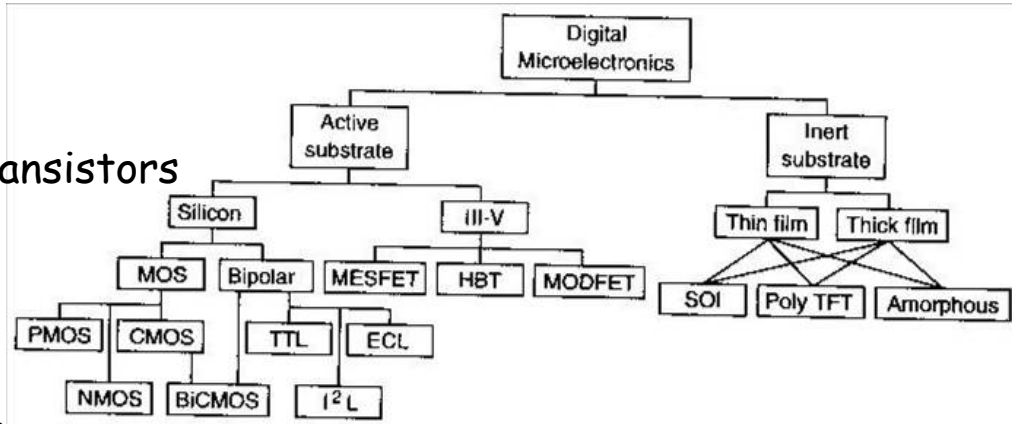
- **Grading:**
  30% 2 Midterm Exams
  15% Homework *
  5% Participation (attendance, quizzes, etc.) *
  25% Lab Assignments (Lab 1-7) *
  25% Design Project (Labs 8-10, Proposal, Project Demo, Project Report)
  **** must obtain a grade of 60% or better to pass the course***
  Tentative dates for the two midterm exams are shown on the Course Topic Outline (also posted on the web). There is no final exam, only a final design project. Ten homework assignments will be due weekly before class on Wednesdays. Approximately 10 5-minute quizzes will be given at the beginning of class on random days.

410 Lab Issues

- When can I work on lab assignments?
  - open lab, work in any PC lab when you want
  - TAs will be in lab at set times each week to assist you
    - schedule will be posted on the class website
- Who is the TA?
  - Zeyong Shan: lab hours & lab grader
- What's the lab process?
  - assigned each week on a Friday
  - in-lab check off by the next Friday
    - must show/demonstrate specific results to TA
  - lab reports due in class on Monday
    - see format/sample on the class website
- When will labs begin?
  - first assignment next Friday –need to learn stuff in class first

Integrated Circuit Technologies

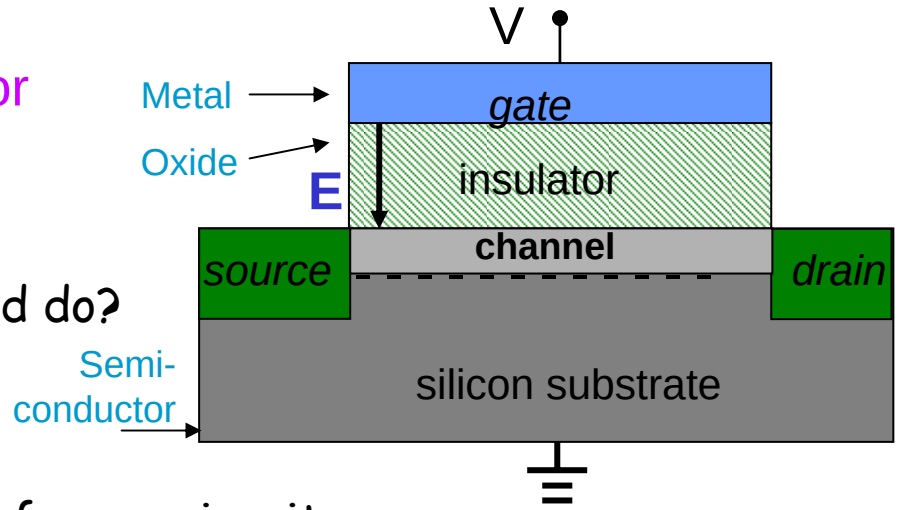
- "Technologies" for digital ICs
  - passive (inert) circuits:
    - resistors and capacitors only, no transistors
  - active circuits; with transistors
    - III-V devices (compound semic.)
    - MOS and Bipolar devices (silicon)



- ECE410 will cover CMOS because…
- CMOS dominates the semiconductor/IC industry
  - **Silicon is cheaper** ➔ preferred over other materials
  - **physics** of CMOS is **easier** to understand
  - CMOS is **easier to implement/fabricate**
  - CMOS provides **lower power-delay product**
  - CMOS is **lowest power**
  - density: can get **more** CMOS transistors/functions **in same chip area**
- **BUT!** CMOS is not the fastest technology!
  - BJT and III-V devices are faster

What is a MOSFET?

- Digital integrated circuits rely on transistor switches
  - most common device for digital and mixed signal: MOSFET
- Definitions
  - MOS = Metal Oxide Semiconductor
    - physical layers of the device
  - FET = Field Effect Transistor
    - What field? What does the field do?
    - Are other fields important?
  - CMOS = Complementary MOS
    - use of both nMOS and pMOS to form a circuit

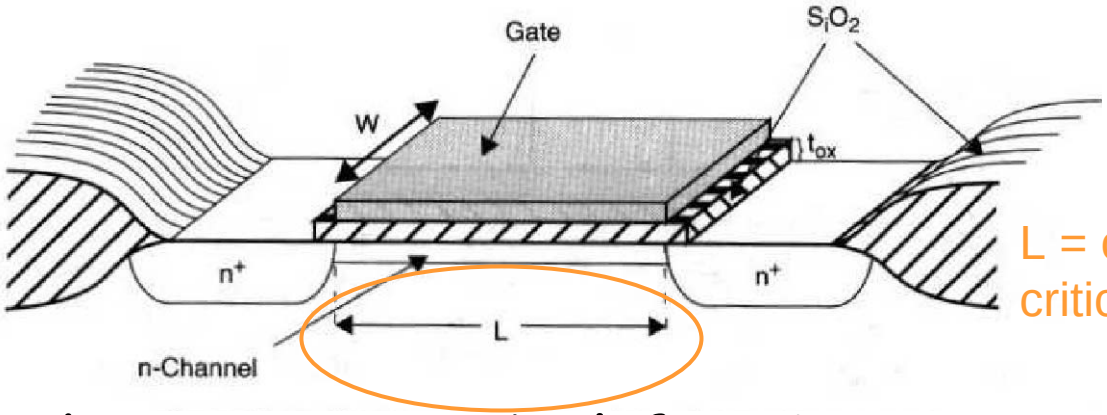


- Primary Features
  - gate
  - gate oxide (insulator)
  - source and drain
  - bulk/substrate
  - channel

NOTE: "metal" is replaced by polysilicon in modern MOSFETs

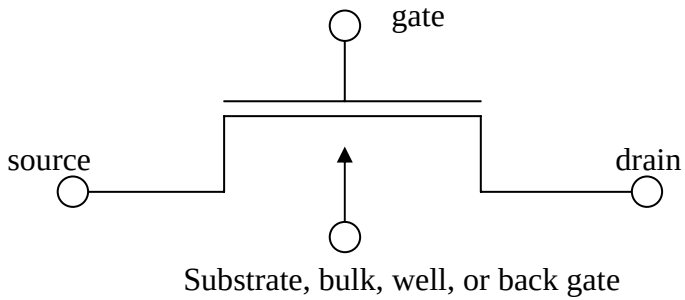
MOSFET Physical View

- Physical Structure of a MOSFET Device

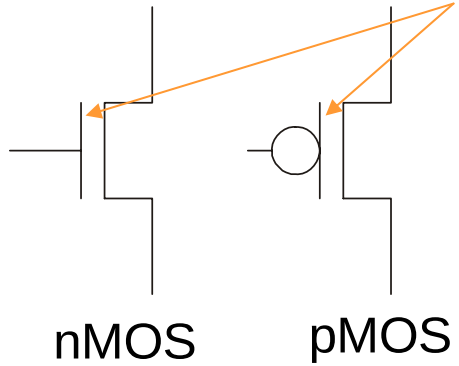


L = channel length
critical dimension = "feature size"

- Schematic Symbol for 4-terminal MOSFET



- Simplified Symbols



note: no physical connection at Gate terminal, symbolic of gate insulator in MOSFET

CMOS Cross Section View

- Cross section of a 2 metal, 1 poly CMOS process

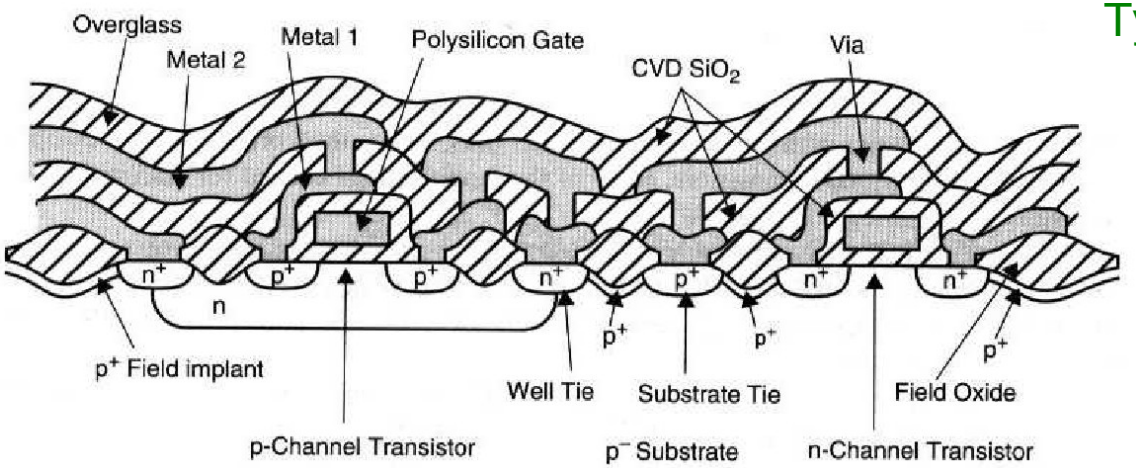
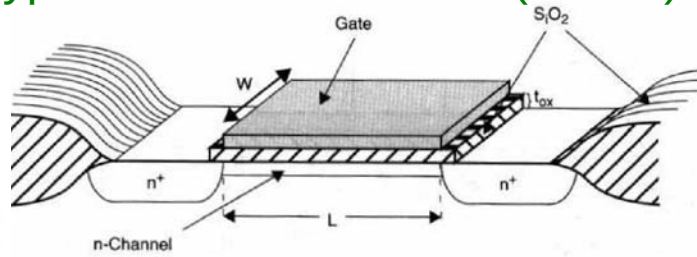
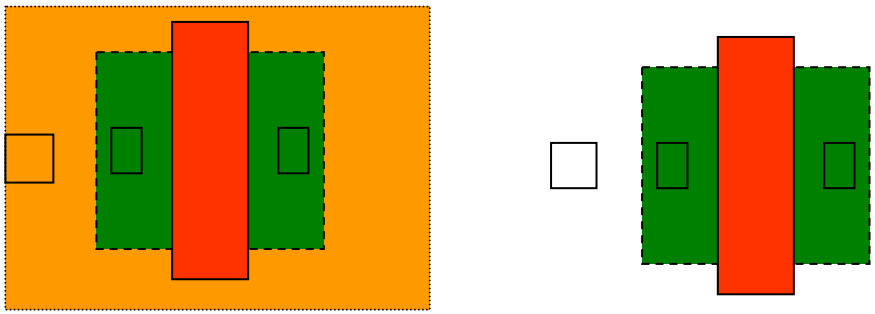


Figure 2.11 The final cross section of a CMOS microcircuit with two layers of metal.

Typical MOSFET Device (nMOS)

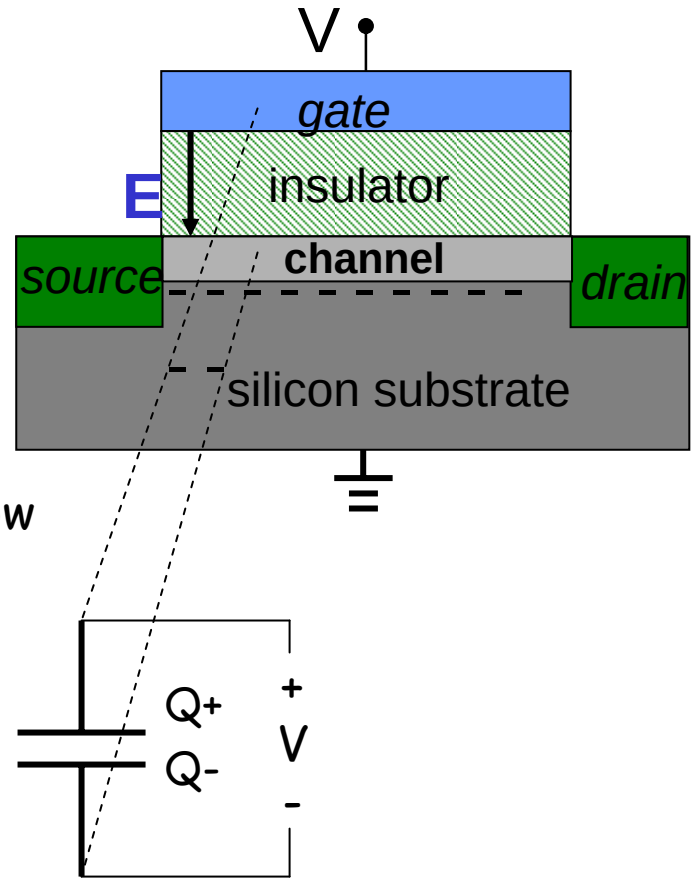


- Layout (top view) of the devices above (partial, simplified)



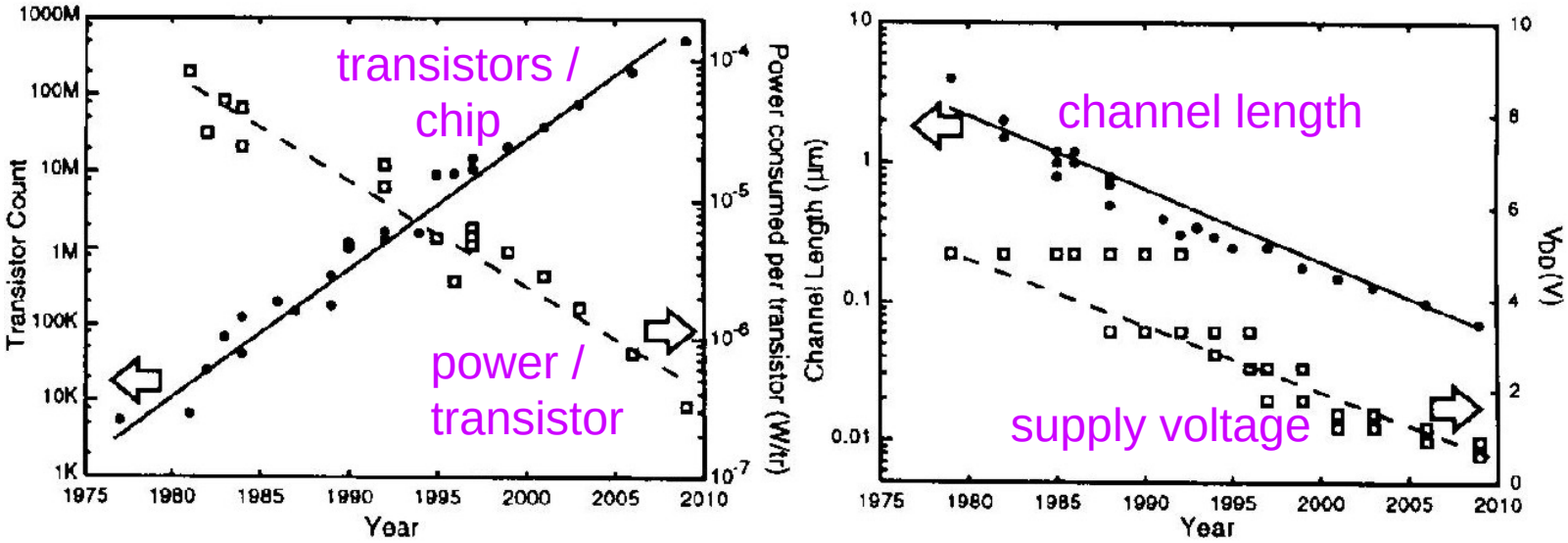
Fundamental Relations in MOSFET

- Electric Fields
  - fundamental equation
    - electric field: E = V/d
  - vertical field through gate oxide
    - determines charge induced in channel
  - horizontal field across channel
    - determines source-to-drain current flow
- Capacitance
  - fundamental equations
    - capacitor charge: Q = CV
    - capacitance: C = ε A/d
  - charge balance on capacitor, Q+ = Q-
    - charge on gate is balanced by charge in channel
    - what is the source of channel charge? where does it come from?



CMOS Technology Trends

- Variations over time
  - # transistors / chip: increasing with time
  - power / transistor: decreasing with time (constant power density)
  - device channel length: decreasing with time
  - power supply voltage: decreasing with time



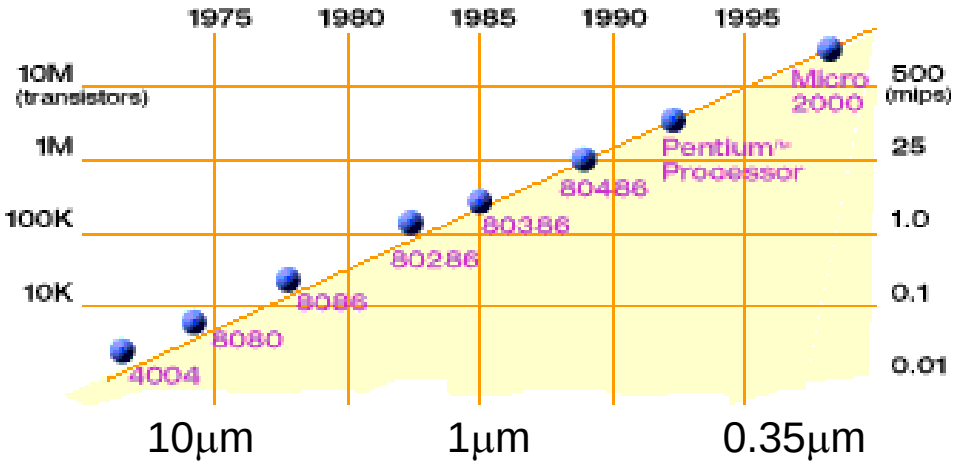
rref: Kuo and Lou, Low-Voltage CMOS VLSI Circuits, Fig. 1.3, p. 3

low power/voltage is critical for future ICs

Moore's Law

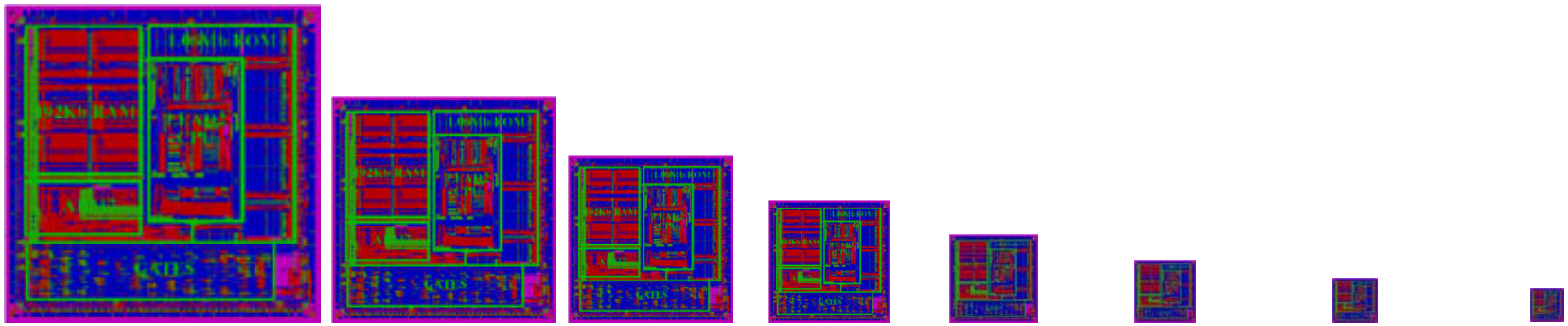
- In 1965, ***Gordon Moore*** realized there was a striking trend; each new generation of memory chip contained roughly ***twice as much capacity*** as its predecessor, and each chip was released within ***18-24 months*** of the previous chip. He reasoned, computing power would rise exponentially over relatively brief periods of time.

- Moore's observation, now known as ***Moore's Law***, described a trend that has continued and is still remarkably accurate. ***In 26 years*** the number of transistors on a chip has increased more than ***3,200 times***, from 2,300 on the 4004 in 1971 to 7.5 million on the Pentium¨ II processor in 1998.



(ref: http://www.intel.com/intel/museum/25anniv/hof/moore.htm)

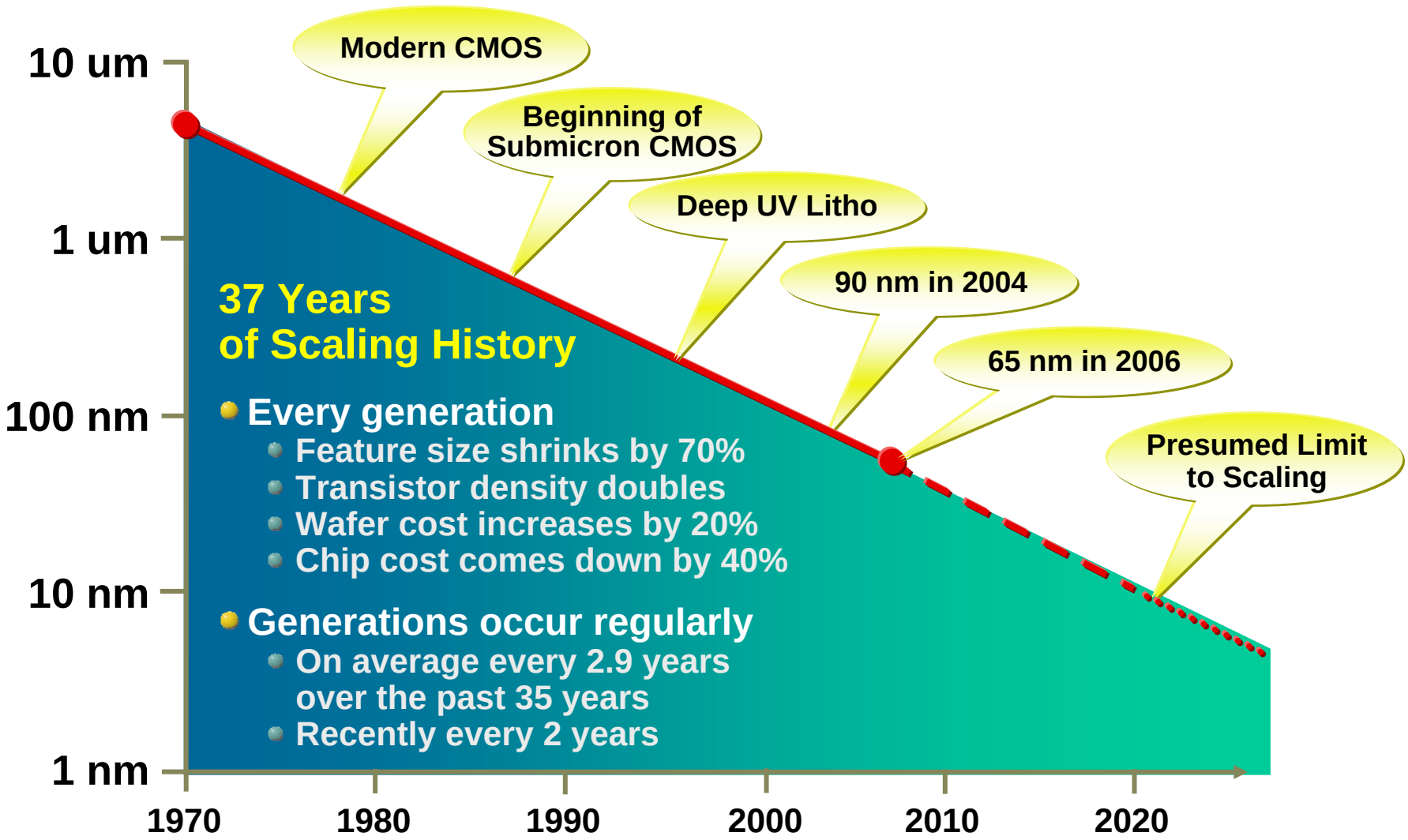
GSM Digital Baseband Evolution



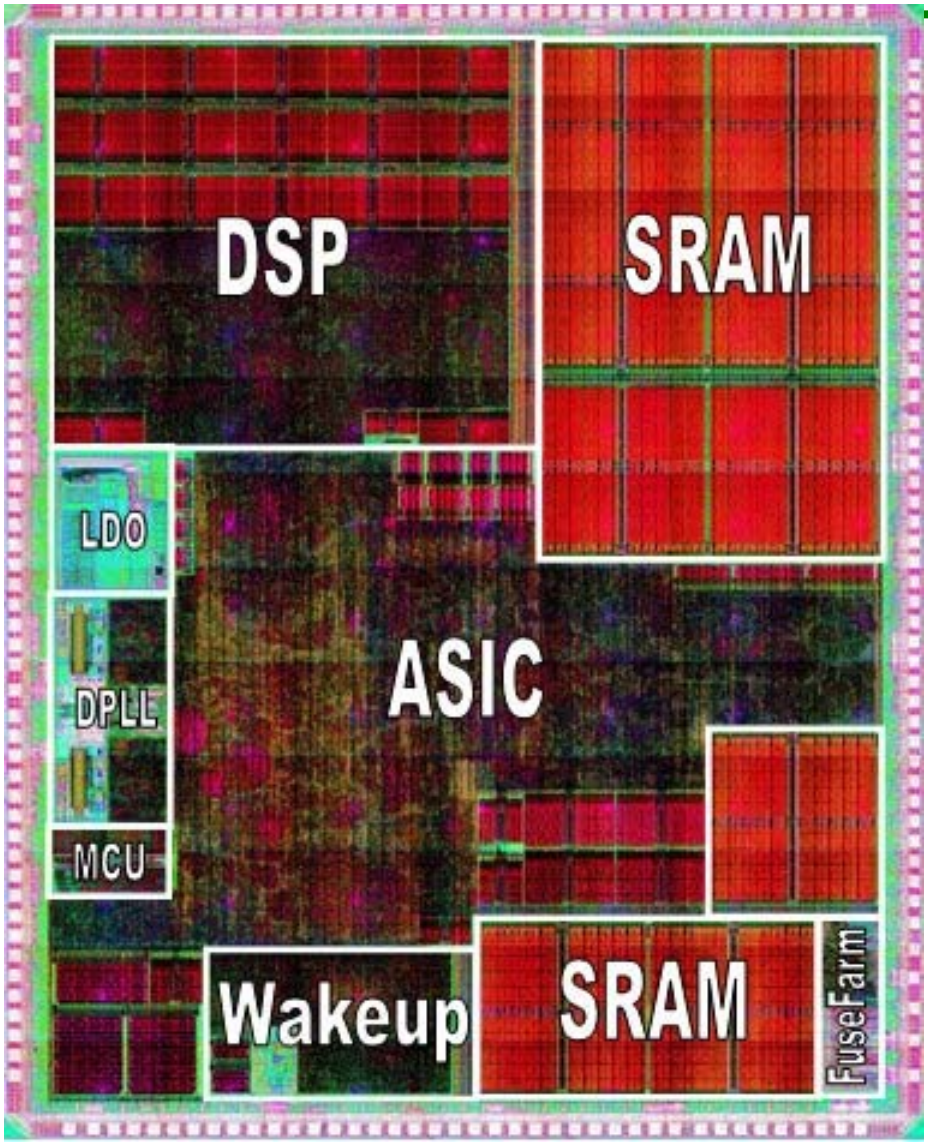
Year	1994	1997	1999	2000	2002	2004	2006	2008
Nano-meter	500nm	350nm	250nm	180nm	130nm	90nm	65nm	45nm
Wafer size	6"	8"	8"	8"	12"	12"	12"	12"
Die size (mm^2)	80.7	46.6	19.2	10.7	6.7	4.2	2.4	1.4
Dies per wafer	310	950	2550	4700	12,200	18,700	26,500	46,500

150X increase in die per wafer

Semi-Conductor Scaling



Example 65 nm Product: DSP chip



Features:

- Die Size: 13.3mm^2
- 5.9M bits SRAM
- 1.9M gates of logic
  - eFuse (dieID) and repair
  - ARM7 uC
  - LEAD3 DSP (250K gates)
  - MegaCell (300K gates)
  - ASIC gates (1.3M gates)
- In Volume Production

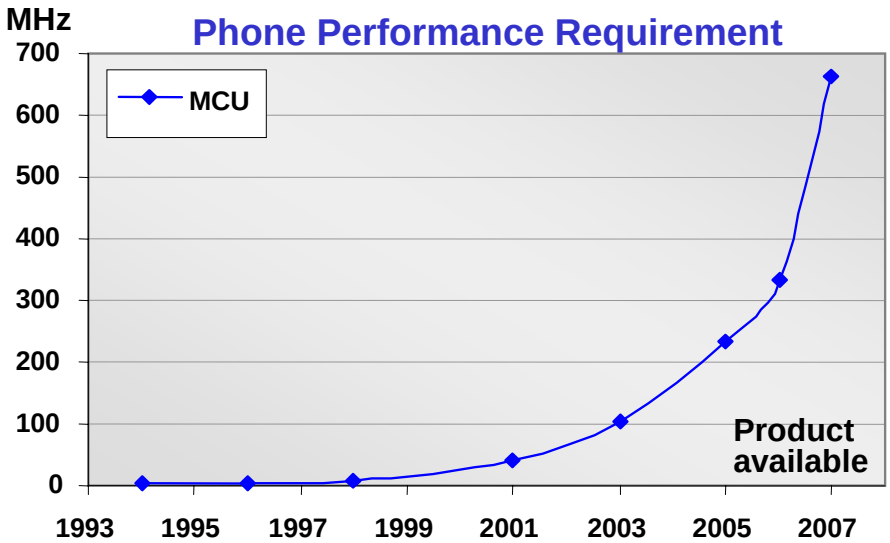
The Impending Constraint: Power Consumption

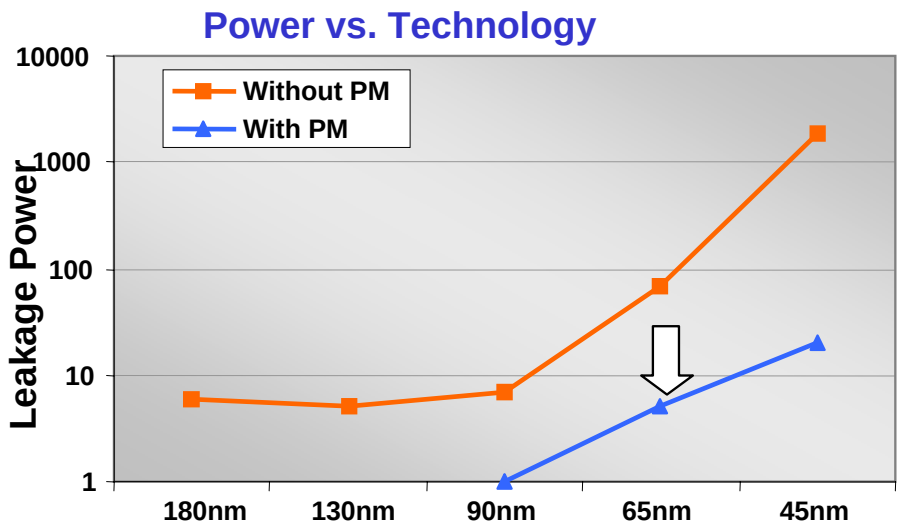
Pwr_Active = Cap*Voltage^2*Freq + Leakage

- Cap: Decrease with technology advance
- Voltage: Nearly constant, possibly at minimum now
- Freq: Increases with technology advance
- Leakage: Increases with technology advance & with temperature (caused by higher power)

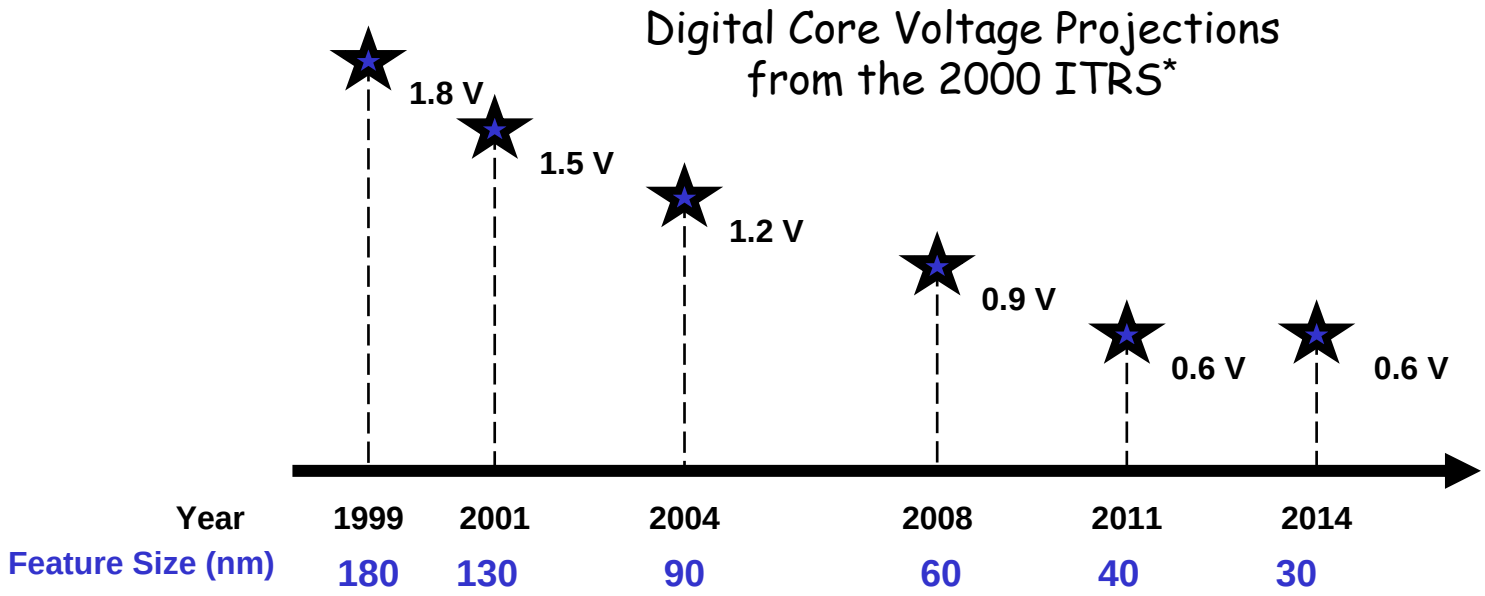
Pwr_Idle = Leakage

- Leakage: Increases with technology advance & with temperature





Power Supply Trends



* http://public.itrs.net/Files/2000UpdateFinal/ORTC2000final.pdf

- Data from projections in 2000
- Actually
  - reached 65nm in 2006 and 45nm in 2008, way ahead of projections