ECE410 **VLSI Design** **Spring 2007**

Lecture: MWF, 11:30 12:20, 1145 Engineering Bldg
Lab: Labs are open; ***lab times on the enrollment schedule have no significance***.

Instructor: Dr. Andrew Mason, EB 1217, mason@egr.msu.edu

Office Hrs.: Mon: 5-6pm (discussion session), Wed: 10:00-11:30
or send email for an appointment

410 Lab TA: Casey Wallace, walla118@egr.msu.edu
TBA

Lab TA/Instructor Email: ece410ta@egr.msu.edu
This address will go to all of the people above and should be used for all general lab/project questions so that the first person available can answer your question. For questions related to homework, please email Dr. Mason directly; the TAs do not deal with homework.

Lab/TA Hours:
You may work on your assignments in any available UNIX lab any time you wish. TAs will be available to answer questions at designated times that will be posted on the class website.

Course Website: http://www.egr.msu.edu/classes/ece410/mason/
A significant amount of material for this class will be posted on the course website, including assignments, lab tutorials, and lecture notes.

Student Email: ece410all@egr.msu.edu
We will send email to the entire class using the above alias, which points to your *egr* email account. Please be sure to check your *egr* email this semester.

Prerequisite: ECE 230, 302, and 303

Required Text:
J. Uyemura, Introduction to VLSI Circuits and Systems, Wiley, 2002. ISBN 0-471-12704-3

Reference Texts:
Weste and Harris, CMOS VLSI Design, 3rd Ed., 2005, ISBN 0-321-14901-7
K. Martin, Digital Integrated Circuit Design, 2000, ISBN 0-19-512584-3
Baker, Li, Boyce, CMOS Circuit Design, Layout, and Simulation, IEEE Press, 1998.

Catalog Description:
Digital integrated circuit design fundamentals. Design specifications: functionality, performance, reliability, manufacturability, testability, cost. Standards, silicon compilers, foundries. Design layout rules, rule checking. Circuit extraction, simulation, verification. Team-based design.

Attendance and Conduct in Class:
Students are expected to attend class and be bright and cheerful with lots of questions. It will be difficult to perform well in this class without attending the lectures. It is the student's responsibility to get notes and handouts for any missed class.

Grading:
30% 2 Midterm Exams
15% Homework *
5% Participation (attendance, quizzes, etc.) *
25% Lab Assignments (Lab 1-7) *
25% Design Project (Labs 8-10, Proposal, Project Demo, Project Report)
**** must obtain a grade of 60% or better to pass the course***

Tentative dates for the two midterm exams are shown on the Course Topic Outline (also posted on the web). There is no final exam, only a final design project. Ten homework assignments will be due weekly before class on Wednesdays. Approximately 10 5-minute quizzes will be given at the beginning of class on random days.

Lab Assignments and Lab Project:
Lab Assignments using the Cadence VLSI design software (available in all Engineering UNIX labs) will be an integral part of this course. Lab components make up 50% of your grade. ***There are no set lab times***, but the UNIX lab in EB 2200 will be reserved for ECE410 during several 3-hour blocks. During these times a TA will be available to help answer questions. Details of each assignment will be posted on the course website. Each student will have a UNIX class directory at ***/egr/courses/personal/ece410/<username>.***

Weekly Lab Assignment will have an in-lab check off with a TA that must be completed by 5pm on Friday of the week due. Reports will include specific deliverables which must be turned in before class on Monday. There will be 7 "normal" lab assignments plus 3 labs associated with the team-based design project. Each normal lab is worth 20 points, 5 assigned to the check off and 15 to the report. Report grades will be evaluated by your TA and based 60% on the quality of your lab work and 40% on the quality and completeness of your report. The design project will be done in 2-3 person groups and grades will be assigned according to the following breakdown.

10% Proposal 30% Labs 8-10 30% Project Demo 10% Individual 20% Report

Other Policies:
- Cheating in any form will not be tolerated! This includes copying homework, copying circuit design files, cheating on exams, or any other form of unethical behavior.
- There is no makeup for missed quizzes. If you have an excusable absence and notify the instructor by email before class begins, missed quizzes will not count against your grade.
- Homework can be done in groups but must be turned in individually. Direct copying of homework will result in a zero-point score for all people involved.
- Homework must be turned in at the beginning of class on the date it is due (generally Wednesdays). ***No late homework will be accepted.***
- Lab check offs and reports must be completed by their due data. Extensions for extreme situations should be arranged with the instructor.
- Makeup exams will only be allowed for excused absences and only when the instructor is informed before the exam. Makeup exams will be oral exams given after the exam date.