3/28/12 - Please turn in your check-ins and take a HW#8 assignment & Midterm 2 Extra credit assignment.

Reminders:
- No lecture this Fri (3/30)

LAB DAY

- Final Proposal is due on Mon
- Lab 8 check-off (20% of overall Final Project) by Fri @ 4PM

Announcement: We will skip over and return to signed multiplication, so that we have more time today to cover SRAM, which is more critical to your final projects.

WARM UP: What is the advantage of CSAs when summing 3 or more numbers?

- Reduces delay through multiple adder stages by only ripple-summing the carry in the last stage.

Chapter 13: Memories and Programmable Logic

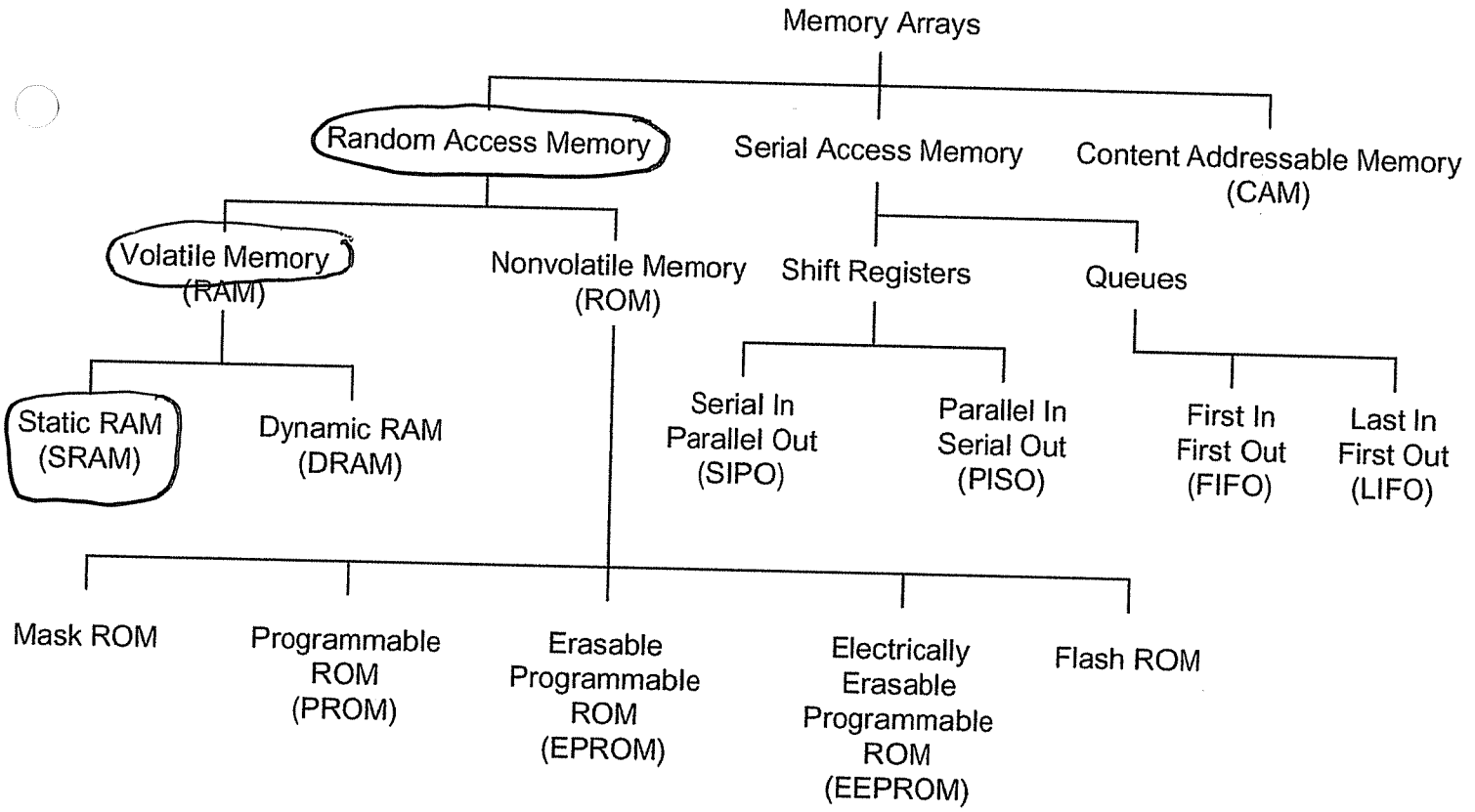
13.1 The Static RAM

Random Access Memory – accessed with an address, has a latency independent of the address (access as needed)

Misleading acronyms:

RAM – is a type of Random Access Memory that has read/write capability, and is volatile – data is only held as long as power is applied.

ROM – *read-only memory*, nonvolatile memory that holds data indefinitely. Misleading, since many ROMs can be written as well.



Volatile memories can be further divided into *static* and *dynamic* structures.

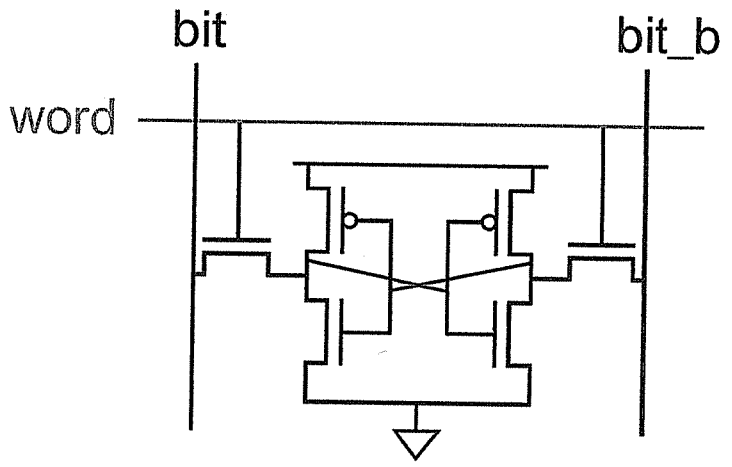
Static (SRAM) – use some form of feedback to maintain their state
Dynamic (DRAM) – use charge stored on a floating capacitor through an access transistor. Leakage requires that dynamic cells be periodically read and rewritten to refresh their state
SRAM are faster and easier to use than DRAM, but require more area per bit.

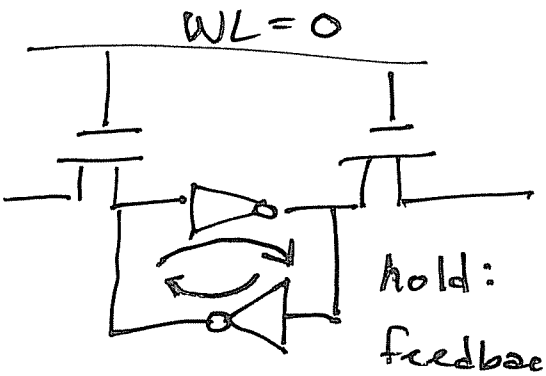
Memory cells have one or more **ports** for access. In read/write memory, each port can be *read-only, write-only* or capable of both *read* and *write.*

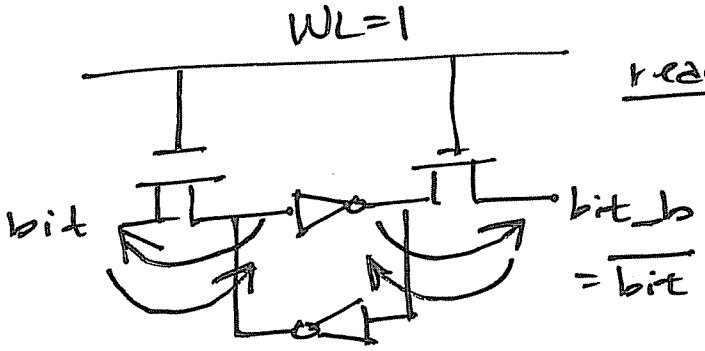
An SRAM cell function: read and write data, and hold the data as long as power is applied. SRAM are used preferentially over flip-flops, since they are much smaller. They achieve the small size at the expense of more complex peripheral circuitry to read and write the cells, but for large RAM arrays this is a good trade-off.

SRAMs have three operational modes:
Hold: the value of the bit is stored for future use
Write: a logic 0 or 1 is fed to the cell for storage
Read: the value of the stored bit is transmitted out

SRAM Basic structure: Six Transistor (6T) design:





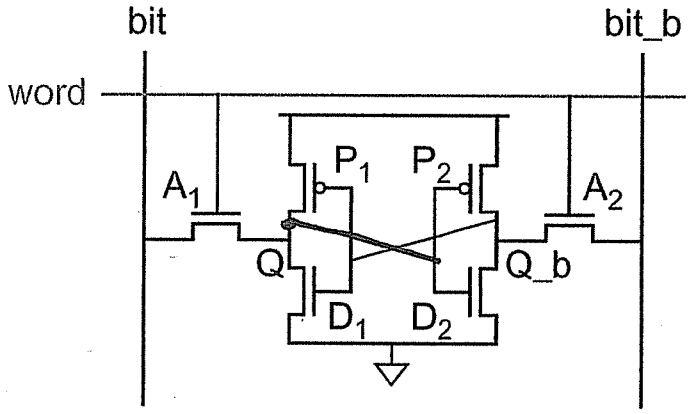


read: bit ? bit_b
take
value from
latch

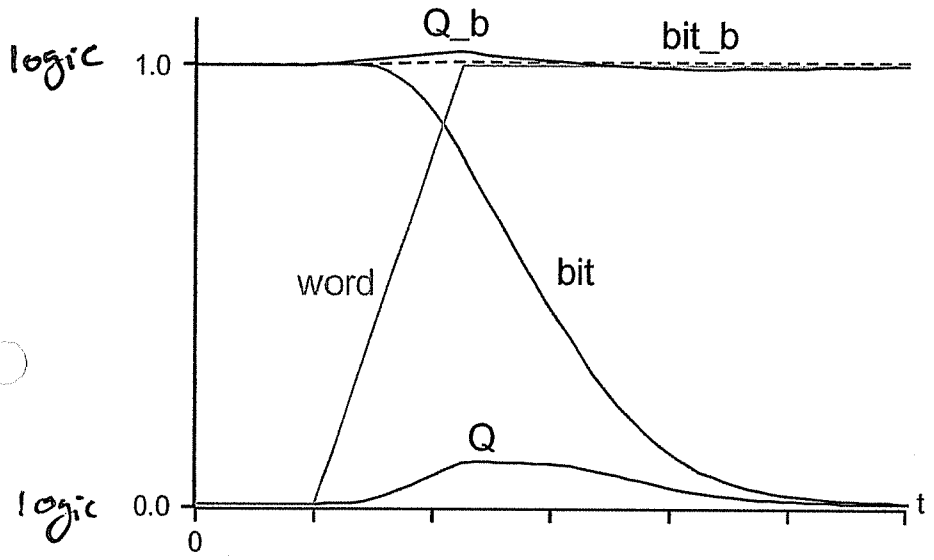
write: latch takes value
from bit and bit_b

Key design challenge: Sizing the transistors appropriately to achieve both read AND write capabilities.

Read: Consider first a read operation, where both bitlines are precharged high, so *bit* is initially at 1, and $Q = 0$. The trick is to make sure Q STAYS at 0 even though it is initially exposed to $bit = 1$. *bit* will flow current through Q as it discharges. Q will rise a little as a result. It needs to not rise *too much.* How much is too much? It needs to stay below the switching threshold of the second inverter.



(a)

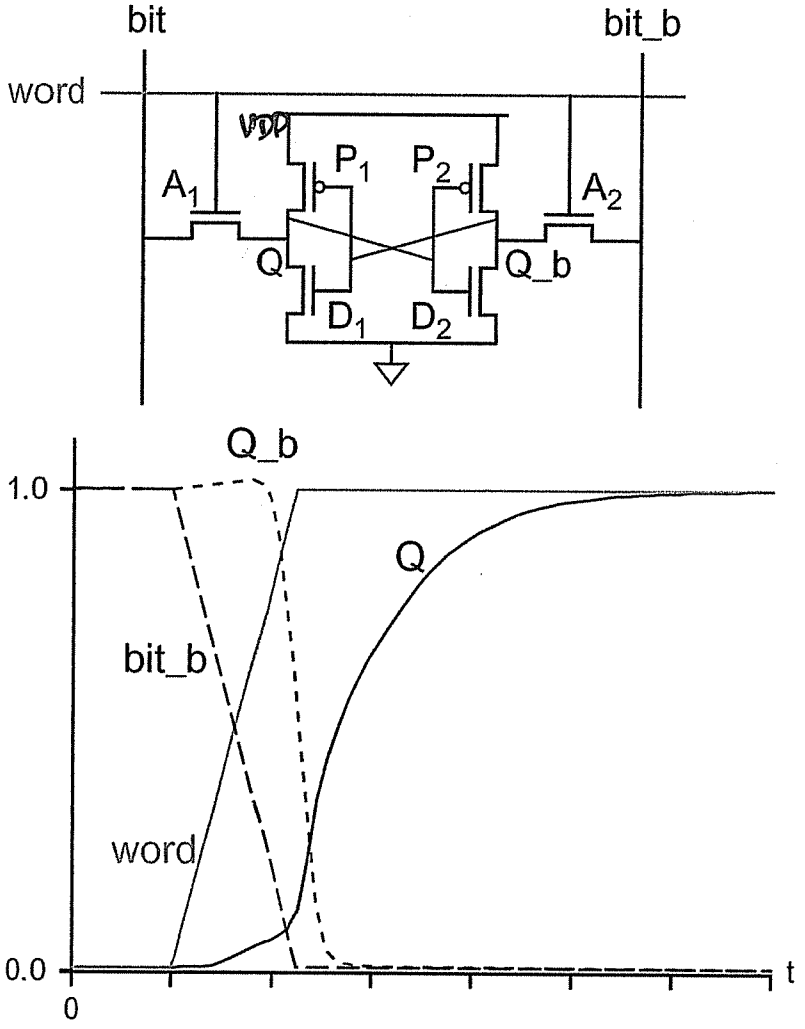


(b)

Q is held low by *D1* but pulled high by current flowing through *A1*. As a result, the driver *D* must be stronger than the access transistor *A*.

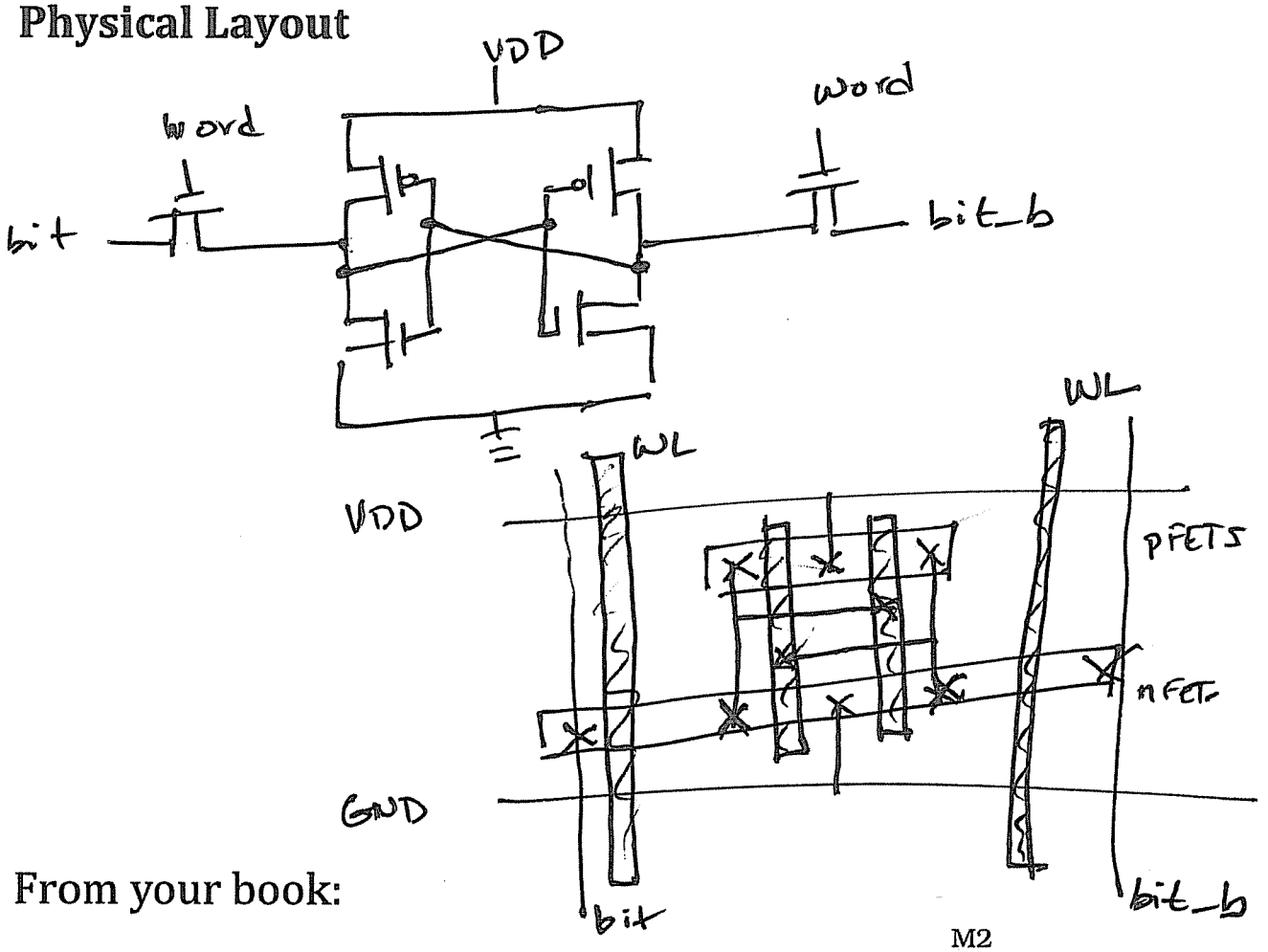
read capability: D > A

Write: In order for the cell to be read stable, we know that *bit* will be unable to force Q high through $A1$. Therefore, the cell must be written by forcing Q_b low through $A2$. The transistor $P2$ will oppose this operation, so therefore $A2$ needs to be stronger than $P2$. When Q_b falls low, $D1$ will turn off, allowing Q to be pulled high.

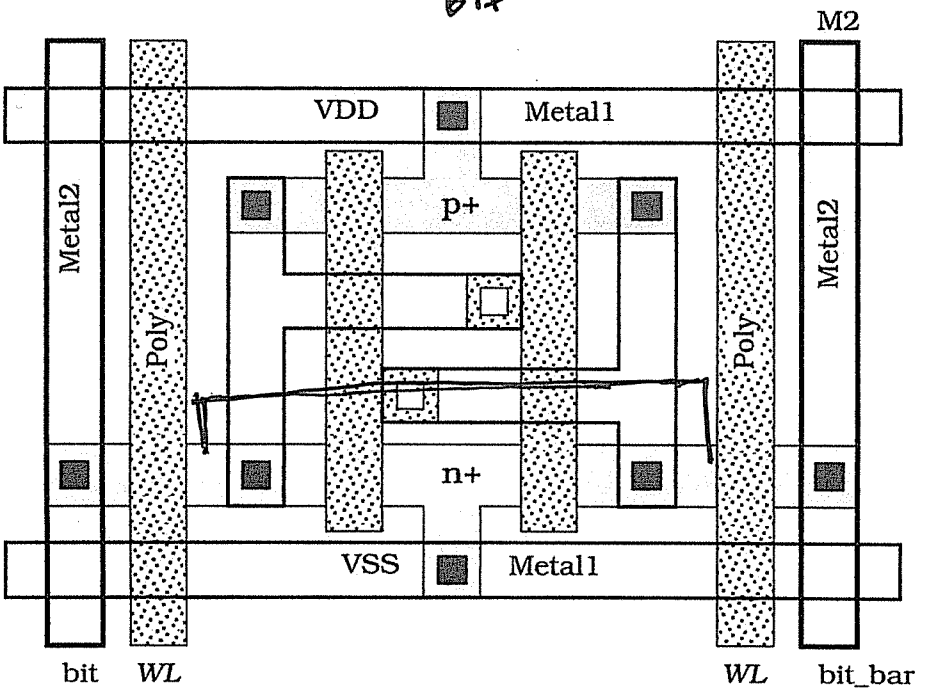


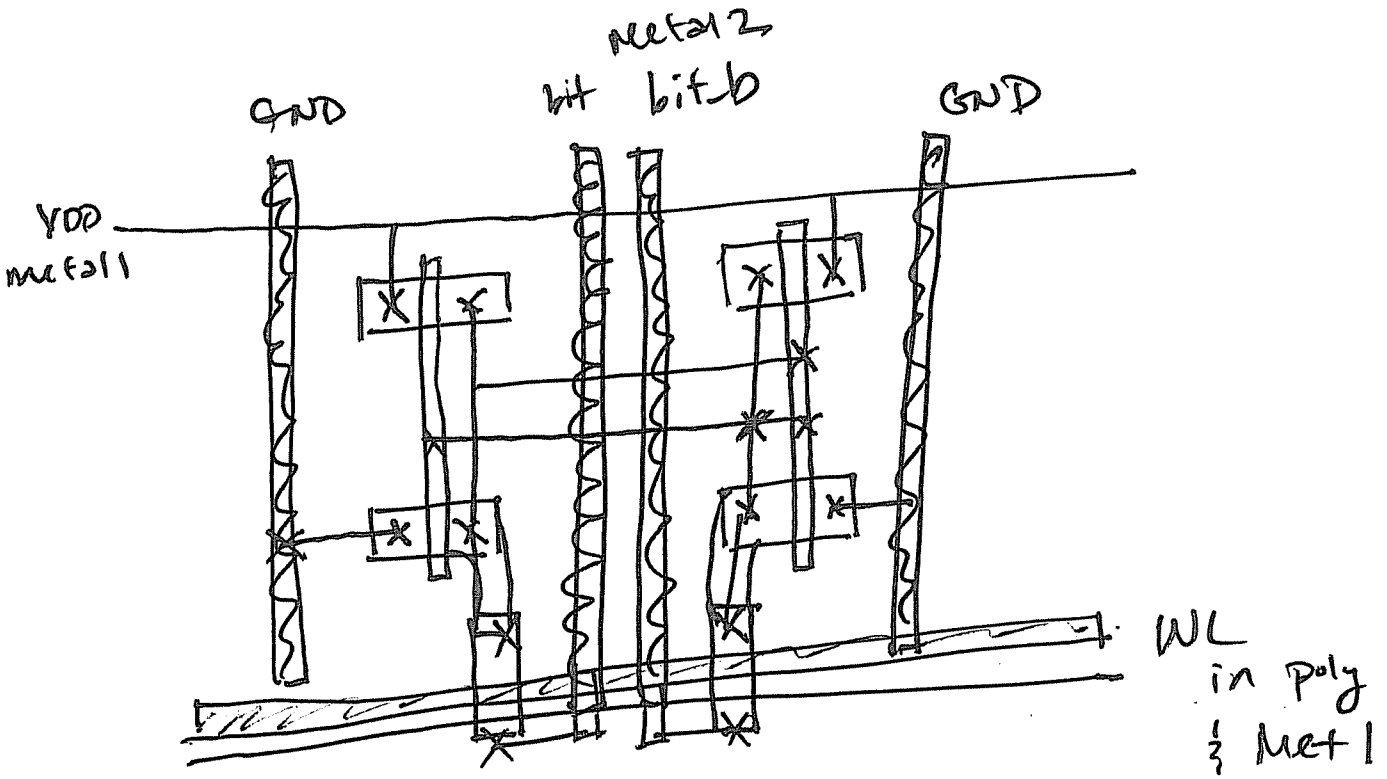
For read and write stability, the transistors must therefore be sized $D > A > P$. However, for good layout density all of the transistors must be kept relatively small.

Physical Layout



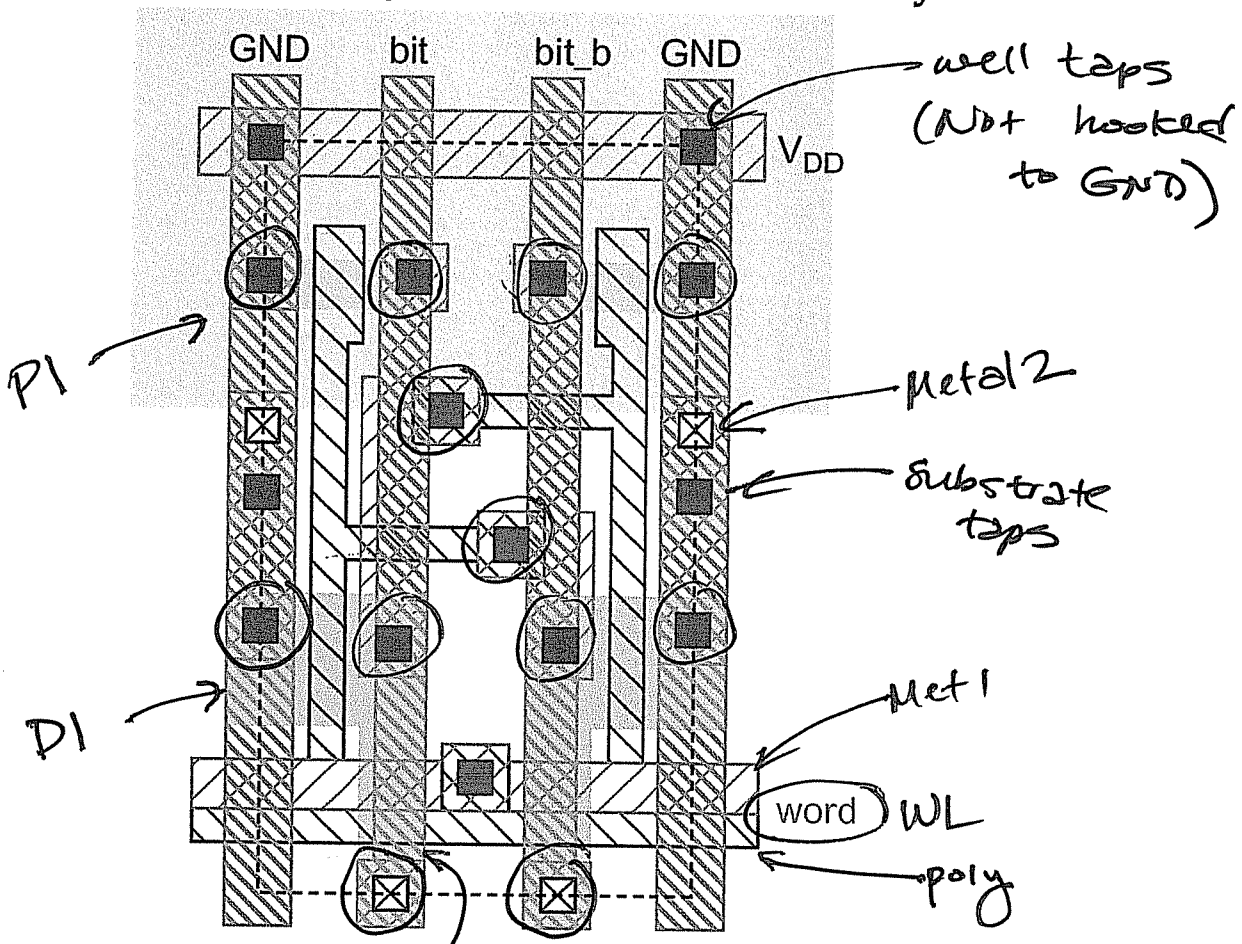
From your book:

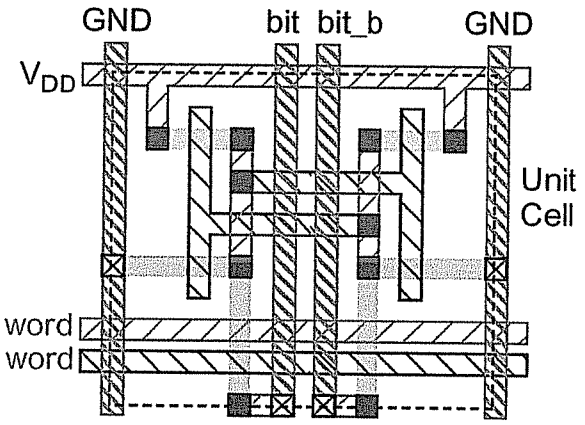


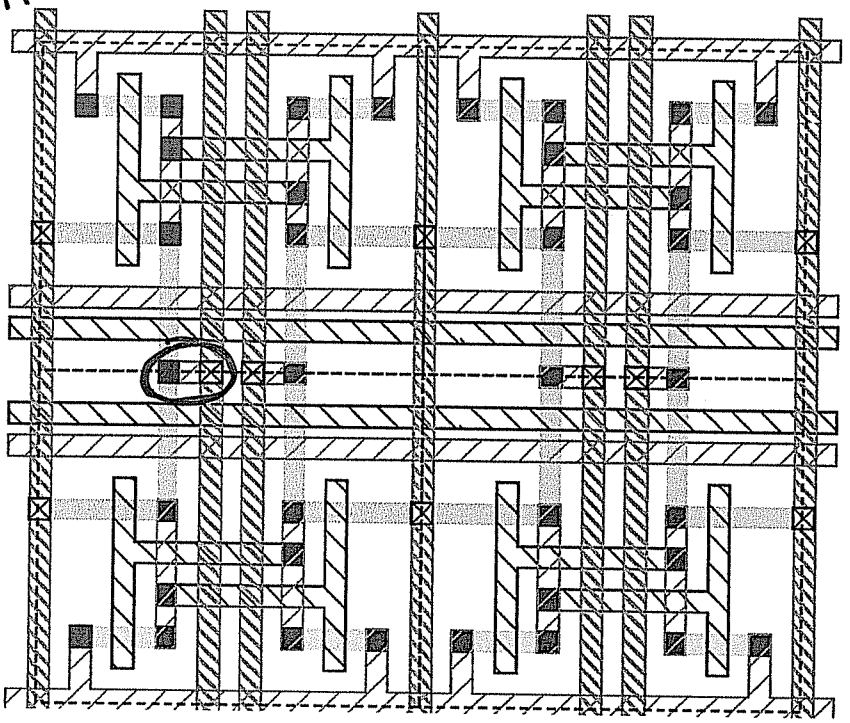

Metal2
GND
bit
bit_b
GND
VDD
Metal1
WL
in Poly
½ Met1

Consider an alternative where we run the bit lines up the middle:

The (more complicated) "traditional" 6T SRAM layout.





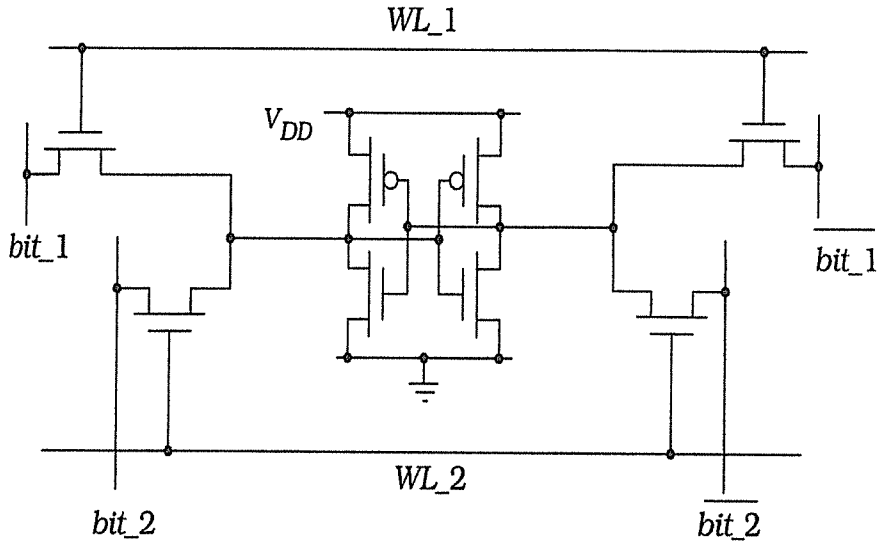


This layout has advantages over the layout in your text:

- The A and D transistors are different sizes, (for read stability)
- There is a shared diffusion contact to the bitlines between pairs of cells. This reduces C_{FET}, reducing the delay in discharging the bitline during read access
- Word is run in both poly and metal1. This allows word to propagate quickly through a large array, and still gate transistors in poly. The two lines need to be tied together at least every 4-8 cells. The layout above shows them contacted in each cell. The layout in the text routes Word only in poly, which will cause large RC delays for large arrays.
- Power and ground are shared between mirrored adjacent cells.

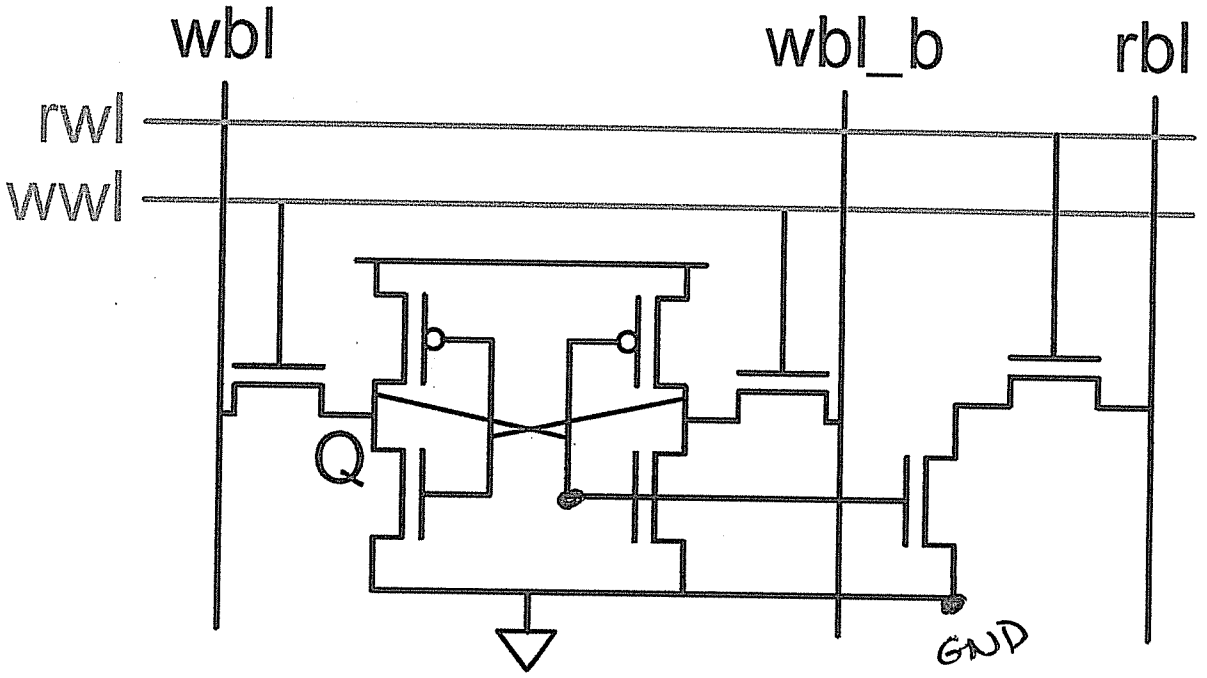
This traditional design was used until the 90 nm generation, and a more lithographically friendly version with fewer bends in the poly has been used ever since.

Multi-port SRAM



Provide access to more than one pair of *bit, bit_b* lines.

A notable example of a multiport cell is the 8T (8 transistor) dual-port SRAM cell.



The more compact 6T cell is limited by the tradeoff between read margin, write margin, transistor sizes and operating voltage.

The 8T cell circumvents some of these issues by avoiding backdriving during a read operation. Note that the read operation merely connects to ground if $\bar{Q}$ is also connected to GND, and therefore cannot backdrive the state node. By removing the read/write tradeoff, the 8T allows lower voltage operation, which is important for modern processes. Intel switched from 6T to 8T cells within the cores for its 45nm process Core processors.

Schedule for remaining lectures:

3/30: LAB DAY (no lecture)

4/2: 13.2, some remaining datapath topics

4/4: 13.3 – 13.5

4/6: LAB DAY (no lecture)

4/9: [As many of the remaining topics as possible]

4/11: Review for Exam 2

4/13: EXAM 2

Remaining topics:
- Signed Multiplication
- One/zero detectors
- Magnitude comparators
- equality comparators

} will try to get to these on 4/2

- Pseudo-nMOS
- Dynamic CMOS Logic Circuits
- Dual-Rail Logic Networks

Reading: Finish Ch. 13

Check-In: Describe the operation of a differential amplifier

Due Mon.