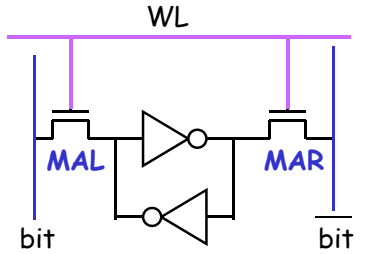
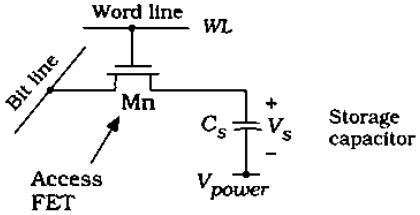
Memory Basics

- RAM: Random Access Memory
  - historically defined as memory array with individual bit access
  - refers to memory with both Read and Write capabilities
- ROM: Read Only Memory
  - no capabilities for "online" memory Write operations
  - Write typically requires high voltages or erasing by UV light
- Volatility of Memory
  - volatile memory loses data over time or when power is removed
    - RAM is volatile
  - non-volatile memory stores date even when power is removed
    - ROM is non-volatile
- Static vs. Dynamic Memory
  - Static: holds data as long as power is applied (SRAM)
  - Dynamic: will lose data unless refreshed periodically (DRAM)

SRAM/DRAM Basics

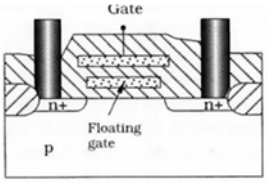
- SRAM: Static Random Access Memory
  - Static: holds data as long as power is applied
  - Volatile: can not hold data if power is removed
  - 3 Operation States: hold, write, read
  - Basic 6T (6 transistor) SRAM Cell
    - bistable (cross-coupled) INVs for storage
    - access transistors MAL & MAR
    - word line, WL, controls access
      - WL = 0 (hold) = 1 (read/write)
- DRAM: Dynamic Random Access Memory
  - Dynamic: must be refreshed periodically
  - Volatile: loses data when power is removed
  - 1T DRAM Cell
    - single access transistor; storage capacitor
    - control input: word line (WL); data I/O: bit line
- DRAM to SRAM Comparison
  - DRAM is smaller & less expensive per bit
  - SRAM is faster
  - DRAM requires more peripheral circuitry





ROM/PROM Basics

- ROM: Read Only Memory
  - no capabilities for "online" memory Write operations
  - data programmed
    - during fabrication: ROM
    - with high voltages: PROM
    - by control logic: PLA
  - Non-volatile: data stored even when power is removed
- PROM: Programmable Read Only Memory
    - programmable by user -using special program tools/modes
    - read only memory -during normal use
    - non-volatile
  - Read Operation
    - like any ROM: address bits select output bit combinations
  - Write Operation
    - typically requires high voltage (~15V) control inputs to set data
      - stores charge to floating gate (see figure) to set to Hi or Low
  - Erase Operation
    - to change data
    - EPROM: erasable PROM: uses UV light to reset all bits
    - EEPROM: electrically-erasable PROM, erase with control voltage



EPROM device structure

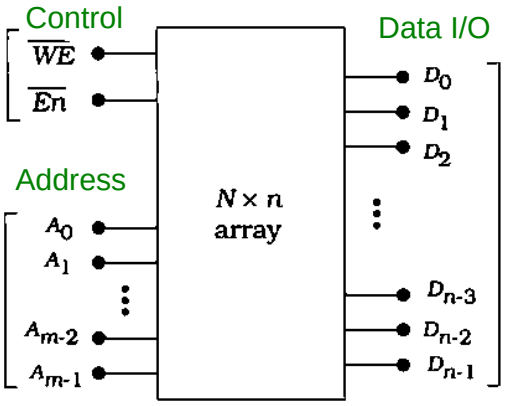
Comparison of Memory Types

- DRAM
  - very high density → cheap data cache in computers
  - must be periodically refreshed → slower than SRAM
  - volatile; no good for program (long term) storage
- SRAM (basically a Latch)
  - fastest type of memory
  - low density → more expensive
    - generally used in small amounts (L2 cache) or expensive servers
- EEPROM
  - slow/complex to write → not good for fast cache
  - non-volatile; best choice for program memory
- ROM
  - hardware coded data; rarely used except for bootup code
- Register (flip flop)
  - functionally similar to SRAM but less dense (and thus more expensive)
  - reserved for data manipulation applications

Memory Arrays

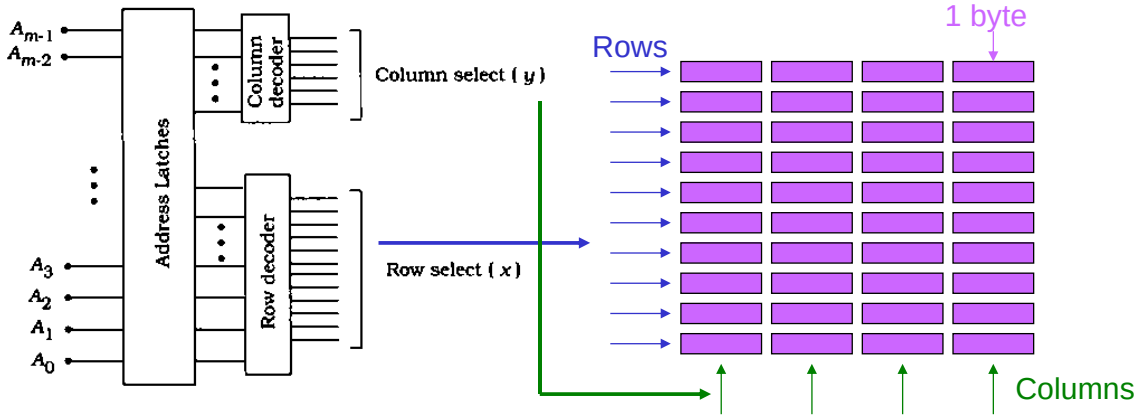
- N x n array of 1-bit cells
  - n = byte "width"; 8, 16, 32, etc.
  - N = number of bytes = "length"
  - m = number of address bits
    - max N = 2^m
- Array I/O
  - data (in and out)
    - D_{n-1} - D_0
  - address
    - A_{m-1} - A_0
  - control
    - varies with design
    - WE = write enable (assert low)
      - WE=1=read, WE=0=write
    - En = block enable (assert low)
      - used as chip enable (CE) for an SRAM chip

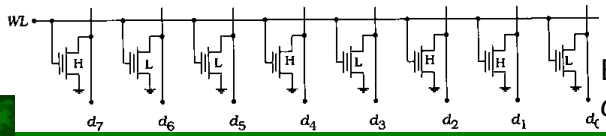
Memory "size":
bytes = N, # bits = N×n
Example:
1k x 8 RAM → 10 addr lines, 8-bit bytes
2^{10} = 1k (1024) mem locations = **length**
width = 8-bit, **size** = 1k-byte, 8k-bits



Memory Array Addressing

- Standard Memory Addressing Scheme
  - ***m*** address bits are divided into ***x*** row bits and ***y*** column bits (x+y=m)
    - address bits are encoded so that 2^m = N
    - array physically organized with both vertical and horizontal stacks of bytes

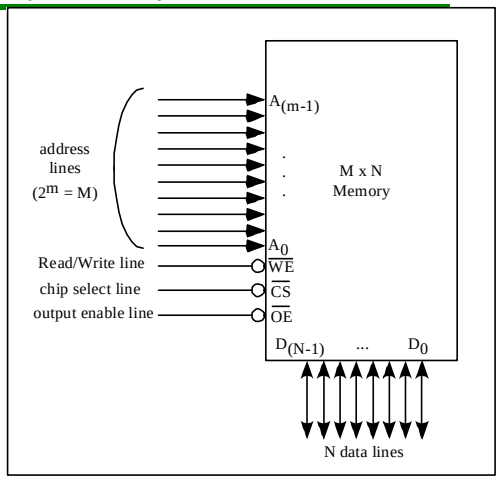


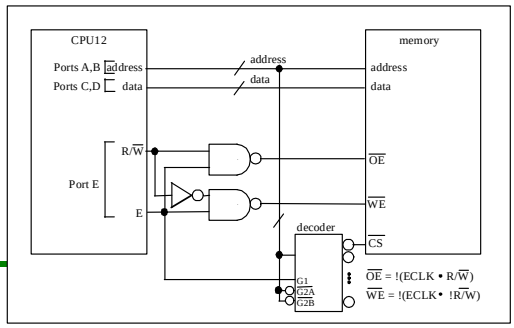


Example byte:
one word in an 8b-wide EPROM

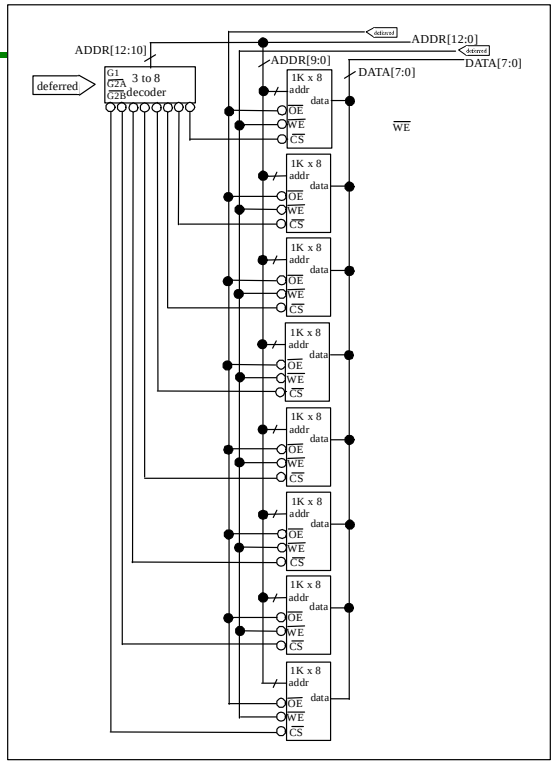
Typical Memory Chip

- Data
  - x-bits in parallel, typically x = 8, 16
- Address signals
  - m address signals → M=2^m addresses
- Control signals
  - **/WE: write enable** - when activated, values on data lines are written to specified address
  - **/OE: output enable** - data at specified location placed on data pins of memory chip, data lines connected to data bus using tristate outputs
  - **/CS: chip select** - selects a specific chip in an array of memory chips
- Connection to HC12 ----->

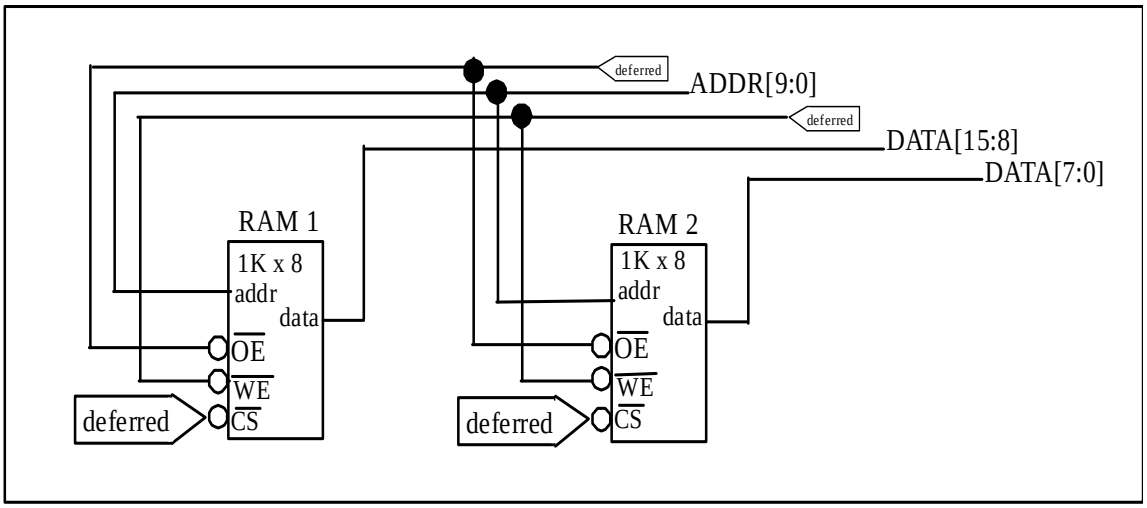




Memory Expansion
expanding memory length



Memory Expansion
expanding memory width



Memory Expansion
expanding memory length and width