Compact and Low Power Analog Front End with *in-situ* Data Decimator for High-Channel-Count ECoG Recording

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***Abstract*— High channel count neural implants that can record brain activities across diverse cortical regions represent the next step toward whole brain interfaces that will enable new understanding of brain operation and treatment of many neural disorders. To overcome the size and power constraints limiting the channel count of existing neural implants, this paper presents a new neural amplifier array design that utilizes hardware sharing to achieve low power and compact size. Moreover, to ease the burden of large volume data handling, *in-situ* data decimation is performed to enable off body evaluation of synchrony between signal pairs. A 32-channel analog front end array was designed and post-layout simulations show that the entire front end occupies only 0.031 mm^2 per channel while consuming only 3.34 µW per channel at 3.3 V in 0.5 µm CMOS. This front end decimates data by an order of magnitude while keeping the synchrony information with more than 89.1% accuracy.**

Keywords—high density neural recording; low power ECoG; resource sharing; phase synchrony; deta decimation

I. INTRODUCTION

Recent advances in the recording capabilities of neural implants have provided significant insight into the fundamental structure and networking schemes of the brain. Unveiling additional detailed information about the brain could yield new opportunities for treating many neural disorders as well as improving the quality of life for many disabled people. Improved understanding of neural function also opens new opportunities to develop bioinspired systems using e.g. neural network architectures. Key metrics for evaluating implantable neural recording options include scale, spatial and temporal resolution, and invasiveness. Recently, electrocorticography (ECoG) has emerged as an attractive approach for recording neural activity because it provides good spatiotemporal resolution while permitting greater scale and less invasiveness than penetrating microelectrodes.

Typically, millions of neurons generating microvolt signals are responsible for communication in a brain. Capturing these weak signals in a noisy environment is challenging, especially when recording systems need to meet implantation requirements for low power and small size. To address the simultaneous requirements for noise, power and size, researchers have been developing advanced neural recording implants [1], [2]. However, the strict requirements on size and power dissipation have historically limited the number of recording sites within an implant. Furthermore, for high-channel-count recording implants, excessive memory or data transfer rate is required which poses another limit on implementing these neural implants. On the other hand, implants with many recording channels are of great demand to improve spatial resolution and scale, permitting coverage of multiple brain regions. For instance, large-scale brain activity monitoring would enable researchers to both study neurophysiological principles and advanced brain-machine interfaces (BMIs) [3]. Therefore, new high-channel-count neural implants that perform *in-situ* data decimation while also meeting noise, size and power constraints are highly desired.

To enable future neural recording microsystems with thousands of channels, this paper introduces an ultra-compact and low power ECoG neural recording module that realizes efficient resource sharing between amplifier arrays and implements a newly developed algorithm [4] for *in-situ* data decimation. The reported system achieves exceptional area and power per channel metrics with the noise performance and frequency response necessary for ECoG while decimating data to enable an order of magnitude increase in number of recording channels which is a necessary step toward high-channel-count recording implants.

II. DATA DECIMATION USING PHASE PRESERVING QUANTIZATION

In ECoG recording, a common approach to analyze brain function and interpret neural events is to calculate the synchrony between recording channels. Among different methods for synchrony measurement, phase-locking value (PLV) is popular due to its insensitivity to variation in neural signal amplitude [5]. In BMI applications, PLVs would ideally be determined in real time to enable real-time feedback of informative features. However, the calculation of PLVs for thousands of channels is computationally intensive and would demand excessive power and circuit area to accomplish within an implant. For instance, the power and area budget for PLV calculation for 32 pairs of neural signals were reported as 400 µW and ~1.86 mm^2, respectively using custom computational hardware in 0.13 um CMOS [6]. For an *n*-channel system, synchrony should be examined for *k* 2-channel signal combinations or pairs, where $k = C(n,2) = n!/(2(n-2)!)$. *k* rapidly increases with *n* and at high channel count demands a power and area budget

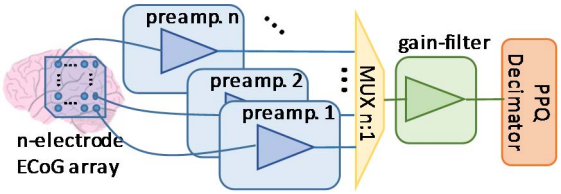

Fig. 1. Illustration of an n-channel neural recording system.

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that is not affordable in an implant regime. An alternative approach adopted in our work is to send ECoG data off body where more power is available for external processing.

For chronic experiments in freely moving subjects, recorded data needs to be transferred off body wirelessly. Consider a neural signal that is sampled at 160 Hz (to support gamma band ECoG signals with 80 Hz bandwidth) and 10-bit resolution, where 1,000 channels would require at least 1.6 Mbps wireless transfer rate. This transfer rate would increase linearly with the number of channels or sampling frequency. Thus, because wireless links consume significant power that increases with data transfer rate, the wireless transfer rate becomes a limiting factor. Therefore, as we seek to achieve high channel counts, data decimation before transmission is necessary to overcome wireless link limitations.

We have recently developed a method called phase-preserving quantization (PPQ) that retains the synchrony information between ECoG signals while decimating data by an order of magnitude [4]. PPQ has been demonstrated to calculate inter-channel PLV with at least 90% accuracy with only 1-bit quantization of raw neural data. PPQ decimation was implemented in the neural recording analog front end reported here.

III. Architectural Design

As shown in Fig. 1, the structure of our neural recording system consists of an *n*-electrode (*n*-channel) ECoG array with *n* preamplifiers and a common gain stage that also provides frequency band filtering. The amplifier block is followed by a signal processing block that implements 1-bit quantization for digitization and PPQ data decimation. Because neural signals are weak and susceptible to noise, each channel is assigned to an individual preamplifier stage; this design choice also eases the noise performance requirement of subsequent stages. Hence, our approach for enabling high channel counts centers around reducing the area and power of the preamplifiers, decimating signals to enable high-volume data, and scaling the architecture to support as many channels as possible.

A. Shared Preamplifiers

In prior work [7], [8], it has been shown that the area and power of a biosensor amplifier array can be significantly reduced using an operational transconductance amplifier (OTA) sharing technique. The symmetric structure of an OTA allows it to be viewed as positive and negative halves, and when the positive inputs of independent OTAs use a common reference voltage, their positive halves can be shared, as shown in Fig. 2. Thus, an *N*-channel neural preamplifer array could be implemented with *N* negative-half "pixel" segments and a single "shared segment", significantly reducing area and power of each channel and permitting more channels within the same budget.

B. Gain Stage and Filter

To provide sufficient gain, neural recording systems typically include a common gain stage that is shared by multiple preamps, as shown in Fig. 1. With proper design of the amplifier feedback network, the gain stage can also double as a filter to reject noise and extract the signal band of interest. ECoG signals contain information in several sub-bands such as delta (1–3 Hz), theta (4–7 Hz), alpha (8–13 Hz), beta (14–30 Hz), and gamma (30–80 Hz) [9]. To permit application flexibility, a tunable filter was chosen to pass different frequency bands based on user input.

A common gain-filter stage helps to reduce power and area, and its resources can be time-division multiplexed between a number of channels, where the maximum number of multiplexed channels is limited by channel sampling rate and mismatch in preamp OTA sharing. A detailed small signal model for mismatch induced effects has been presented in [10]. To service high channel counts, we utilized the architecture shown in Fig. 3, where *N* recording channels share a common gain-filter stage forming a cluster, and the outputs from *M* clusters are multiplexed to permit $n = N \times M$ total channels.

As discussed in the next section, the preamp and gain-filter stages can utilize the same core OTA structure. Thus, the gain-filter stage was segmented and shared the same way the preamps were to save power and area.

C. PPQ Decimator

This block contains a comparator referenced to the DC value of gain-filter stage. Each cluster includes one decimator to handle 8 amplified and filtered signals. Data decimation is occurred in this stage where each signal quantized with 1-bit resolution. The schematic of this comparator is shown in the inset of Fig. 3.

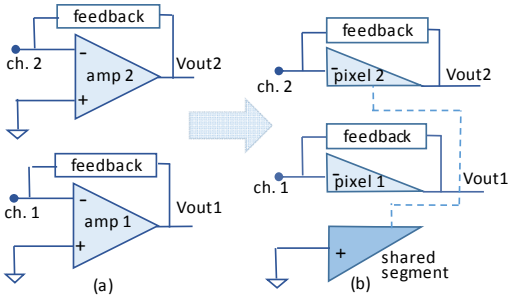

Fig. 2. (a) A traditional 2-channel amplifier and (b) a 2-channel amplifier using a shared-segment configuration.

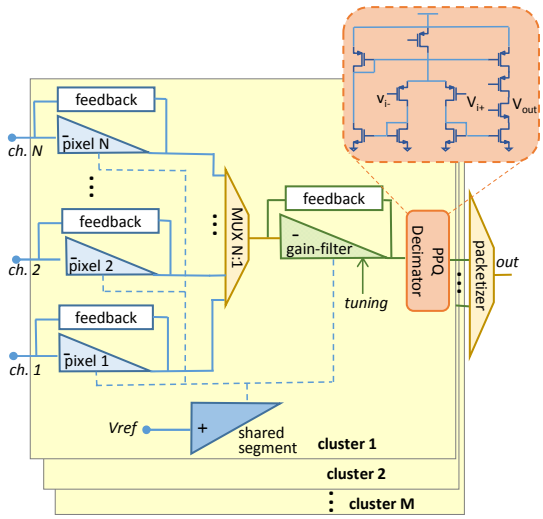

Fig. 3. Neural recording system for $n = N \times M$ channels with hardware resource sharing. The inset shows the schematic of the 1-bit PPQ quantizing comparator.

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IV. Circuit Design and Implementation

A. Preamplifier and Gain-Filter Stages

The first stage of the analog front end is the neural preamplifier that is directly connected to the electrode to capture the neural signal. To isolate the neural signal DC level from the preamplifier DC level and set an accurate gain, the capacitive input and feedback structure shown in Fig. 4a was selected, where the preamp gain is $A_v = C_1/C_2$. To generate a DC path for the OTA inverting input, a resistive feedback path was created using transistor M_R. The parallel combination of resistively-connected M_R and feedback capacitor C_2 forms an inherent high-pass filter (HPF). Because neural amplifiers need to see very low frequency signals, the pole of this filter needs to be located close to the origin, which requires a large resistor or capacitor. A large C_2 is not preferred because CMOS capacitors occupy excessive chip area, and C_2 is inversely proportional to preamp gain. Therefore, we chose to implement a large on-chip resistance using a MOS-Bipolar pseudoresistor (M_R) that has been shown to provide very high resistance with small area [1]. By setting C_2 to 100 fF and the W/L of M_R to 1.5µm/1.5µm, the preamplifier was designed to have a HPF low frequency cutoff at around 1 Hz. The preamp also has an inherent low-pass filter at the OTA output due to the load capacitance of the next stage, which produces a high frequency rolloff around a few kHz. ECoG signal sub-bands of interest can be selected using the tunable bandpass filter stage that follows the preamplifier. With C_2 set to 100 fF, the preamplifier gain is defined by C_1; however, C_1 also plays an important role in noise performance, and optimization of its value is presented later in this section, after noise analysis.

Fig. 4b, defines the structure chosen for the gain-filter stage. Like the preamp, this stage provides capacitive gain defined by $A'_v = C'_1/C'_2$. It also provides tunable bandpass filtering with the low cutoff determined by C'_2 and M_2 in the OTA feedback path and the high cutoff determined by C_L and M_3 at the OTA output. The high and low pass cutoff frequencies can be tuned by the user through the gate voltages of M_2 and M_3, respectively, where the tuning of M3 can accommodate a range of C_L load capacitances in the tens of fFs. To set the proper frequency response and filtering range of this stage, C'_2 was designed to be 100 fF and the W/L for both M_2 and M_3 was set to 1.5µm/1.5µm. Next, we note that an overall gain, A_{amp}, of 500 (54dB) is desirable for each neural input channel and is defined by

$$A_{amp} = A_{v(preamp)} \cdot A'_{v(gain-filter)} = \frac{C_1}{C_2} \times \frac{C'_1}{C'_2} \quad (1)$$

Since C_2 and C'_2 were set to 100 fF for proper filter response, (1) shows that $C_1 x C'_1 = 5$ pF^2 is necessary to achieve A_{amp}=500. Optimization of these values is presented below after defining their noise performance roles.

B. Shared OTA Design

The preamplifier and gain-filter were designed to use identical OTAs to realize the OTA sharing technique discussed in section II. Although prior work with OTA sharing [8] used a different OTA structure, we chose the telescopic OTA because it provides exceptional size, power and noise performance as well as an elegant implementation

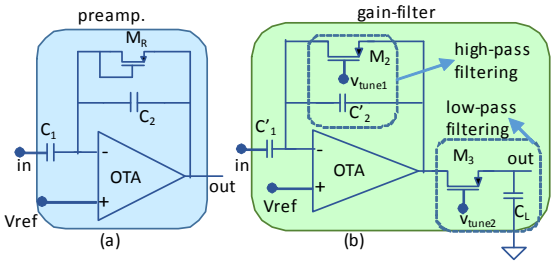

Fig. 4. (a) Preamplifier with capacitive feedback, and (b) tunable filter and gain stage.

of OTA sharing, as shown in Fig. 5. Our OTA contains a shared segment that provides the biasing for multiple independent signal amplification segments. It also supports eight preamps "pixel" segments and a segment for the common gain-filter stage. PMOS transistors were chosen as input transistors (i.e. $M_{p1,x}$) because of their lower 1/f noise compared to their NMOS counterparts. The size of the input PMOS transistors is critical to the noise performance of the entire amplifier as discussed below.

Notice in Fig. 5 that many channels are connected to node VT, which could cause the potential at this node to fluctuate as input signals change in different channels. This would result in undesirable crosstalk between channels. To resolve this, an inverting feedback was applied at node VF, which decreases the resistance seen at VT, r_{VT}, by:

$$r_{VT} = \frac{r_{s\_p1,sh}}{1+g_{m\_tail}R_{VF}} \quad (2)$$

where $r_{s\_p1,sh}$ is source resistance of $M_{p1,sh}$, g_{m_tail} is the transconductance of M_{tail} and R_{VF} is the equivalent resistance at node VF. As a result, the source resistance of $M_{p1,sh}$ in shared segment is considerably lower than any of the input (pixel and gain-filter) segments. Consequently, the voltage at node VT is defined mainly by the shared segment, and thus the input segments are well isolated from each other.

C. Noise Analysis

The main contributor to noise in the overall neural amplifier is the preamplifier stage, whose input-referred noise power is given by [1]

$$\overline{v_{ni,amp}^2} = \left(\frac{C_1+C_2+C_{in}}{C_1}\right)^2 . \overline{v_{ni}^2} \quad (3)$$

where $\overline{v_{ni}^2}$ is the input referred noise power of the OTA, C_1 and C_2 are the same as in Fig. 4 and C_{in} is the parasitic input

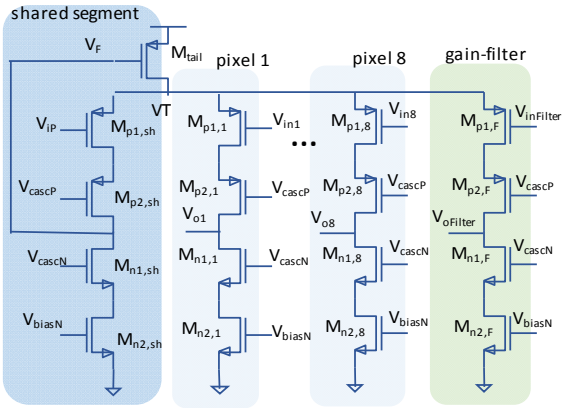

Fig. 5. Schematic of a shared telescopic OTA.

capacitance of the OTA. C_{in} acts to attenuate the input signal and hence increases the input referred noise. Therefore, a smaller C_{in} improves the overall noise performance, which can be achieved using small input PMOS transistors in the OTA (i.e. $M_{p1,x}$). However, small input transistors generate higher 1/f noise which is important for low frequency neural signals and could increase input referred noise of both the OTA ($\overline{v_{ni}^2}$) and the whole amplifier ($\overline{v_{ni,amp}^2}$). To balance this tradeoff, the input PMOS transistor sizes were set to (W/L) = 5×(10.5µm/6 µm), which results in a gate capacitance of 283 fF for input PMOS transistors and thus a small C_{in}.

Another important factor in noise performance is the value of C_1. As (3) suggests, larger C_1 reduces the input referred noise of the amplifier. On the other hand, since each channel requires an individual C_1, a smaller C_1 is more area efficient. In this work, a value of C_1 = 5 pF was chosen to address the tradeoff between area and noise. This sets the preamplifier gain to $A_{v(preamp)}$ = 50 (34 dB), which in turn allows us to set C'_1 = 1 pF (since C'_1=5/C_1) to achieve a gain-filter stage gain of $A'_{v(gain\text{-}filter)}$ = 10 = 20 dB.

V. Results and Discussion

To validate this design concept, an 8-channel neural amplifier array with a tunable filter was designed in 0.5 µm CMOS technology with a 3.3 V supply. Fig. 6 shows the layout of the neural amplifier array with an 8-channel preamplifier, an 8:1 multiplexer, a gain-filter stage and a PPQ data decimation stage. The 8-channel array occupies an area of 0.251 mm^2, or 0.031 mm^2 per channel. Post-layout simulation shows 3.34 µW power dissipation per channel from which amplifiers consume only 0.646 µW per channel.

To measure noise performance, the neural amplifier was tuned for ECoG recording in the range of 1 Hz – 80 Hz. An input referred noise of 1.93 μV_{rms} was measured for each channel, which meets application requirements. Because amplifiers exhibit a well-known tradeoff between noise and power, a useful metric for comparing performance is the noise efficiency factor (NEF) defined as [1]

$$NEF = v_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi.U_T.4kT.BW}} \qquad (4)$$

where $v_{ni,rms}$ is the input referred noise, I_{tot} is the total bias current and BW is bandwidth of the amplifier. For ECoG bandwidths, our amplifier achieves NEF=3.71. Table I summarizes the simulated characteristics of the ECoG amplifier. These results show similar or better area, power, and NEF compared to state of the art neural amplifiers [11], [12].

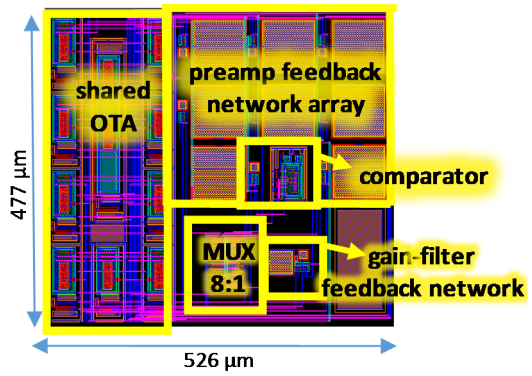

Fig. 6. Layout of 8-channel neural amplifier with tunable filter and data decimator (comparator).

To evaluate PLV performance following PPQ decimation within our neural recording chip, 4 clusters of the 8-channel module in Fig. 6 were used in parallel to process 32 channels of ECoG data recorded from a rat. The gain-filter stage was tuned to capture signals in the alpha band, and the filtered signal then passed through the PPQ decimator and quantized to 1 bit. This decimated data was then used to calculate PLVs. The connectivity matrix (CM) in Fig. 7 shows PLVs as the indicator of synchrony between every two-channel pair for all 32 channels. To compare the accuracy of our results, root mean square of each element of the connectivity matrix in Fig. 7 (CM_{PPQ}) was calculated relative to the correspondent element in the reference CM without any data decimation ($CM_{orig.}$), using

$$RMS_{error} = \sqrt{\frac{1}{k}\sum\left(CM_{PPQ} - CM_{orig.}\right)^2} \qquad (5)$$

where k is the number of pairs. Then,

$$Accuracy = (1 - RMS_{error}) * 100 \qquad (6)$$

In our design, while the data was decimated by an order of magnitude, an accuracy of 89.1% was achieved.

VI. Conclusion

To facilitate high channel count neural recording, a low-power, ultra-compact neural amplifier array with tunable frequency filter has been presented. The analog front end also decimates recorded data by an order of magnitude while maintaining phase synchrony information with 89.1% accuracy. Post-layout simulation results show that this analog module consumes only 0.031 mm^2 of area and 3.34 µW of power per channel while providing adequate noise performance and the ability to tune response across the range of ECoG frequencies from delta to gamma bands (1 Hz to 80 Hz). These results demonstrate a means for achieving future high channel count recording implants.

TABLE I. Simulated Characteristics of the ECoG Amplifier

Parameter	value	Parameter	value
Supply	3.3 V	Bandwidth	80 Hz
Power/channel	0.646 µW	In. ref. noise	1.93 µVrms
Area/channel	0.031 mm^2	NEF	3.71

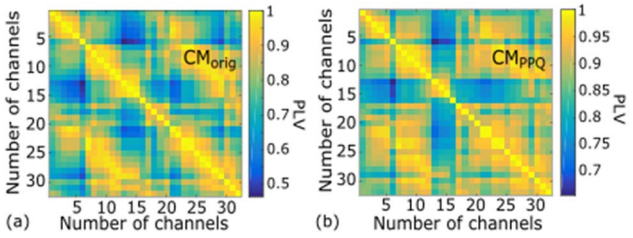

Fig. 7. CMs of 32-channel ECoG data in alpha band (a) unquantized original data and (b) PPQ decimated data which achieves 89.1% accuracy compared to CM_{orig}.

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