

A Method for Reliability Evaluation of Multi-Level Converters

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Abstract—In recent years, several multilevel converters have been developed. The best-known multilevel converter types are: diode clamped, capacitor clamped and cascade. From these basic configurations a variety of multilevel converters have been produced in order to increase efficiency, reduce number of diodes or switches and increase reliability. The increasing proliferation of these converters in motor drives, flexible ac transmission systems (FACTS), and renewable resource integration motivates the development of reliability methods to evaluate these devices and reliability issues therein. This paper proposes a method based on minimal path set to evaluate the reliability of multilevel converters. The method is demonstrated on a five-level converter.

Index Terms—reliability, path set analysis, power electronic converter reliability, multilevel converters.

I. INTRODUCTION

In recent years, the development and use of multilevel converters in power systems has grown significantly. Application of these converters range from motor drives to flexible ac transmission systems (FACTS) to renewable resource interfaces. Multilevel converters overcome many technical problems associated with conventional converters, such as the mitigation of voltage stress limitations of insulated gate bipolar transistors (IGBT) [1]. The increasing proliferation of these converters motivates the development of reliability methods to evaluate these devices and reliability issues therein. Yang et al. [2] reports that “power electronic devices are the most fragile components across all industry sectors,” and provides a survey of the various reliability issues encountered in such devices. Much research [3] has been devoted to improving the fault tolerance of multi-level converters. However, the reliability evaluation of such converters has still not been well addressed. Some researchers [4], [5] have considered the reliability in the topological design of converters. Further, techniques that rely on the use of two-state or derated state models are not suitable for power electronic converters. For instance, a power generator can produce rated power, zero power and any value in between. In power electronic converters and switches the situation is different. Power converters, especially multilevel converters, can produce many voltage levels that can be considered successful states. However, power electronic

switches can fail open or fail short and these states are discrete states.

In the literature there are many techniques to evaluate system reliability. Some of these techniques are analytical, such as reliability network analysis, minimal cut set, minimal path set, and state enumeration. There are also methods based on Monte Carlo simulation. However, system states need to be determined first in order to apply these techniques. In power electronic systems, it is not always necessary to build the reliability block diagram or state transition in order to evaluate system reliability. An examination of the configurations of converters reveals that in most cases their topology is amenable to the application of direct methods of analysis. In section III, we show that minimal path sets can be directly created from the configuration of a converter.

Reliability considerations of power electronic converters in the literature can be categorized into qualitative and quantitative evaluations. Most work on qualitative comparison between converters, such as [3], [6], [7], the reliability of converters is evaluated and compared based on fault tolerant ability which can be achieved by modifying the control scheme or converter configuration. Quantitative evaluation, on the other hand, is based on assessing the reliability of the converters based on failure and repair rates such as in [1], [8]–[11]. The common practice of quantitative evaluation assumes that all components are required for the system to success and therefore the components are assumed to be connected in series from reliability of view. In such work, the failure rate of the system is the sum of the failure rates of the components. In [1], [8], [9], the authors assumed that the Mean Time To Repair (MTTR) is very small with comparison to Mean Time To Failure (MTTF) and considered the Mean Time Between Failures (MTBF) as the reciprocal of the failure rate of the system and have focused on system MTBF as the index of interest. In [10] a flat MTTR of 6 hours was assumed, while in [11] the authors estimated MTTR values from Weibull distributions and experimental data. In [12], the authors utilized the cut set technique to derive equations to evaluate HVDC converter reliability, but did not report results.

In this paper, the minimal path-set technique is utilized to evaluate availability and frequency of failures of multi-

level converters. We applied this technique due to redundancy property of the multi-level converters and multi-state property of power electronic components.

This paper is organized as follows: section II provides a brief description of the modeling and method used in this work, section III described the proposed approach, section IV illustrates the method on five-level inverter and section V provides some concluding remarks.

II. RELIABILITY MODELING OF MULTILEVEL CONVERTERS

A. Reliability of Power Electronic Components

In power electronic systems, the components that contribute predominantly to system failure are IGBTs, diodes and capacitors. The reliability performance of these components are affected by environmental and stress factors. According to the MILHDBK-217F military standard [13], the failure rates of these components are described as shown below. IGBT failure rate is described by

$$\lambda_{IGBT} = \lambda_{IGBT_b} \pi_T \pi_Q \pi_E \quad \text{Failures}/10^6 \text{ hours} \quad (1)$$

where λ_{IGBT_b} is base failure rate of the IGBT, π_T temperature factor, π_Q quality factor and π_E environmental factor.

Similarly, diode failure rate is given by

$$\lambda_{diode} = \lambda_{diode_b} \pi_T \pi_S \pi_C \pi_Q \pi_E \quad \text{Failures}/10^6 \text{ hours} \quad (2)$$

where λ_{diode_b} is base failure rate of the diode, π_S voltage stress factor, π_C contact construction factor and π_T , π_Q and π_E as for IGBT.

Capacitor failure rate is given by

$$\lambda_{cp} = \lambda_{cp_b} \pi_T \pi_C \pi_V \pi_{SR} \pi_Q \pi_E \quad \text{Failures}/10^6 \text{ hours} \quad (3)$$

where λ_{cp_b} is base failure rate of the capacitor, π_V voltage stress factor, π_{SR} series resistance factor and π_T , π_C , π_Q and π_E as for IGBT.

B. Configuration and Modeling

The configuration of systems comprising switching devices is particularly amenable to network-based analytical methods such as those using minimal cut and minimal tie sets. In these methods, a reliability block diagram of the system is constructed based on the relationships between the functional blocks of the systems and graph theoretic or network analysis methods are used to analyze the block diagrams and determine system reliability. These methods are amply described in [14] and [15], but we provide a brief description of the path-set method below.

In most power electronic systems, the components are connected in a way such that their block diagrams can be derived easily by inspection of their configurations. However, the models for these particular components must recognize the fact that power electronic switches are characterized by having three states devices (normal, fail open or fail short). The problem is how to analyze and deal with such systems. In this research a method is proposed to derive minimal path sets directly from the configuration of a converter, thereby obviating the construction of a reliability block diagram.

C. Path-Set Method

Simple systems can be analyzed using series/parallel reduction technique. However, decomposition of complex systems into series/parallel paths may not be practical and time consuming. Also, it is quite difficult to make such decomposition process programmable. Path-Sets approach is more useful and easier for computer application.

Suppose a system described by a network consists of nodes and arcs as shown in Fig. 1. The source node is denoted by s and the sink node by t . Each component of the system is represented by an arc passing from one node to another. If a component fails, its corresponding arc is removed. The system succeeds if at least one path exists between s and t .

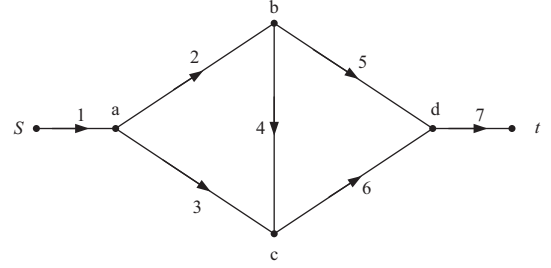


Fig. 1. Network describing a system of seven components.

The path-set and minimal path-set can be defined as follows:

- A *path-set* is a set of components such that their success will make the system successful for the specified operating conditions.
- A *minimal path-set* is a path set that does not contain any other path set as a proper subset; it can be viewed as a path in which all components included in the path are required to be working in order for the system to function. In other words, if any component fails, the system will fail.

Having determined the minimal path-sets, the system reliability can be determined as follows [14] and [15].

Components of a minimal path are connected in series. However, the minimal path-sets themselves are connected in parallel. Therefore, the availability of the system can be expressed as,

$$P_s = P(T_1 \cup T_2 \dots T_m) \quad (4)$$

Where, T_i is the availability of the minimal path-set i and m is the number of the minimal path-sets.

The frequency of failures of the system, f_f and frequency of successes of the system, f_s are disjoint subsets and there exists frequency balance between them. Having said that, the frequency of failure and frequency of success are equal,

$$f_s = f_f \quad (5)$$

The frequency of failures/successes between the minimal i^{th} path-set and the minimal k^{th} path-set can be calculated as follows:

$$f(T_i \cup T_k) = f(S_i \cup S_k)$$

Where, S_i and S_k are the state space subsets equivalent to minimal path-sets T_i and T_k respectively

Therefore, the frequency of failures between the minimal i^{th} path-set and the minimal k^{th} path-set can be expressed as follows

$$f(T_i \cup T_k) = (S_i \cup S_k) = P(T_i) \lambda_i + P(T_k) \lambda_k - P(T_i \cap T_k) (\lambda_i \cup \lambda_k) \quad (6)$$

Where, $(\lambda_i \cup \lambda_k)$ is the summation of the failure rates of components common to T_i and T_k and $P(T_i)$ and $P(T_k)$ are the probability of success of the minimal path-sets i and k .

The frequency of failures of the system, f_f is expressed as:

$$f_f = f(T_1 \cup T_2 \dots T_m) \quad (7)$$

As an example, for the system in Fig. 1, the minimal path-sets are:

$$\{1, 2, 5, 7\}, \{1, 3, 6, 7\}, \{1, 2, 4, 6, 7\}, \{1, 3, 4, 5, 7\}$$

The probability and frequency of failure are given by:

$$P_s = P(T_1 \cup T_2 \cup T_3 \cup T_4)$$

$$f_f = f(T_1 \cup T_2 \cup T_3 \cup T_4)$$

D. Multilevel Converter Configuration

Multilevel converters have been utilized in many high power applications such as power system load flow control and compensation and motor drives. The best-known multilevel converters are cascade, diode clamped and capacitor clamped (known as flying capacitor). The multilevel inverters are characterized by multi voltage levels with less distortion. Also, they are known by having high efficiency, low switching frequency and low voltage devices [16]. Fig. 2 shows the three basic configurations of the multilevel inverters.

From these three basic multilevel converters, many new combinations are produced and several multilevel inverters have been developed from the basic structures. For instance, in order to reduce the number of dc sources in the cascaded inverters, a diode clamped or capacitor clamped is adopted to replace a full bridge cell and recognized as Mixed-Level Hybrid Multilevel Cells and Asymmetric Hybrid Multilevel Cells in which $C_2 > C_1$ as shown in Fig. 3 [16].

III. RELIABILITY EVALUATION OF MULTILEVEL CONVERTERS

A. Proposed Approach

When components of a converter are working normally, there is no need to build a reliability block diagram. However, for the other states, i.e. fail open or fail short, it is necessary to create a minimal path for each case. Also, for multilevel inverters, some voltage levels are acceptable for system to operate. Therefore, reliability minimal paths for each level are to be determined. In addition, from the enumeration of

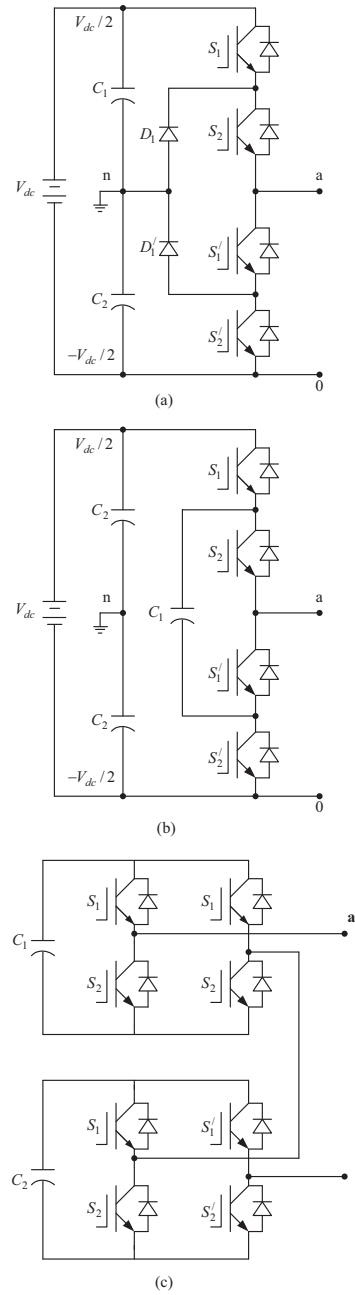


Fig. 2. Basic configurations of multilevel converters .

operating states of a converter, the minimal number of paths for unavailability is less than the minimal number of paths for availability.

We provide below an algorithm for directly determining the minimal path sets from the topology of a converter and calculating the reliability. Fig. 4 shows the flowchart of the method.

Algorithm description:

- Determine the voltage level for which the unavailability is to be calculated.
- For each switch and diode enumerate fail open and fail short states. For capacitors consider open state only.

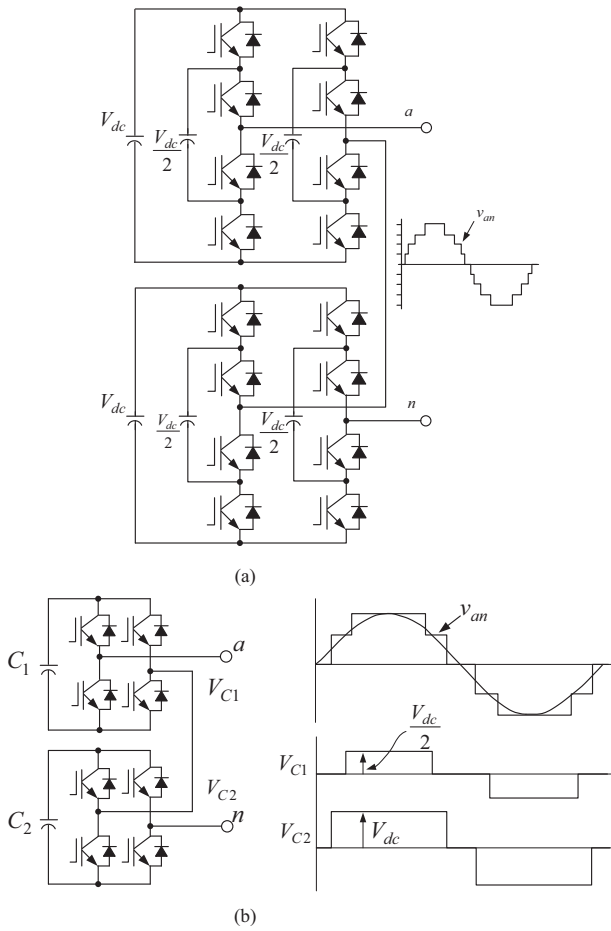


Fig. 3. (a) Mixed-Level Hybrid Multilevel Cells and (b) Asymmetric Hybrid Multilevel.

- Starting from the left to the right, sweep the converter components for failures.
- If this path connects the sending and receiving ends of the specified voltage level, save this path and continue searching for another path.
- From the minimal unavailability paths, determine the overall unavailability by series and parallel reduction.
- The unavailability of each path can be calculated by series combination and all paths are combined by parallel combination.

B. Reliability Calculation

Due to the large number of switching devices in multilevel converters, the overall reliability of the converter is mainly affected by its configuration [10]. Also, failures of power electronic switches can be fail open or fail short. Therefore, these switches are considered as three state devices: normal, fail open or fail short. The proposed method is explained on one leg of the three basic configurations.

Cascade and capacitor clamped converters have only capacitors and IGBTs and the diode clamped in addition to the capacitors and IGBTs contains diodes. Even though diode clamped converters have components more than the capacitor

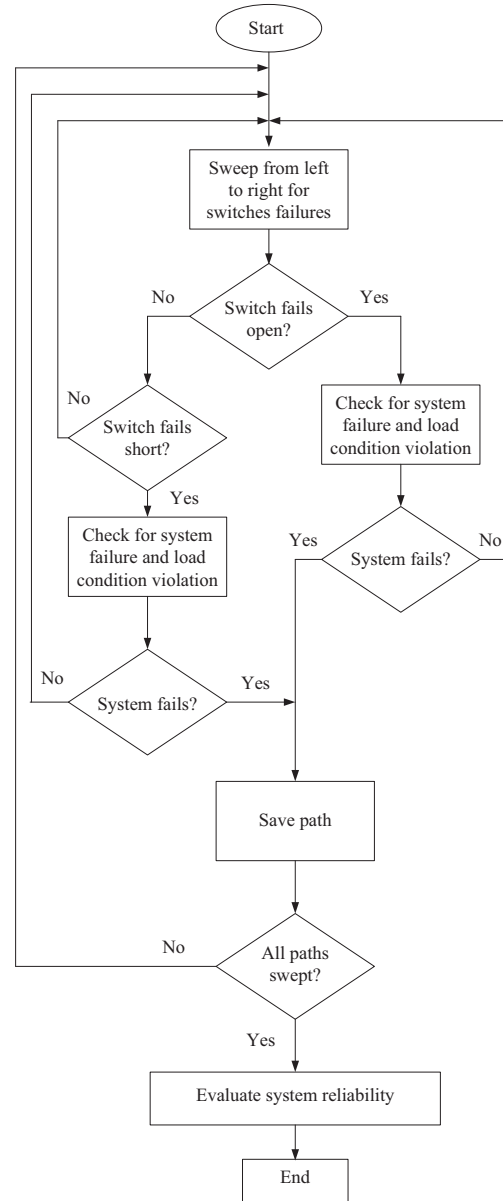


Fig. 4. Flowchart for Converter Reliability Evaluation.

clamped, capacitors are the most vulnerable components in the converters.

Since there are several possibilities to voltage levels, and many electronic components, the proposed method is applied on the switches only. The proposed method is applied on the five-level converter presented in [3] as shown in Fig. 5.

To produce $1 V_{dc}$ output voltage, the following switches have to be working:

$$S_{P1}, S_{P2}, S_{P3} \text{ or } S_{P4}$$

Therefore any combination other than this will cause the system to fail. If S_{P1} fails open, the paths will be reduced to three paths S_{P2}, S_{P3} or S_{P4} . If S_{P1} fails short, the paths will be reduced to no paths and so on.

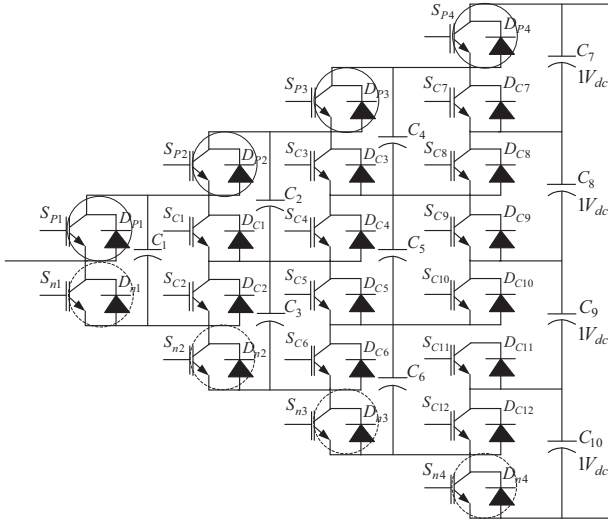


Fig. 5. Generalized Five-Level Converter.

To produce $2 V_{dc}$ output voltage, the following switches have to be working:

$$(S_{P1} \text{ and } S_{P2}), (S_{P1} \text{ and } S_{P3}), (S_{P1} \text{ and } S_{P4}), \\ (S_{P2} \text{ and } S_{P3}), (S_{P2} \text{ and } S_{P4}) \text{ or } (S_{P3} \text{ and } S_{P4})$$

Therefore, any combination other than that will cause the system to fail. For instance, if S_{P1} fails open, the path will be reduced to three paths (S_{P2} and S_{P3}), (S_{P2} and S_{P4}) or (S_{P3} and S_{P4}). If S_{P1} fails short, the paths will be reduced to three paths (S_{P1} and S_{P2}), (S_{P1} and S_{P3}) or (S_{P1} and S_{P4}) and so on.

To produce $3 V_{dc}$ output voltage, the following switches have to be working:

$$(S_{P1}, S_{P2} \text{ and } S_{P3}), (S_{P1}, S_{P2} \text{ and } S_{P4}), \\ (S_{P1}, S_{P3} \text{ and } S_{P4}) \text{ or } (S_{P2}, S_{P3} \text{ and } S_{P4})$$

Therefore any combination other than this will cause the system to fail. For example, if S_{P1} fails open, the path will be reduced to one path (S_{P2}, S_{P3} and S_{P4}). If S_{P1} fails short, the path will be reduced to three paths (S_{P1}, S_{P2} and S_{P3}), (S_{P1}, S_{P2} and S_{P4}), (S_{P1}, S_{P3} and S_{P4}) and so on.

To produce $4 V_{dc}$ output voltage, S_{P1}, S_{P2}, S_{P3} and S_{P4} have to be working.

To produce $0 V_{dc}$ output voltage, S_{n1}, S_{n2}, S_{n3} and S_{n4} have to be working.

From these paths, the unavailability and frequency of failures can be calculated. For example, the mean time to failure (MTTF) for the overall system can be found adding the MTTFs of the paths.

IV. CASE STUDY

For purpose of illustration, the proposed method is applied on the generalized five-level converter shown in Fig. 5. The

failure rates of the components are taken from [13] and the calculation and the assumptions are shown below

A. Reliability of Converter Components

1) *Failure Rates of IGBTs*: Assumptions: IGBT quality: JANTXV; Environment: G_B ; Temperature: $50C^\circ$

From [13], $\lambda_b = 8.3 \times 10^{-3}$; $\pi_T = 1.9$; $\pi_Q = 0.7$; and $\pi_E = 1.0$. Therefore,

$$\lambda_{IGBT} = 11.039 \times 10^{-3} \text{ Failures/}10^6 \text{ hours}$$

2) *Failure Rates of Diodes*: Assumptions: Diode quality: JANTXV, switching case; Environment: G_B ; Temperature: $50C^\circ$; Electric stress factor: 0.5; Contact construction factor: Metallurgically Bended.

From [13], $\lambda_b = 1 \times 10^{-3}$; $\pi_T = 2.2$; $\pi_S = 0.19$; $\pi_C = 1.0$; $\pi_Q = 0.7$; and $\pi_E = 1.0$. Therefore,

$$\lambda_{diode} = 2.926 \times 10^{-4} \text{ Failures/}10^6 \text{ hours}$$

3) *Failure Rates of Capacitors*: Assumptions: Capacitor Type: CP, Capacitor, Fixed, Paper-Dielectric, Direct Current; Quality: R type; Environment: G_B ; Temperature: $50C^\circ$; Size: $1000 \mu F$; and Electric stress factor: 0.5.

From the [13], $\lambda_b = 3.7 \times 10^{-4}$; $\pi_T = 1.6$; $\pi_Q = 0.1$; $\pi_C = 1.9$; $\pi_v = 1.4$; $\pi_S R = 0.66$; and $\pi_E = 1.0$. Therefore,

$$\lambda_{CP} = 11.6923 \times 10^{-5} \text{ Failures/}10^6 \text{ hours}$$

Repair rate is assumed to be equal for all the components and equals $5.708 / 10^6 \text{ hours}$ or $0.05/\text{year}$.

B. Determination of Voltage Level Probabilities

The proposed method is implemented in MATLAB taking into consideration main switches and clamping switches for failing open and failing short.

The annualized Loss Of Load Probability (LOLP) and Loss Of Load Frequency for producing $0 V_{dc}$, $1 V_{dc}$, $2 V_{dc}$, $3 V_{dc}$ or $4 V_{dc}$ are shown in Table I.

TABLE I
ANNUALIZED LOLP AND LOLF FOR THE FIVE VOLTAGE LEVELS

Level No.	Level Voltage	LOLP	LOLF occ/year
1	$0 V_{dc}$	0.0076988706	3.3623381651
2	$1 V_{dc}$	0.0000371169	0.0296747258
3	$2 V_{dc}$	0.0000149613	0.0103278362
4	$3 V_{dc}$	0.0000371169	0.0296747258
5	$4 V_{dc}$	0.0076988706	3.3623381651

From Table I, if the load is designed to operate on level 5 ($4 V_{dc}$) and it is allowed for a short period of time to work on level 4 ($3 V_{dc}$), LOLP can be considered 3.712×10^{-5} instead of 7.699×10^{-3} and LOLF $2.967 \times 10^{-2} \text{ occ/year}$ instead of 3.362 occ/year which is one of the advantages of multi-level converters.

The results given in Table I shows only information about the overall converter Loss Of Load Probability and Loss of Load Frequency. From Table I one can not interpret the effects

of each component on converter reliability or in other words sensitivity. To address the effects of each component, we assumed that failure of one component occurs at a time and we considered its effect on overall converter reliability. From this analysis we found that the most critical components are the main switches and Diodes. For level 4, the most critical components are S_{P1} , S_{P2} , S_{P3} and S_{P4} . For level 1, the most critical components are S_{n1} , S_{n2} , S_{n3} , S_{n4} . In general, diodes (D_{P1} , D_{P2} , D_{P3} , D_{P4} , D_{n1} , D_{n2} , D_{n3} and D_{n4}) have less effect on the reliability of a converter than the IGBTs. The results are given in Tables II, III, IV and V.

TABLE II
ANNUALIZED LOLP AND LOLF FOR THE FIVE VOLTAGE LEVELS WITH
FAILURE OF S_{P1} , S_{P2} , S_{P3} OR S_{P4}

Level No.	Level Voltage	LOLP	LOLF occ/year
1	0 V_{dc}	0.0076988706	3.3623381651
2	1 V_{dc}	0.0019525625	0.8428517565
3	2 V_{dc}	0.0019525625	0.8428517565
4	3 V_{dc}	0.0076988706	3.3623381651
5	4 V_{dc}	1.0000000000	0.0000000000

TABLE III
ANNUALIZED LOLP AND LOLF FOR THE FIVE VOLTAGE LEVELS WITH
FAILURE OF S_{n1} , S_{n2} , S_{n3} OR S_{n4}

Level No.	Level Voltage	LOLP	LOLF occ/year
1	0 V_{dc}	1.0000000000	0.0000000000
2	1 V_{dc}	0.0076988706	3.3623381651
3	2 V_{dc}	0.0019525625	0.8428517565
4	3 V_{dc}	0.0019525625	0.8428517565
5	4 V_{dc}	0.0076988706	3.3623381651

TABLE IV
ANNUALIZED LOLP AND LOLF FOR THE FIVE VOLTAGE LEVELS WITH
FAILURE OF D_{P1} , D_{P2} , D_{P3} OR D_{P4}

Level No.	Level Voltage	LOLP	LOLF occ/year
1	0 V_{dc}	0.0002105235	0.0861127609
2	1 V_{dc}	0.0000555546	0.0210999858
3	2 V_{dc}	0.0000555546	0.0210999858
4	3 V_{dc}	0.0002105235	0.0861127609
5	4 V_{dc}	1.0000000000	0.0000000000

TABLE V
ANNUALIZED LOLP AND LOLF FOR THE FIVE VOLTAGE LEVELS WITH
FAILURE OF D_{n1} , D_{n2} , D_{n3} OR D_{n4}

Level No.	Level Voltage	LOLP	LOLF occ/year
1	0 V_{dc}	1.0000000000	0.0000000000
2	1 V_{dc}	0.0002105235	0.0861127609
3	2 V_{dc}	0.0000555546	0.0210999858
4	3 V_{dc}	0.0000555546	0.0210999858
5	4 V_{dc}	0.0002105235	0.0861127609

V. CONCLUSION

Many methods are available in the literature to evaluate engineering systems reliability. Many of them can be applied on two state systems. Also, some methods can be used for multi state systems. However, power electronic converters not only have multi state operating conditions, but also their states are discrete states and the system can continue working in the presence of some faults. Also, in most power electronic applications, there is no need to build the reliability block diagram to analyze their reliability. In this work, minimal path set method is utilized in evaluating multilevel converter reliability. The proposed method traces the faulted components directly from the circuit configuration. The proposed method is applied on a five-level converter for illustration.

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