LM139/LM239/LM339/LM2901/LM3302
Low Power Low Offset Voltage Quad Comparators

General Description
The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic—where the low power drain of the LM339 is a distinct advantage over standard comparators.

Advantages
- High precision comparators
- Reduced VOS drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features
- Wide supply voltage range
  - LM139 series, 2 V DC to 36 V DC or ±1 V DC to ±18 V DC
  - LM139A series, LM2901 2 V DC to 28 V DC
  - or ±1 V DC to ±14 V DC
- Very low supply current drain (0.8 mA) independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ±5 nA and offset voltage ±3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Connection Diagrams

See NS Package Number J14A
Order Number LM339AM, LM339M or LM2901M
See NS Package Number M14A
Order Number LM339N, LM339AN, LM2901N or LM3302N
See NS Package Number N14A

*Available per JM38510/1/201
**Available per SMD # 9562-8873901

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## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 10)

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<tr>
<td>Supply Voltage, V+</td>
<td>36 VDC or ±18 VDC</td>
<td>28 VDC or ±14 VDC</td>
<td>Operating Temperature Range</td>
<td>LM339/LM339A</td>
<td>0°C to +70°C</td>
<td>LM239/LM239A</td>
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<td>Differential Input Voltage (Note 8)</td>
<td>−0.3 VDC to 36 VDC</td>
<td>−0.3 VDC to 28 VDC</td>
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<td>Input Voltage</td>
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<tr>
<td>Input Current (VIN &lt; −0.3 VDC), (Note 3)</td>
<td>50 mA</td>
<td>50 mA</td>
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<td>Power Dissipation (Note 1)</td>
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<tr>
<td>Molded DIP</td>
<td>1050 mW</td>
<td>1050 mW</td>
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<td>Cavity DIP</td>
<td>1190 mW</td>
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<td>Small Outline Package</td>
<td>760 mW</td>
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<td>Output Short-Circuit to GND, (Note 2)</td>
<td>Continuous</td>
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<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
<td>−65°C to +150°C</td>
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<tr>
<td>Lead Temperature (Soldering, 10 seconds)</td>
<td>260°C</td>
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## Electrical Characteristics

(V+ = 5 VDC, TA = 25°C, unless otherwise stated)

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<tbody>
<tr>
<td>Input Offset Voltage</td>
<td>(Note 9)</td>
<td>1.0</td>
<td>2.0</td>
<td>1.0</td>
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<td>5.0</td>
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<tr>
<td>Input Bias Current</td>
<td></td>
<td>25</td>
<td>100</td>
<td>25</td>
<td>250</td>
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<tr>
<td>Input Offset Current</td>
<td></td>
<td>3.0</td>
<td>25</td>
<td>5.0</td>
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<td>3.0</td>
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<tr>
<td>Input Common-Mode Voltage Range</td>
<td>V+ = 30 VDC (LM3302, V+ = 28 VDC)</td>
<td>0 V+ − 1.5</td>
<td>0</td>
<td>V+ − 1.5</td>
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<td>V+ − 1.5</td>
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<td>Supply Current</td>
<td></td>
<td>0.8</td>
<td>2.0</td>
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<td>Voltage Gain</td>
<td></td>
<td>50</td>
<td>200</td>
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<td>200</td>
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<td>200</td>
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<td>Large Signal Response Time</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>ns</td>
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<td>Response Time</td>
<td></td>
<td>1.3</td>
<td>1.3</td>
<td>1.3</td>
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<tr>
<td>Output Sink Current</td>
<td></td>
<td>6.0</td>
<td>16</td>
<td>6.0</td>
<td>16</td>
<td>6.0</td>
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### Electrical Characteristics \((V^+ = 5\, V_{DC},T_A = 25^\circ C,\text{ unless otherwise stated})\) (Continued)

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<tr>
<td>Saturation Voltage</td>
<td>(V_{IN}(-) = 1, V_{DC}, V_{IN}(+) = 0, I_{SINK} \leq 4, mA)</td>
<td>250</td>
<td>400</td>
<td>250</td>
<td>400</td>
<td>250</td>
<td>400</td>
<td>250</td>
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<tr>
<td>Output Leakage Current</td>
<td>(V_{IN}(+) = 1, V_{DC}, V_{IN}(-) = 0, V_O = 5, V_{DC})</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
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### Electrical Characteristics \((V^+ = 5.0\, V_{DC},\text{ Note 4})\)

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<tr>
<td>Input Offset Voltage</td>
<td>(Note 9)</td>
<td>4.0</td>
<td>4.0</td>
<td>9.0</td>
<td>9.0</td>
<td>9</td>
<td>15</td>
<td>40             mV_{DC}</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>(I_{IN}(-) - I_{IN}(+) = 0), (V_{CM} = 0)</td>
<td>100</td>
<td>150</td>
<td>100</td>
<td>150</td>
<td>50</td>
<td>200</td>
<td>300            nA_{DC}</td>
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<tr>
<td>Input Bias Current</td>
<td>(I_{IN}(+) ) or (I_{IN}(-) ) with Output in Linear Range, (V_{CM} = 0) (Note 5)</td>
<td>300</td>
<td>400</td>
<td>300</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>1000           nA_{DC}</td>
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<tr>
<td>Input Common-Mode Voltage Range</td>
<td>(V^+ = 30, V_{DC}) (LM3302), (V^+ = 28, V_{DC}) (Note 6)</td>
<td>0</td>
<td>(V^+ - 2.0)</td>
<td>0</td>
<td>(V^+ - 2.0)</td>
<td>0</td>
<td>(V^+ - 2.0)</td>
<td>(V^+ - 2.0) (V_{DC})</td>
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<tr>
<td>Saturation Voltage</td>
<td>(V_{IN}(-) = 1, V_{DC}, V_{IN}(+) = 0, I_{SINK} \leq 4, mA)</td>
<td>700</td>
<td>700</td>
<td>700</td>
<td>700</td>
<td>400</td>
<td>700</td>
<td>700             mV_{DC}</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>(V_{IN}(+) = 1, V_{DC}, V_{IN}(-) = 0, V_O = 30, V_{DC}) (LM3302), (V_O = 28, V_{DC})</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0             (\mu A_{DC})</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>Keep all (V_{IN})’s (\geq 0, V_{DC}) (or (V^-), if used), (Note 8)</td>
<td>36</td>
<td>36</td>
<td>36</td>
<td>36</td>
<td>36</td>
<td>36</td>
<td>28             (V_{DC})</td>
</tr>
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**Note 1:** For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the “ON-OFF” characteristic of the outputs keeps the chip dissipation very small \(P_D = 100\, mW\), provided the output transistors are allowed to saturate.

**Note 2:** Short circuits from the output to \(V^+\) can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of \(V^+\).

**Note 3:** This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as an input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the \(V^+\) voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than \(-0.3\, V_{DC}\) (at 25°C).

**Note 4:** These specifications are limited to \(-55^\circ C \leq T_A \leq 125^\circ C\) for the LM139/LM339A. With the LM239/LM239A, all temperature specifications are limited to \(-40^\circ C \leq T_A \leq 85^\circ C\). For LM3302, \(V_{O} = 30\, V_{DC}\), and over the full input common-mode range \((0\, V_{DC} \leq V_{CM} \leq 1.5\, V_{DC})\), at 25°C.

**Note 5:** The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

**Note 6:** The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode range is \(V^+ - 1.5\, V_{DC}\) at 25°C, but either or both inputs can go to \(+30\, V_{DC}\) without damage \((25\, V_{DC}\) for LM3302), independent of the magnitude of \(V^+\).

**Note 7:** The response time specified is a \(100\, mV\) input step with 5\, mV overdrive. For larger overdrive signals 300\, ms can be obtained, see typical performance characteristics section.

**Note 8:** Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than \(-0.3\, V_{DC}\) (for 0.3\, V_{DC} below the magnitude of the negative power supply, if used) at 25°C.

**Note 9:** At output switch point, \(V_O = 1.4\, V_{DC}\), \(R_S = 0\, ohm\) with \(V^+\) from 5\, V_{DC} to 30\, V_{DC} and over the full input common-mode range \((0\, V_{DC} \leq V_{CM} \leq 1.5\, V_{DC})\), at 25°C. For LM3302, \(V^+\) from 5\, V_{DC} to 28\, V_{DC}.

**Note 10:** Refer to RETS139AX for LM139A military specifications and to RETS139X for LM139 military specifications.

- Supply Current
- Input Current
- Output Saturation Voltage

Response Time for Various Input Overdrives—Negative Transition

Response Time for Various Input Overdrives—Positive Transition

Typical Performance Characteristics LM2901

- Supply Current
- Input Current
- Output Saturation Voltage

Response Time for Various Input Overdrives—Negative Transition

Response Time for Various Input Overdrives—Positive Transition

TL/H/5708–6

TL/H/5708–7
Application Hints

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to $< 10 \text{k}\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded. The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 VDC to 30 VDC. It is usually unnecessary to use a bypass capacitor across the power supply line.

Typical Applications ($V^+ - 5.0 \text{VDC}$)

- Basic Comparator
- Driving CMOS
- Driving TTL
- AND Gate
- OR Gate

The differential input voltage may be larger than $V^+$ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3 \text{VDC}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the $V^+$ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of $V^+$) and the $\beta$ of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω $R_{SAT}$ of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

![Diagram of application circuits](image-url)
Typical Applications \((V^+ = 15 \, V_{DC})\) (Continued)

**One-Shot Multivibrator**

**Bi-Stable Multivibrator**

**One-Shot Multivibrator with Input Lock Out**
Typical Applications \((V^+ = 15 \text{ V}_{\text{DC}})\) (Continued)

Large Fan-In AND Gate

Pulse Generator

ORing the Outputs

* FOR LARGE RATIO OF R1/R2, D1 CAN BE OMITTED.
Typical Applications ($V^+ = 15V_{DC}$) (Continued)

**Time Delay Generator**

![Diagram of Time Delay Generator with labeled components and waveforms showing input and output voltages over time.]

**Non-Inverting Comparator with Hysteresis**

![Diagram of Non-Inverting Comparator with labeled components and waveforms showing input and output voltages.]

**Inverting Comparator with Hysteresis**

![Diagram of Inverting Comparator with labeled components and waveforms showing input and output voltages.]

TL/H/5706–14
TL/H/5706–18
TL/H/5706–19
Typical Applications \( (V^+ - 15 \text{ V}_{\text{DC}}) \) (Continued)

**Squarewave Oscillator**

Typical circuit diagram showing a squarewave oscillator with components labeled as follows:
- \( V^+ \)
- \( 75 \, \text{pF} \)
- \( 100k \)
- \( 100k \)
- \( 4.3k \)
- \( \frac{1}{4} \text{LM320} \)
- \( V^0 \)
- \( f = 100 \, \text{kHz} \)

**Comparing Input Voltages of Opposite Polarity**

Typical circuit diagram showing two comparators with input voltages of opposite polarities.
- \( +V_{\text{IN}} \)
- \( -V_{\text{IN}} \)
- \( 100k \)
- \( 100k \)
- \( 2N2222 \)
- \( 1/4 \text{LM320} \)
- \( V^0 \)

**Basic Comparator**

Circuit diagram showing the basic comparator component.
- \( +V_{\text{IN}} \)
- \( -V_{\text{IN}} \)
- \( 3k \)
- \( 1/4 \text{LM320} \)
- \( V^0 \)

**Output Strobing**

Circuit diagram showing output strobing.
- \( +V_{\text{IN}} \)
- \( -V_{\text{IN}} \)
- \( 0.2k \)
- \( 1/4 \text{LM320} \)
- \( V^0 \)
- \( \text{STROBE INPUT} \)

**Limit Comparator**

Circuit diagram showing a limit comparator.
- \( +V_{\text{IN}} \)
- \( -V_{\text{IN}} \)
- \( 2R_s \)
- \( R_s \)
- \( +V_{\text{REF}} \)
- \( -V_{\text{REF}} \)
- \( 2N2222 \)
- \( 1/4 \text{LM320} \)
- \( V^0 \)

**Crystal Controlled Oscillator**

Circuit diagram showing a crystal controlled oscillator.
- \( +V_{\text{IN}} \)
- \( -V_{\text{IN}} \)
- \( 200k \)
- \( 100k \)
- \( 2.0k \)
- \( 0.1 \, \mu \text{F} \)
- \( \text{CRYSTAL} \)
- \( f = 100 \, \text{kHz} \)

*Or open-collector logic gate without pull-up resistor*
Typical Applications \((V^+ = 15 \text{ V}_{\text{DC}})\) (Continued)

Two-Decade High-Frequency VCO

\[ V = 5 \text{ V}_{\text{DC}}, \quad +V_2 = 2.4 \text{ V}_{\text{DC}}, \quad +V_1 = 3.6 \text{ V}_{\text{DC}}. \]

\[ 700 \text{ Hz} < f_0 < 100 \text{ kHz}. \]
Typical Applications \((V^+ = 5 \, V_{DC})\) (Continued)

Transducer Amplifier

Zero Crossing Detector (Single Power Supply)

Split-Supply Applications \((V^+ = +15 \, V_{DC} \text{ and } V^- = -15 \, V_{DC})\)
Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$) (Continued)

Zero Crossing Detector

Comparator With a Negative Reference

Schematic Diagram