Digital Counter/Timers and How They Work

Counter/Timer Logic can be represented schematically as shown below,

Clock Timers use a Source to increment a Counter. Whenever the counter increments past its maximum value, an Overflow is generated which pulses the counter Out. The Gate is used to enable or disable the clock function.

Clock Timers can be used for many types of time keeping and/or event counting functions.

**To Count Events:**
- a) Disable Gate to turn off Counter.
- b) Connect Event signal to Source
- c) Load Counter with Zero.
- d) Enable Gate to turn on counter.
- e) Read event count from Counter

**To Time Events:**
- a) Connect a known frequency pulse train to the Source to increment the counter.
- b) Disable the Gate to stop the Counter.
- c) Load the Counter with zero.
- d) Enable the gate when the event starts and Disable the gate at the end of the event.
- e) Read the Counter contents. Event time = Count/Timebase.
LabVIEW “Easy I/O” Counter-Timer VI’s

Count Events or Time.vi
Counts events (rising or falling edges on counter’s SOURCE pin) or elapsed time. You will typically place the VI in a loop. Set start/restart on the first call and set stop on the last call. To count events, set the event source/timebase to 0.0.

Measure Frequency.vi
Measures the frequency of a TTL signal on the specified counter’s SOURCE pin. In addition to this connection, you must wire the counter’s GATE pin to counter-1’s OUT pin. This VI is useful for relatively high frequency signals.

Measure Pulse Width or Period.vi
Measures the pulse width (length of time a signal is high or low) or period (length time between adjacent rising or falling edges) of a TTL signal connected to the counter’s GATE pin.