Exam 2-Solutions  

**ECE 410**

*During this exam you are allowed to use a calculator and the equations sheet provided. You are not allowed to speak to or exchange books, papers, calculators, etc. with other students.*

Total Points: 100  
Time: 60 minutes (11:30pm – 12:30pm)

- Write your name at the top of the exam and your initials at the top of each sheet.
- Note the point value of each question and try to at least attempt each problem. Partial credit will be given for all problems involving calculations.
- Show all of your work. Try to use only the pages provided (write on back if necessary)
- Give units in your answers.
- Sign the honor pledge at the bottom of this page. Unsigned exams will not be graded.

**True or False:** For each of the following statements, circle T if it is true and F if it is false.  
 **2 pts. each.**

| T | F | 1. To set the switching threshold (midpoint) voltage, Vm, to VDD/2 in a CMOS inverter, the pMOS transistor must be wider than the nMOS. |
| T | F | 2. The most significant parameter in CMOS power consumption is the supply voltage, VDD. |
| T | F | 3. Increasing power supply voltage, VDD, will decrease the speed performance of CMOS gates. |
| T | F | 4. The best way to improve the speed performance of a CMOS circuit is to decrease the channel width. |
| T | F | 5. For adding large words (e.g., 32-bit), a ripple carry adder will be much faster than a carry look-ahead adder. |
| T | F | 6. The D-flip flop provides synchronous data storage and is used to create registers, counters and other useful digital functions. |
| T | F | 7. For the best speed performance in a 6T SRAM cell, the access transistor must have a larger width (W). |
| T | F | 8. A FET-programmable ROM uses a contact layer mask to set data values in the memory array. |
| T | F | 9. In the field of semiconductors, MEMS stands for Micro Environmental Motor Sensors. |
| T | F | 10. The added cost and complexity of BiCMOS process is only justified if large output currents are needed. |

**Honor Pledge**

*By signing below, I pledge that I have neither given nor received aid on this exam, nor have I witnessed any other student giving or receiving aid.*
**Multiple Choice:** In the box beside each question, write the letter for the ONE answer that best fits the question/statement. **3 pts. each.**

12. Which of the following is a factor in CMOS total power consumption?
   A) average switching frequency  
   B) threshold voltage  
   C) transistor resistance  
   D) number of substrate contacts

11. Which of the following circuits should have the **slowest** average **rise time**?
   A) INV  
   B) NOR2  
   C) NAND2  
   D) NAND3

14. Adding buffers to a CMOS circuit will do which of the following?
   A) reduce power consumption  
   B) minimize chip size  
   C) improve signal rise/fall times  
   D) add a large capacitive load

13. Which of the following functions are not commonly included in an ALU?
   A) addition  
   B) count up/down  
   C) increment  
   D) logic AND

16. Which of the following is an **advantage** of BiCMOS over static CMOS?
   A) power consumption  
   B) cost per chip  
   C) functions per chip area  
   D) switching speed

15. Which type of memory is non-volatile with bit data that can be re-written?
   A) EPROM  
   B) SRAM  
   C) ROM  
   D) none of the above

17. **CMOS Logic Functions:**  **7 points**
   Draw the CMOS schematic for the function:
   \[ F = xy + z \]
Calculation: Solve the following problems in the space provided and on the backs of these pages if necessary. You must show ALL major steps on these test pages. Unless otherwise noted, for all problems assume minimum feature size $= 2\lambda = 0.6\mu m$, and $VDD = 3V$.

18. CMOS DC Timing Characteristics: 18 points
Answer the following questions based on the circuit shown to the right.

a) If $Vx = 0V$, what logic function is implemented?

Answer: INV

b) What is $V_{OL}$ if $Vx = 0V$?

$V_{OL} = |Vtp|

Answer: $V_{OL} = 0.5V$

c) Is $V_{OH} = VDD$ if $Vx=0V$? Briefly explain your answer.

Answer: NO
Explain:

M2 is always on and will pull the output low when M1 is on $\Rightarrow$ VOH always less than VDD.

d) If $Vx = 0V$, write an expression for the gate switching threshold, $V_m$

i) What is the region of operation of M1?

Region: Saturation

ii) What is the region of operation of M2?

Region: Saturation since VSG=VSD

iii) Write an expression that could be solved to find $V_m$ (do not evaluate the expression, just write it). Your expression should be ONLY in terms of $V_m$, VDD, Vtp, $\beta_1$, and $\beta_2$.

Note, $\beta = \mu Cox W/L$

$I_{D1} = I_{D2} \Rightarrow \frac{\beta_1}{2} (V_{SG1} - |V_{tp}|)^2 = \frac{\beta_2}{2} (V_{SG2} - |V_{tp}|)^2$

$\Rightarrow \beta_1 (V_{DD} - Vm - |V_{tp}|)^2 = \beta_2 (Vm - |V_{tp}|)^2$

e) How can this circuit be modified to maximize the output voltage swing (i.e., get $V_{OH}$ close to VDD and $V_{OL}$ close to ground)? Explain briefly

i) in terms of size parameter (W, L) for transistors M1 and/or M2?

$V_{OL} = |Vtp|$, can not be changed

$V_{OH}$ can be raised by decreasing the W/L ratio of M2 or increasing W/L of M1

ii) Are there any other circuit parameters that can be modified to improve output voltage swing?

Increasing $Vx (> 0V)$ will make current in M2 weaker and allow $V_{OH}$ to go higher.
19. **CMOS Transient Timing Characteristics:** [18 points]

This problem refers to the schematic of a digital circuit shown to the right. Although a pMOS load has been used to simplify the circuit, you can assume that the nMOS network functions like a typical static CMOS gate.

a) Write an expression for the output capacitance in terms of parasitics components $C_{gs}$, $C_{gd}$, $C_{sb}$, and $C_{db}$ and output load capacitance $C_L$. Specify the transistor for each component using the notation $C_{gsA}$, $C_{sbB}$, etc.

**EXPRESSION:** $C_{out} = C_L + C_{gdA} + C_{gdB} + C_{gdP} + C_{dbA} + C_{dbB} + C_{dbP}$

b) In the table below, identify the logic value combination(s) for inputs A, B, C, and D that would produce the **worst case fall time**. Assume all transistors are the same size.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>worst case fall time</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>worst case fall time (if more than one)</td>
<td>0</td>
<td>1</td>
<td>1</td>
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</tbody>
</table>

c) In the table below, identify the logic value combination(s) for inputs A, B, C, and D that would produce the **best case fall time**. Assume all transistors are the same size.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>best case fall time</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>best case fall time (if more than one)</td>
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d) If all transistors are the same size with $R_n=500\Omega$, what is the **fall time** ($t_f=2.2\tau_n$) if $C_{out}=50\text{fF}$ and $C_x=10\text{fF}$ for the transition $ABCD=0100$ to $ABCD=0111$?

$$\tau_n = C_{out}(R_n+R_n/2)+C_x(R_n/2) = 50(1.5)(500)+10(500)/2 = 40,000\times10^{-15}$$

$$t_f = 2.2(40\times10-12) = 88 \text{ psec}$$

$$t_f = 88 \text{ [psec]}$$

e) Write a simplified expression for the falling-time time constant, $\tau_n$, in terms of $C_{out}$, $C_x$, and $R_n$ for the transition $ABCD=0100$ to $ABCD=1110$ if $R_A=4R_n$, $R_B=3R_n$ and $R_C=R_D=R_n$.

$$\tau_n = C_{out}(4R_n|||3R_n+R_n))+C_x(R_n) = 2C_{out}R_n + C_xR_n$$

**EXPRESSION:** $\tau_n = 2C_{out}R_n + C_xR_n$
20. CMOS Arithmetic and Logic Gates: 9 points

a) Complete the truth table for a 2/4 active-low decoder.

<table>
<thead>
<tr>
<th>S1</th>
<th>S0</th>
<th>d3</th>
<th>d2</th>
<th>d1</th>
<th>d0</th>
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<tbody>
<tr>
<td>0</td>
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</table>

c) Complete the truth table for a 1-bit binary full-adder with inputs x, y and Cin.

<table>
<thead>
<tr>
<th>x</th>
<th>y</th>
<th>Cin</th>
<th>Sum</th>
<th>Cout</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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b) A 4-bit shift/rotate register has outputs F3-F0. What are the outputs in terms of inputs A3-A0 after performing the SHIFT_RIGHT function two times?

<table>
<thead>
<tr>
<th>F3</th>
<th>F2</th>
<th>F1</th>
<th>F0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>A3</td>
<td>A2</td>
</tr>
</tbody>
</table>

21. CMOS Memory: 10 points

A CMOS memory cell uses one nMOS access transistor and a storage capacitor to save data.

a) What type of memory is this?

ANSWER: DRAM

b) If the nMOS access transistor has Vtn=0.6V and μn = 500cm²/V, what is the maximum voltage that can be stored with VDD=3V?

\[ V_{max} = 2.4 \] [V]

c) 1x10⁻¹³ coulombs of charge are stored on this cell at a max storage voltage = 2.5V. If the minimum cell readout voltage is 0.5V, what is the maximum allowable leakage current for a hold time of 1μsec?

\[ Cs=Q_{max}/V_{max} = 10^{-13}/2.5 = 4x10^{-14}=40fF \]

\[ I_L = Cs(dV)/\tau_h = 40f \times (2.5-.5) / 1\mu = 80nA \]

\[ I_L (max) = 80 \] [nA]

d) If the minimum voltage after charge leakage on the cells is 1V, what is the final bit line voltage if Cs = 30fF and Cbit = 0.27pF?

\[ V_f = V_{min}(Cs)/(Cs+Cbit) = 1(30f)/(30+270f) = 0.1V \]

\[ V_f = 0.1 \] [V]
Equations Sheet

<table>
<thead>
<tr>
<th>V = I R</th>
<th>Q = C V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 = Q / t</td>
<td></td>
</tr>
</tbody>
</table>

n p = n_i^2 
σ = q(μ_n n + μ_p p)

R = L/σA 
Jx = σ Ex

Cox = ε_o x / t_ox
Qc = -C_D(V_G - V_m)

β_n = μ_n Cox (W/L) 
R_n = 1 / β_n [(V_DDD - Vtn)]

I_D = I_s (e^((V_D / V_T) - 1), \Psi_0 = V_T \ln \left( \frac{N_A N_D}{n_i^2} \right)
W = \left[ \frac{2e(\Psi_0 + V_R) N_D + N_A}{q N_D N_A} \right]^{1/2}

C_s = A \left( \frac{q e N_A N_D}{2(N_A + N_D)} \right)^{1/2} \left( \frac{1}{\sqrt{\Psi_0 + V_R}} \right)
W \approx x_p = \left[ \frac{2e(\Psi_0 + V_R)}{q N_A} \right]^{1/2}, W \approx x_n = \left[ \frac{2e(\Psi_0 + V_R)}{q N_D} \right]^{1/2}

C_{SB} = C_j A_{Sho} + C_{Ssw} C_{DB} = C_j A_{Dbot} + C_{Ssw} P_{Dsw}
C_{GS} = \frac{1}{2} C_G C_{GD} = \frac{1}{2} C_G

\tau_r = 2.2 \tau_n, \quad \tau_r = 2.2 \tau_p

t_p = 0.35(\tau_n + \tau_p)

DRAM: t_h = (C_s / I_L)(AVs)/f_refresh = 1 / 2t_h

region | nMOS equations | pMOS equations |
--------|----------------|----------------|
Cutoff | I_D = 0 | |
Triode | \[ I_D = \frac{\mu_n C_{OX}}{2} W \left[ 2(V_{GS} - V_m) V_{DS} - V_{DS}^2 \right] \] | \[ I_D = \frac{\mu_p C_{OX}}{2} W \left[ 2(V_{SG} - V_{QP}) V_{SD} - V_{SD}^2 \right] \]
Saturation (Active) | \[ I_D = \frac{\mu_n C_{OX}}{2} W (V_{GS} - V_m)^2 \] | \[ I_D = \frac{\mu_p C_{OX}}{2} W (V_{SG} - V_{QP})^2 \]

k' P = \mu n C_{OX} 
\beta = \mu C_{OX} W / L

Constants

kT = 0.026 eV, at room temperature
k = 8.62x10^-5 eV/K, Boltzman’s constant
V_T = 0.026 V, thermal voltage
q = 1.6x10^-19 C (coulombs)
n_i = 1.45x10^10 cm^-3, Si at room temperature
\epsilon_0 = 8.85x10^-14 F/cm
\epsilon_{OX} = (3.9) 8.85x10^-14 F/cm
\epsilon_{Si} = (11.8) 8.85x10^-14 F/cm

Quadratic Equation:
ax^2 + bx + c = 0 \Rightarrow x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}

DeMorgan’s Rules

(a * b)' = a' + b'
(a + b)' = a' * b'

Useful Logic Properties

1 + x = 1 \quad 0 + x = x
1 * x = x \quad 0 * x = 0
x + x' = 1 \quad x * x' = 0
a * a = a \quad a + a = a
ab + ac = a (b+c)

properties which can be proven
(a+b)(a+c) = a+bc \quad a + a'b = a + b
a + ab +ac = a