2/15/12 - Please turn in your check-ins, extra credit assignments and homework #4 in three separate piles, and pick up HW#5 and the exam 1 review question handout.

**WARM UP** - Today is more of a "wrap-up": one last topic from Ch 6 that we need to cover:

**Short Channel Effect**: Reducing the size of a transistor channel (L) reduces the threshold voltage $V_T$ a small amount:

![Diagram of semiconductor device showing channel length](image)

In short channels the effect is particularly notable, because of the proximity of the source and drain.

As an alternative to Body Biasing, Designers can control $V_T$ in very small transistor processes by increasing the channel length.

**Example**: In Intel's 65nm process, making tx's 10% longer
- Reduces $I_{on}$ by 10%
- Reduces $I_{off}$ by 300%!

The dual core Xeon processor uses longer txs almost exclusively in caches, and in 54% of the core gates.
Exam 1 Review Questions
as asked by you and your classmates on Monday's Check-In.

1. Will there be design problems, and how should I approach design problems?
This depends on how you define "design problems." There will be problems that require you to solve a problem that is different in some way from lecture and homework problems. Approach them systematically, as we have done in examples, and show all your work and reasoning, since partial credit is available for all calculation problems.

2. Are Transmission Gates CMOS?
I would say yes, since they are used in CMOS designs, and fabricated in the same process. It's a good question though - What argument is there against TGs being called CMOS?

* Not hooked to VDD or GND
* Complementary - Each input controls both an nFET and pFET which are not "on" simultaneously
* In a TG BOTH are "on" or BOTH are "off"
3. What parameter is determined by the width of the active layer? By the width of the poly trace?

\[ W: \text{Width of the } \uparrow \downarrow \text{tx channel} \]

\[ L: \text{Length of the } \uparrow \downarrow \text{tx channel} \]

4. How do I determine the logic gate order when it is not explicit from the parenthesis in an equation? 
   \textit{Add in parenthesis before transforming the equation, so that it makes sense.}

   \textbf{Example:}

   \[ f = \frac{(AB + CD)B + D}{((A \cdot B) + (C \cdot D)) \cdot B + D} \]

5. What is the linear model of a FET?

\[ \text{To determine these parameters, see HW #4 Problem 1 Solution} \]
Current and Subthreshold Leakage

6. What are the transistor operating regions, and the $I_{DS}$ in each of these regions? (N-FET)

$$I_D = \begin{cases} 
0 & V_{GS} < V_{TN} \quad \text{cutoff} \\
\frac{B_n}{2} (V_{DSAT} - \frac{V_{DS}}{2}) V_{DS} & V_{DS} < V_{DSAT} \quad \text{linear} \\
\frac{B_n}{2} (V_{DSAT}^2) & V_{DS} > V_{DSAT} \quad \text{saturation}
\end{cases}$$

$$V_{DSAT} = V_{GS} - V_{TN}$$

7. What equation should I use to find $I_D$ in cutoff?

This will generally be specified. Compared to the linear and saturation currents, $I_D \approx 0$ at cutoff. If asked to find the leakage current, use the expression we discussed in the last lecture:

$$I_{D_{leak}} = I_{D0} e^{\frac{V_{GS} - V_{TN}}{nVT}}$$
8. Explain the charging regimes in a MOSFET, including the difference between weak and strong inversion: \( \text{(nFET)} \)

**Accumulation:**

\[ V_{GS} < 0 \]  

\[ -V \]

- attracts positive holes

No current

**Depletion:**

\[ V_{GS} > 0 \] but "small"

\[ +V \]

Bulk charge left in depletion region

positive holes pushed away

**Weak Inversion:**

\[ V_{GS} < V_{Th} \]  

\[ +V < V_{Th} \]

Some electrons collect in channel \( \Rightarrow \) not enough for full conduction

**Strong Inversion:**

\[ V_{GS} > V_{Th} \]

Channel forms allowing conduction from source to drain
9. Does $V_{BS} = 0$ mean that $C_{GB} = 0$?

![Diagram of a transistor](image)

$V_{BS} = 0 \Rightarrow C_{GB} = ?$ Depends on $V_G$

So if $V_G > V_{Th} \Rightarrow$ channel

Physical Layout

$Q = \frac{CV}{Q_c} V_G$

$Q = \frac{CV}{Q_c} V_G$

10. Generate the output $f = \overline{ab + \overline{c}}$ using only NANDs, NORs, and INVs. You may use inverted outputs. How many transistors does your design require?

$f = \overline{ab + \overline{c}}$

$f = (a \cdot b) + \overline{c}$

$8$
11. Design a custom physical layout that produces the output \( f = ab + \overline{c} \). You may use inverted inputs. How many transistors does this custom design require?

\[
f = \left( (a \cdot b) + \overline{c} \right) \Rightarrow f = \left( (\overline{a} + \overline{b}) \cdot \overline{c} \right)
\]
12. Could I have done the physical layout in problem 11 by dividing up the poly traces like the diagram below, so that I wouldn’t be limited by the order I move through them in the Euler path?

Problems with this method:
You will need to connect the traces together, which will require poly contacts, which are higher resistance and so will reduce the speed of your gate.
The additional contacts will also need to fit in your cell, and could take up additional room, reducing the logic density.

Good design practices have 1 input port per input per cell, and where possible, employ a single poly trace per input to reduce resistance caused by poly contacts.

13. How do I approach a layout when an Euler path cannot be drawn that moves through both nMOS and pMOS transistors in the same order?
You will have to divide the active region. Divide it as few times as possible, and draw an Euler path for each region separately, for each Euler “region” move through the transistors in the same order in the n- and p-FETS, and then design your physical layout as you would for a single active region. Always use a single poly trace per input if possible.
Example: Draw the physical layout for $f = \frac{(AB + CD)E}{(A + B) + (C + D) + E}$ using split active regions.
For FRIDAY: Study for the exam
No check-in.

For MONDAY: Reading: 7.1-7.2 (if you haven't already)

Check-in: What characteristics can we determine about a gate by performing a DC analysis?