2/10/12 Please turn in your check-in assignment.

Reminder: Check-off Lab 3 by 4pm today. Brief Report is due Monday.

Warm Up/Common Mistakes from HW3

1. How many transistors are in each of these primitive gates?

- Inverter: 2
- NOR: 4
- NAND: 4

2. Draw the transistor level schematic for

\[ f = a + b(c+d) \] (Do bubble pushing to find the pFET Circuit) Draw an Euler graph. Draw an Euler path. Draw the physical layout.

\[ \bar{a} \left( \bar{b} + (\bar{c} \oplus \bar{d}) \right) = f \]
\text{GRAPH} (2)

\text{PATH}\n
\text{a} \to \text{b} \to \text{d} \to \text{c}

\text{VDD}\n
\text{GND}\n
\text{a} \xrightarrow{1} \text{b} \xrightarrow{1} \text{c} \xrightarrow{1} \text{d} \xrightarrow{1} \text{a}

\text{VDD}\n
\text{GND}\n
\text{a} \xrightarrow{3} \text{b} \xrightarrow{3} \text{c} \xrightarrow{3} \text{d} \xrightarrow{3} \text{a}

\text{VDD}\n
\text{GND}\n
\text{a} \xrightarrow{3} \text{b} \xrightarrow{3} \text{d} \xrightarrow{3} \text{c}
Channel length modulation

Problem: The reverse biased p-n junction at the drain effectively shortens the channel width

\[ L_{\text{eff}} = L - L_d \]

As channel length gets smaller, channel length modulation becomes more significant.

Often modeled with a parameter \( \lambda \):

\[
I_D = \frac{B}{2} V_{D\text{SAT}}^2 \left[ 1 + \lambda (V_{DSn} - V_{D\text{SAT}}) \right]
\]

\( \lambda \): Set to 0 for basic calculations
Gate Overlap

\[ L' = \text{Drawn Length} \]
\[ L_0 = \text{Overlap of gate} \]
\[ L = \text{channel length} \]
\[ L = L' - 2L_0 \]

**Leakage**

**Ideal:** When idle, CMOS gates draw 0 current and dissipate 0 power

**Real:** Some leakage even when "OFF"

*Subthreshold leakage*

Just below \( V_T \) (\( Vgs < V_T \)) is called "weak inversion"
- Some channel, but in an nFET the substrate is more strongly p-type than the channel is n-type
Subthreshold leakage increases significantly with $V_{ds}$

- Main source of leakage
  - $nA's$ per $\mu m$ of $tx$ width
  - within a 65nm process

As threshold voltage decreases to allow a lower $V_{dd}$, subthreshold leakage increases

Leakage also increases at high temperatures
$V_{DD}$ - velocity saturation/mobility degradation 
$\Rightarrow$ less current than expected at high $V_{DD}$
- No point in using high $V_{DD}$ for fast transistors
- Instead, $V_{DD}$ decreasing with each process generation to reduce power consumption
- Very short channels and thin gate oxides would be hurt by high $V_{DD}$
Reading Assignment: Get caught up to 7.2. Study for the exam. Do the extra credit assignment.

Check-In: Ask me a question to cover in a review for Exam 1. (You must ask a question, don't tell me you understand everything so far.)