2/8/12 Please turn in your check-in and HW #3 assignments in separate piles, and pick up HW #4

**WARM UP:** A CMOS process produces gate oxides with a thickness $t_{ox} = 100 \mu m$. The FET carrier mobility values are given as $\mu_n = 550 \text{ cm}^2/\text{V.s}$ and $\mu_p = 210 \text{ cm}^2/\text{V.s}$

a. Calculate the oxide capacitance per unit area in units of $\text{fF/um}^2$ (assume $\varepsilon_{ox} = 3.9 \varepsilon_0$)

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \cdot 8.85 \times 10^{-12} \text{ F/m}}{100 \times 10^{-10} \text{ m}} = 0.00345 \text{ F/m}^2$$

$$C_{ox} = 0.00345 \text{ F/m}^2 \times \frac{1 \text{ m}^2}{(1 \text{ um})(1 \text{ um})} = 3.45 \times 10^{-15} \text{ F/um}^2$$

**boxed**

$$C_{ox} = 3.45 \text{ fF/um}^2$$

b. Find the process transconductance values for nFETs and pFETs. Place your answer in units of $\mu A/\text{V}^2$

$$k'_n = \mu_n C_{ox} = (550 \times 10^{-4} \text{ m}^2/\text{V.s}) (0.00345 \text{ F/m}^2)$$

$$= 1.898 \times 10^{-4} \text{ F/V.s}$$

$$[\text{F/s}] = [\frac{1}{\text{A}}] = [\frac{\text{A}}{\text{V}}]$$

$$k'_n = 1.898 \times 10^{-4} \text{ A/V}^2$$

**boxed**

$$k'_n = 1.898 \mu A/\text{V}^2$$
NAND-BASED S-R Latch

NAND: $a \ b \ f$

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$S=1$ Hold
$S=0$ Reset

$Z = 1$ NOR BASED

$Z = 0$ NAND BASED
6.4 pFET Characteristics

Source: terminal closer to VDD connection
Drain: terminal closer to output terminal

Current definition is: source-to-drain

Inversion hole charge: \( Q_h \)
\[ Q_h = 0 \text{ for } (V_{S6p} < |V_{TP}|) \]
\[ Q_h \text{ exists for } (V_{S6p} > |V_{TP}|) \]

Gate capacitance: \( C_{Gx} = \frac{E_{ox}}{t_{ox}} \leq \text{still} \)

Currents: \( \text{pinch-off} \)
\[ V_{S6} > |V_{TP}| \]
\[ -V_{DG} \text{ GATE} \]
\[ V_{DG} < |V_{TP}| \]

\[ V_{DGSTA} = V_{S6p} - |V_{TP}| \]
\[ I_{SD} = \begin{cases} 
0 & \text{for } V_{SDP} < |V_{TP}| \text{ (cutoff)} \\
\beta \left( V_{DSATP} - \frac{V_{SDP}}{2} \right) V_{SDP} & \text{for } V_{SDP} < V_{DSAT} \text{ (linear)} \\
\frac{\beta}{2} \left( V_{DSATP} \right)^2 & \text{for } V_{SDP} > V_{DSAT} \text{ (saturation)}
\end{cases} \]

6.4.1 pFET parasitics

\[ R_P = \frac{1}{\beta_P \left( V_{DD} - |V_{TP}| \right)} \]

\[ \beta_P = k_p' \left( \frac{W}{L} \right) \text{ (larger aspect ratios give faster transistors)} \]

Gate capacitance: \[ C_{G_P} = C_{OX} \frac{W}{L} \]

\[ C_{GS} = C_{GD} = \frac{1}{2} C_G \]
Junction Capacitance:

\[ C_p = C_{jp} A_{bot} + C_{jsw} P_{sw} \]

Either \[ C_{sb} \quad \text{or} \quad C_{db} \]

But \[ C_{jp} \neq C_{jn} \]

Because of differences in doping

6.5 Modeling of Small MOSFETs

6.5.1 "Scaling Theory"

Notably: for a size reduction of 5 in \( V_{dd} \) (Voltage Scaling) you get a power consumption reduction of \( 5^2 \) (Assumes scaling voltages by same factor as transistor size)

Voltage Scaling - Desirable to use low \( V_{dd} \)

Tradeoffs: speed (?)

- \( V_t \) must allow it
Velocity Saturation

Recall that \( E = \frac{V_{ds}}{L} \)  
As \( L \) shrinks \( E \) gets large

\( E \) is important because it governs carrier velocity

\[ V = \mu E \]

\( \uparrow \)

Mobility

As \( V \) gets larger we see

- Increased carrier scattering
- Increased lattice scattering (phonon scattering)

The faster carriers go, more often they collide with carriers + lattice

\( \Rightarrow \) Maximum average speed

\( \Rightarrow \) Saturation velocity

\[ V \]

\[ V_s \]
Velocity is also important for transit time = time for a charge to cross the transistor channel

\[ \tau_t = \frac{V}{L} \Rightarrow \frac{V}{L} \leq \frac{V_s}{L} \text{ limit of switching speed} \]

\[ \tau_t = \frac{\mu E}{L} = \frac{\mu V_d s}{L^2} \]

Huge improvement in switching speed by decreasing L

But the saturation velocity mutes this somewhat
Reading Assignment: Ch 7.1-7.2

Check-In: What is fan-out and what effect does it have on the speed of an inverter?