2/6/12 Please turn in check-ins and lab #2 reports in separate piles.
Reminder: Homework #3 due Wednesday

WARM UP: Given an nFET with:
\[ \beta_n = 2.3 \text{ mA/V}^2, \quad V_{TN} = 0.76 \text{ V} \quad \text{and} \quad V_{DS_n} = 2 \text{ V} \]

Find \( I_D \) for:

a. \( V_{GS_n} = 1 \text{ V} \)
\[ V_{D-SAT} = V_{GS} - V_{TN} = 1 \text{ V} - 0.76 \text{ V} = 0.24 \text{ V} \]
\[ I_{D-SAT} = \frac{\beta}{2} \frac{V_{DSAT}}{2} = \frac{2.3 \text{ mA/V}^2}{2} (0.24 \text{ V})^2 \]
\[ I_D = 0.066 \text{ mA} \]

b. \( V_{GS_n} = 2 \text{ V} \)
\[ V_{D-SAT} = 2 \text{ V} - 0.76 \text{ V} = 1.24 \text{ V} \rightarrow SATURATION \]
\[ I_{D-SAT} = \frac{\beta}{2} \frac{V_{DSAT}}{2} = \frac{2.3 \text{ mA/V}^2}{2} (1.24 \text{ V})^2 \]
\[ I_D = 1.77 \text{ mA} \]

c. \( V_{GS_n} = 3 \text{ V} \)
\[ V_{D-SAT} = 3 \text{ V} - 0.76 \text{ V} = 2.24 \text{ V} \leftarrow \]
\[ I_D = \beta \left( V_{DSAT} - \frac{V_{DS}}{2} \right) V_{DS} = \frac{2.3 \text{ mA/V}^2}{2} (2.24 - \frac{2}{2})^2 \]
\[ I_D = 5.70 \text{ mA} \]
Ch 6.3 - The FET RC Model

Transistors are complicated and non-linear

⇒ simple model for predictive design

later, use full SPICE model for analysis

Drain-Source Resistance

\[ R_n = \frac{V_{DS_n}}{I_{DS_n}} \]

\( I_D \) is a function of \( V_{DS} \)

⇒ \( R_n \) is inherently non-linear

![Graph showing the relationship between \( I_{DS_n} \) and \( V_{DS_n} \)]
Point a: where $V_{DS}$ is very small

Channel assumed to be uniformly inverted

Derived $I_D$ for this case in Sect. 3.2

$$I_D = \beta_n (V_{gs} - V_{TH})(V_{DS}) = \beta_n V_{DSAT} V_{DS}$$

Point b:

Voltage attracting charge to channel is average of Drain and Source regions

$$I_D = \beta_n \left( V_{DSAT} - \frac{V_{DS}}{2} \right) V_{DS}$$

Use for all linear region calculations
Point C: Saturation

The $V_{DS}$ is treated as $V_{DSat}$

$$I_D = I_{D-SAT} = \frac{\beta_n}{2} V_{DSAT}^2$$

---

Note for all three approximations:

a: $I_D = \beta_n V_{DSAT} V_{DS}$

b: $I_D = \beta_n \left( V_{DSat} - \frac{V_{DS}}{2} \right) V_{DS}$

c: $I_D = \frac{\beta_n}{2} V_{DSAT}^2$

$I_D \propto \beta_n$, so $R_n = \frac{V_{DSn}}{I_{Dn}} \propto \frac{1}{\beta_n}$

A Device with a high transconductance has larger currents and lower resistance
\[ \beta_n = \frac{k_n'}{L} \] \text{ Geometry Dependant} \tag{5}

As transistors shrink they get faster (smaller L), and wider transistors (larger W) are also faster.

For simple modeling, we want ONE \( R_n \) expression:

We will use

\[ R_n = \frac{\eta}{\beta_n \left( V_{DD} - V_{TH} \right)} \]

\[ \frac{V_{DSAT}}{} \]

This is called "multiplying factor", no physical basis, in the lit. Varies from 1-6.

We will use \( \eta = 1 \) which means some \( R_n \) values will be small.

\[ R_n = \frac{1}{\beta_n V_{DSAT}} \]
Sect 6.3.2 Capacitances

Gate Capacitance: $C_6 = \text{Cox} \times A_6$

For a simple approximation:

\[ C_{GS} \quad \text{GATE} \quad C_{GD} \]

\[ \text{SOURCE} \quad \text{GATE} \quad \text{DRAIN} \]

Where $C_{GS} = C_{GD} \approx \frac{1}{2} C_6$
Junction Capacitance

Capacitance created by pn junctions and so found at every p-n interface including source and drain.

How does junction capacitance work?

Charge separated by a distance ⇒ capacitance

To estimate junction capacitance we might use:

\[ C = C_j A_{pn} \frac{1}{\text{Area of pn junction}} \]

Determined by process, varies with doping level.
Two issues:

1. C varies with voltage
   (ignore for now)

2. pn junction has both depth and area

   \[ \Rightarrow \text{for a simplified calculation, use the drawn geometry, and } x_j = \text{a given parameter (doping or junction depth)} \]

Each rectangle comprises a boundary between a p- and n-region
So \( A_{bot} = X \cdot W \) and 
\[
C_{bot} = C_j \cdot X \cdot W
\]

Sidewalls 
\[
C_{sw} = \text{sum of all sidewall caps.}
\]

\[
A_{sw} = 2(W \cdot x_j) + 2(X \cdot x_j)
\]
\[
= (2W + 2X) x_j
\]

\[
P_{sw}
\]

\( \text{side wall perimeter} \)

So 
\[
C_{sw} = C_{jsw} P_{sw}
\]

where \( C_{jsw} = C_j x_j \)

\( \text{sidewall capacitance per unit perimeter} \)

\[
C_{SB} = C_{SD} = C_{bot} + C_{sw}
\]
**Simple RC Model:**

\[ C_S = C_{GS} + C_{SB} \]
\[ C_D = C_{GD} + C_{DB} \]

**Linear Model:**
**EXAMPLE:** In last lecture's warm-up we found for a transistor with $t_{ox} = 90\,\text{Å}$

$$C_{ox} = 3.84 \times 10^{-7} \text{ F/cm}^2$$

with $W = 2\,\mu\text{m}$ and $L = 0.25\,\mu\text{m}$

we have $C_6 = 3.84 \times 10^{-7} (2 \times 10^{-4} \text{ cm})(0.25 \times 10^{-4} \text{ cm})$

$$C_6 = 1.92 \times 10^{-15} \text{ F} = 1.92 \,\text{fF}$$

$$C_{GS} = C_{GD} = \frac{1}{2} C_6 = 0.96 \,\text{fF}$$
Reading Assignment: Finish Ch. 6

Check-In: What is velocity saturation, and why does it occur in short-channel FETs?