1. a. Compute the device trans conductances: \( \beta = k' \left( \frac{W}{L} \right) \)

\[
\beta_p = 65 \mu A/V^2 \quad (8) = \frac{520 \mu A/V^2}{840 \mu A/V^2} \quad (6)
\]

b. Find the FET resistances: \( R = \frac{1}{\beta (V_{DD} - V_T)} \)

\[
R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})} = \frac{1}{(840 \mu A/V^2)(3.3 - 0.7)} = 458 \Omega
\]

\[
R_p = \frac{1}{\beta_p (V_{DD} - V_{Tp})} = \frac{1}{(520 \mu A/V^2)(3.3 - 0.8)} = 769 \Omega
\]

c. Find the rise time

\[
T_p = R_p C_{out} = (769 \Omega)(200 \text{fF}) = 153 \text{ps}
\]

\[
t_r = 2.2 T_p = 336.6 \text{ps}
\]

d. Find the fall time

\[
T_n = R_n C_{out} = (458 \Omega)(200 \text{fF}) = 91.6 \text{ps}
\]

\[
t_f = 2.2 T_n = 202 \text{ps}
\]

e. Find the max. signal frequency

\[
f_{\text{max}} = \frac{1}{t_r + t_f} = \frac{1}{(337 + 202) \times 10^{-12}} = 1.86 \text{ GHz}
\]

f. Find the average propagation delay

\[
\tau_p = 0.35 (T_n + T_p) = 0.35 \left( 91.6 \text{ps} + 153 \text{ ps} \right) = 85.6 \text{ps}
\]

g. Find the mid point voltage

\[
V_M = V_{DD} - \left| V_{Tn} \right| + \sqrt{\frac{P_n}{P_p}} V_{Tn} \quad \sqrt{\frac{P_n}{P_p}} = 1.271 \Rightarrow V_M = 3.3 - 0.8 + 1.271 \times 0.7
\]

\[
V_M = 1.493 \text{V}
\]
2/ \[ t_f = \ln \left( \frac{V_{DD}}{0.85 V_{DD}} \right) - \ln \left( \frac{V_{DD}}{0.85 V_{DD}} \right) \]

for 85% to 5% \( \uparrow \)

Time it takes to fall to 5% \( \uparrow \)

Time it takes to fall to 85%

\[ t_f = \ln \left( \frac{0.85}{0.05} \right) = 2.83 \ \ln \]

for 90% to 10% \( t_f \approx 2.2 \tau_n = 100 \text{ps} \Rightarrow \tau_n = 45.45 \text{ps} \)

So for 85% to 5%: \( t_f = 2.83 \times (45.45 \text{ps}) = 128.6 \text{ps} \)

3/ a. \( t_r = 2.2 \tau_p = 2.2 R_p C_{out} = 2.2 R_p (C_L + C_{FET}) \)

\[ C_{out} = 150 \text{ff} + 75 \text{ff} = 225 \text{ff} \]

\[ \tau_p = R_p C_{out} = (769 \Omega)(225 \text{ff}) = 173 \text{ps} \]

\[ t_r = 2.2 \tau_p = 2.2(173 \text{ps}) = 381 \text{ps} \]

b. \( t_f = 2.2 \tau_n \)

\[ \tau_n = \tau_1 + \tau_2 \leftarrow \text{Elmore formula} \]

\[ \tau_1 = C_{out} \cdot 2 R_n \]

\[ \tau_2 = C_X \cdot R_n \]

\[ \tau_n = C_{out} \cdot 2 R_n + C_X R_n \]

\[ = 225 \text{ff} \cdot 2 \cdot (458 \Omega) + 25 \text{ff} (458 \Omega) \]

\[ = 218 \text{ps} \]

\[ t_f = 2.2 \tau_n = 2.2 (218 \text{ps}) = 479 \text{ps} \]

C. \[ f_{\text{max}} = \frac{1}{t_r + t_f} = \frac{1}{(381 + 479) \times 10^{-12} \text{s}} = 1.16 \text{GHz} \]

d. \[ t_p = 0.35 (\tau_n + \tau_p) = 0.35 (218 \text{ps} + 173 \text{ps}) = 137 \text{ps} \]
3. /cont.

e. \( V_M = V_{DD} - |V_{T_P}| + \frac{\frac{\beta_n}{\beta_p}}{1 + \frac{1}{2} \sqrt{\frac{\beta_n}{\beta_p}}} V_{T_n} \)

\[ \sqrt{\frac{\beta_n}{\beta_p}} = 1.271 \Rightarrow \]

\[ V_M = 3.3 - 0.8 + \frac{\frac{1}{2} (1.271) 0.7}{1 + \frac{1}{2} (1.271)} = 1.80 \text{ V} \]

f. \( t_r = t_0 + \alpha_0 C_L \)

where \( t_0 = 2.2 R_P C_{FET} \leftarrow \) zero load delay

\( \alpha_0 = 2.2 R_P \leftarrow \) slope = \( C_L \) dependence

\[ t_f = t_1 + \alpha_1 C_L \]

where \( t_1 = 2.2 R_n (2 C_{FET} + C_x) \leftarrow \) intercept

\( \alpha_1 = 4.4 R_n \leftarrow \) slope

The two slopes are not the same, because the series connected nFETs increase the resistance of the path to ground for discharging \( C_{out} \). The inter-FET capacitance \( C_x \) increases the zero-load delay (intercept) but does not affect the load capacitance dependence.

9. MATLAB solution on separate page.
4. a. \( V_M = V_{DD} - |V_{TP}| + \frac{1}{3} \sqrt{\frac{\beta_n}{\beta_p}} \ V_{TN} \)

\[
= 3.3 - 0.8 + \frac{1}{3} \left( \frac{1.271}{0.7} \right) = \frac{1.9643 \ V}{1 + \frac{1}{3} (1.271)}
\]

Yes, \( V_M \) is farther to the right in the VTC, indicating that the input voltage has to be higher for the NAND3 output to switch from high to low than for the NAND2. This is because the 3-series-connected nFETs conduct current worse than the 2-series-connected nFETs in the NAND2 gate.

b. Worst case rise time: The worst case rise time for a NAND3 is when only one of the pFETs is "ON" to charge the output capacitance. Equivalent circuit:

This is the same as the NAND2 (and INV) worst case rise time circuit. The rise time will be about the same.

The additional pFET from an additional parallel connected pFET will make it slightly higher.
4. /cont. c. Worst case fall time: The output capacitance discharges through 3 series-connected nFETs:

Since the output capacitance now discharges through 3 nFETs instead of 2, and competes with 2 discharging inter-FET parasitic capacitances rather than 1, so it will be considerably slower.

5. The worst case path for pFETs is through 3 series connected pFETs. Since all the pFETs could be on this path, all should be sized $\beta_p = 3\beta_p = 3 \times$ size of inverter ref.

The worst case nFET paths are the three series paths to ground. The minimum sizes for each FET are given:

$\beta_n = 2\beta_N$