

# ECE 832

## ANALOG INTEGRATED CIRCUIT DESIGN

FALL 2005

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**COURSE:** M W F 12:40 pm - 1:30 pm Rm 119 Farrall Ag. Eng. Hall

**INSTRUCTOR:** G.M. Wierzba Room 3215 EB 355-5225; wierzba@msu.edu

**WEB SITE:** www.egr.msu.edu/~wierzba

**OFFICE HRS:** M W F 11 am - 12 pm or by appointment

**TEXTS:** G.M. Wierzba, *ECE 832 Course e-Notes, Fall 2005 Edition*, available at the Ag Hall Document Center (Room 47 Ag Hall).

Gray, Hurst, Lewis, & Meyer, *Analysis and Design of Analog Integrated Circuits*, Wiley, 2001

**GRADING:** Three one-hour exams (9/21, 10/19 and 11/16) 200 pts  
Final exam\* (Th, Dec.15 @ 12:45 - 2:45 pm) 200 pts  
Homework (normalized)\* 50 pts

\*You must obtain a passing grade to pass the course.

**POLICIES:** Article 2.3.3 of the Academic Freedom Report states that *the student shares with the faculty the responsibility for maintaining the integrity of scholarship, grades, and professional standards*. In addition, the Department of Electrical and Computer Engineering adheres to the policies on academic honesty as specified in General Student Regulations 1.0, Protection of Scholarship and Grades, and in the all-University Policy on Integrity of Scholarship and Grades, which are included in Spartan Life; Student Handbook and Resource Guide.

**HOMEWORK:** Homework is to be done on 8.5" x 11" paper using only one side. It must be stapled and ragged edges must be trimmed. Whenever possible, the correct answer is to be circled or boxed. You may **NOT** work with other students. The work you submit must be done by you. Assignments which are identical to any other student will all receive a grade of **zero**. You must type and run all of your own computer work. Copying of old assignments will be dealt with severely.

**OTHER:** Only simple scientific calculators are allowed for exams. Exam questions have little or no partial credit. There are **NO MAKE UP EXAMS**. One 1-hour exam will be dropped in computing your grade. Late homework **WILL NOT** be accepted. Your lowest homework grade will be dropped in computing your normalized homework grade.

*An 85% attendance rate is required to pass the course, that is, you can miss 7 classes. Please keep your own record of absences.*

## DETAILED TOPICS:

- Chapter 3: Single-Transistor and Multiple-Transistor Amplifiers
  - 3.2 Two-Port Modeling of Amplifiers  
Admittance Parameters, Impedance Parameters, Hybrid Parameter, Inverse Hybrid Parameters, Circuit Representation of Two-Port Networks.
  - 3.3 Basic Single-Transistor Amplifier Stages  
Small-Signal Model of a BJT, JFET and MOSFET, Common-Emitter Configuration, Common-Source Configuration
  - 3.4 Multiple-Transistor Amplifier Stages  
Darlington Pair
  - 3.5 Differential Pairs  
Bartlett's Bisection Theorem, Basic Differential Amplifier, Differential Gain, Common-Mode Gain, Input Resistance, Common-Mode Rejection Ratio, Current Source Biasing
  
- Chapter 1/2: Devices and SPICE Models
  - 1.5 Large-Signal Behavior of MOSFETs  
Transfer Characteristics, Shichman-Hodges Equations, SPICE Curve Tracer, Large-Signal SPICE Model, Small-Signal Model
  - 1.3 Large-Signal Behavior of Bipolar Transistors  
Transfer Characteristics, Eber-Moll Equations, Large-Signal SPICE Model, SPICE Curve Tracer, Small-Signal Model
  - 1.X Large-Signal Behavior of JFETs  
Transfer Characteristics, Device Equations, SPICE Curve Tracer, Large-Signal SPICE Model, Small-Signal Model
  - 1.Y FET - BJT Analogy
  
- Chapter 4: Current Mirror, Active Loads and References
  - 4.2 Current Mirrors  
Simple BJT Current Mirror, Model, MOSFET Current Mirror, Design and Simulation, Cascode BJT Current Mirror, Output Resistance, SPICE Verification, Cascode MOSFET Current Mirror, Design and Simulation, Swing Limits, Output Resistance, Wilson BJT Current Mirror, SPICE Verification
  - 4.3 Active Loads  
Complementary Load, Common-Emitter Amplifier, Common-Source Amplifier, Diode Connected Load - Common Source Amplifier, BJT Differential Pair with Current-Mirror Load, Operating Point, AC Differential Analysis, Symmetry, Output Resistance, Model, AC Common-Mode Analysis, Output Resistance, CMRR, Large-Signal Response, CMOS Differential Pair with Current-Mirror Load, Operating Point, AC Differential Analysis, Symmetry, Output Resistance, Model, AC Common-Mode Analysis, Output Resistance, CMRR, Large-Signal Response,
  - 4.4 Voltage and Current References  
MOSFET Voltage Divider, Design and Simulation, Biasing a Current Mirror

Chapter 6: Operational Amplifiers with Single-Ended Outputs

Chapter 7: Frequency Response of Integrated Circuits

Chapter 9: Feedback Response and Stability of Feedback Amplifiers

Chapter 11: Noise in Integrated Circuits