

RAVI KRISHNA SHAGA

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EDUCATION:

Aug 2008 – present **M.S. in Electrical and Computer Engineering,**
Michigan State University, East Lansing, Michigan.
GPA : 3.89 / 4.0

July 2004–May 2008 **Bachelor of Technology (Hons.) in Electrical Engineering**
Indian Institute of Technology, Kharagpur, India
GPA : 8.12 / 10.0

RESEARCH INTERESTS :

- Analog / Mixed-signal circuit design
- Learning in sigma-delta modulators
- Noise-shaping neural networks

RESEARCH EXPERIENCE:

- **Research Assistant, Adaptive Integrated Microsystems Lab, Michigan State University,** under the guidance of **Prof. Shantanu Chakrabartty.**
Applied Physics Laboratory (JHU) Project : Analog spectral feature extraction for a speaker verification system by using a Mel-frequency based band-pass filter bank. The complete system including biquad filter with center frequency tunable over the audible frequency range, rectifier, low pass filter and a $\Sigma\Delta$ modulator were designed and fabricated on AMIS 0.5 μ m CMOS process.
- **M.S. Thesis : “Resolution Enhancement in higher dimensional sigma-delta modulators”**
The work focuses on finding lower dimensional manifolds in higher dimensional data space and exploiting this data correlation between the different channels to achieve resolution enhancement by using an adaptive sigma-delta ADC learning algorithm.
- **BTech Thesis: “Reduced Order Modeling of Higher Order Systems”** under the guidance of Professor **J.Pal,** Department of Electrical Engineering, IIT Kharagpur. The project involves reducing a higher order system to a lower order system keeping the system performance intact by using Genetic Algorithms. The same model order reduction was also achieved through Markov parameter, Time moment and Impulse energy matching to ensure stability of the system.
- **Advanced VLSI Design Laboratory, IIT Kharagpur (May – June 2008)**
“Design and implementation of a N-bit Wallace tree multiplier” : The time complexity of the algorithm was successfully reduced from $O(n^2)$ to $O(n \log n)$ by introducing fast adders instead of ripple carry adders.

SUMMER INTERNSHIP:

Organization :	Signion Systems Pvt. Ltd. , Hyderabad, India.
Project Work:	“ <i>Optimization of Viterbi Algorithm used in SATCOM Demodulator</i> ”. The project, sponsored by Space Applications Center (SAC) - Ahmedabad, involved optimizing the viterbi code for both total run time and code space so as to facilitate the upgradation of the demodulator from continuous mode of operation to the burst mode of operation.
What I achieved:	The run time of the viterbi decoder module was successfully reduced by more than 25% and the total program run time by 20% in the worst case possible run time scenario and even under the severe compiler optimization limitations.

TERM PROJECTS:

- Design of a charge pump based decorrelation system using a sigma-delta learner.
- End-to-end design of a basic *Pulse-Amplitude-Modulation (PAM) system*.
- Optimization of propagation delay, energy and area in an output pin driver.
- Design of a *triggering circuit for a buck converter*.
- Design of the *Control panel for a Microwave oven* operating in different modes and power levels.
- Study of an *Inverted pendulum* and stabilizing it in its vertical unstable equilibrium position.
- Study of *Proportional-Integrative-Differential (PID) Controller* on a process simulator and level control in a coupled tank.

SKILLS:

- Programming Languages : C, C++, Verilog HDL, HTML
- Software : CADENCE TOOLS, MATLAB/SIMULINK , AutoCAD
Protel DXP , LaTeX, Code Composer Studio, PSPICE
- Foreign languages : French (basic skills)
- Operating Systems : Windows, Ubuntu

ACADEMIC ACHIEVEMENTS:

- **State Rank - 3** in Andhra Pradesh in the Andhra Pradesh Regional Junior College Entrance Examination (APRJC) - 2002.
- **State Rank - 27** in Andhra Pradesh in the state level Polytechnic Entrance Examination - 2002.
- **Recipient of MCM Scholarship**, awarded by IIT Kharagpur. (2004 - 2008)
- **Recipient of Pratibha Scholarship** awarded by the Government of Andhra Pradesh for outstanding performance in academics – 2004.
- **Amongst the Top 100** selected from all over India in the Scholastic Aptitude Test (SAT) - 2002.
- **Among the Top 1%** in India in the All India Joint Entrance Examination (JEE) for admission into the Indian Institute of Technology.

PUBLICATIONS:

- Fazel A., Ravi S., Chakrabartty S., “*Analog to Feature Converter for Coarse-to-Fine Biometric Speaker Verification System*”, in preparation for IEEE Transaction of Circuits and Systems (TCAS)