

A Dynamic Reconfigurable A/D Converter for Sensor Applications

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Abstract— A hybrid algorithmic- $\Sigma\Delta$ ADC has been developed for sensor applications that benefit from dynamic reconfiguration of the tradeoff between resolution and conversion speed. By iteratively feeding back and resampling the residue of a $\Sigma\Delta$ conversion, bit weight information is embedded into the digital output sequence as in an algorithmic conversion. By varying the number of sampling and feedback cycles, the ADC can be dynamically reconfigured at the architectural level to be more $\Sigma\Delta$ -like, achieving higher resolution with lower speed, or more algorithmic-like, providing higher speed with lower resolution. With a nominal 10MHz clock, the ADC can resolve 8 bits in 1.6 μ sec, 16 bits in 51.2 μ sec or various configurations in between. Analysis of an example sensor application shows a 78% power savings due to dynamic reconfiguration to match signal characteristics.

I. INTRODUCTION

With the proliferation of miniaturized and autonomous sensors there has been an ever-increasing demand for reconfigurable analog-to-digital converter (ADC) architectures that can efficiently tradeoff speed and resolution with power consumption. For example, in some wireless ‘listening’ devices [1] (acoustic, vibration, etc.) where the incoming signal is inactive much of time, it is desirable to tune the ADC for low resolution and low power consumption, increasing resolution only when an active signal is detected. In multi-channel/element sensor systems [2], it is desirable to be able to roughly scan all channels quickly and then measure active channels with high resolution. Such adaptation to signal characteristics requires a reconfigurable tradeoff between conversion speed and resolution.

Previous research in reconfigurable ADC architectures has focused primarily on the pipelined architecture, where reconfigurable networks similar to those in Field Programmable Gate Arrays (FPGA) are used to scale pipeline stage depth or re-group the pipeline stages to optimize resolution and/or speed of the ADC [3][4]. However, pipelined architectures are tailored to high speed (1M-100MHz) applications, and their circuit complexity is not well suited to low-power sensor applications where data of interest rarely exceeds 100kHz. A low-power reconfigurable ADC that can reconfigure its architecture between pipelined and $\Sigma\Delta$ modes has been reported [5]. This ADC can achieve a wide range of bandwidth and resolution with adaptive power consumption. However, due to the intrinsic difference between the pipelined and $\Sigma\Delta$ architectures, the system requires very complicated circuits in order to realize the reconfigurability.

In low-power sensor applications, the most commonly used ADC architectures are: successive approximation register (SAR) [6], integrating [7], algorithmic [8], and sigma-delta ($\Sigma\Delta$) [9]-[11]. Algorithmic ADCs are typically applied to 100 kHz – 1 MHz signals requiring less than 12-bit resolution. Its architecture normally consists of a multiply-by-two, a sample-and-hold (SaH), a comparator, and a 1-bit DAC, as shown in Figure 1(a). On the other hand, $\Sigma\Delta$ ADCs can easily achieve a resolution higher than 16-bit using over-sampling and noise shaping techniques [9]-[11]. However, because of the large number of clocking cycles required for each conversion, $\Sigma\Delta$ architecture are generally only useful in low speed applications. A first-order $\Sigma\Delta$ architecture normally consists of an integrator, a comparator and a 1-bit DAC, as shown in Figure 1(b).

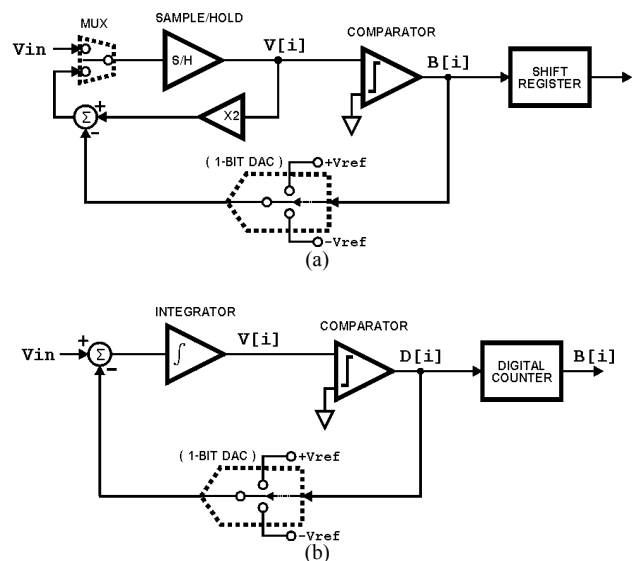


Figure 1. (a) Algorithmic ADC and (b) first-order $\Sigma\Delta$ ADC architecture.

This paper introduces a new ADC architecture that utilizes hardware similarities in algorithmic and $\Sigma\Delta$ topologies to efficiently reconfigure operation, at the architectural level, to tune conversion speed, resolution, and power consumption to signal characteristics. The novel hybrid algorithmic $\Sigma\Delta$ ADC will be described and results from behavioral analysis will be presented. Application of the hybrid algorithmic- $\Sigma\Delta$ ADC in sensor systems will be discussed.

II. HYBRID ALGORITHMIC $\Sigma\Delta$ ARCHITECTURE

A. Architecture

The extended conversion technique, wherein coarse conversion is added to measure the residue of a fine conversion, is widely used to improve resolution. In a broad sense, all two-step ADCs and subranging ADCs use the extended conversion technique. If the fine conversion is a first-order $\Sigma\Delta$ conversion, the error in the coarse conversion can be suppressed by the number of counting steps in the first $\Sigma\Delta$ conversion [12]. That is, the oversampling in the first phase improves the resolution of the second phase also.

Because subranging ADCs can be viewed as a cascade of multiple two-step architecture ADCs, it is intuitive to study the effect of applying multiple extended conversions on a first-order $\Sigma\Delta$ architecture ADC. As shown in Figure 2, a sample and hold (SaH) and an analog MUX can be added to the conventional first-order $\Sigma\Delta$ architecture to iteratively sample the integrator residue voltage V_{res} and feed it back to the $\Sigma\Delta$ input. Multiple extended conversions on a first-order $\Sigma\Delta$ can be achieved in this manner. Due to the mathematical nature of its operation and the hardware required, we have named the circuit in Figure 2 a *hybrid algorithmic- $\Sigma\Delta$ ADC*. This circuit allows the tradeoff between conversion speed and resolution (or power consumption) can be addressed by adjusting the number of loops in each of these two modes.

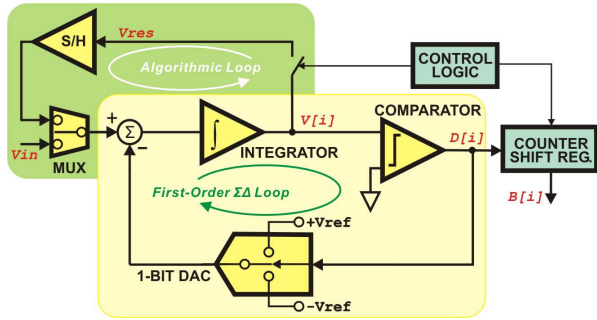


Figure 2. A multiple extended conversion $\Sigma\Delta$ ADC, the proposed architecture for a hybrid algorithmic- $\Sigma\Delta$ ADC.

B. Operation

In hybrid algorithmic- $\Sigma\Delta$ operation, the analog MUX is first switched to V_{in} , the input voltage, and a conventional first-order $\Sigma\Delta$ conversion is performed. Assuming it takes L cycles, then

$$V_i = V_{i-1} + (V_{in} - D_{i-1} \cdot V_{ref}) \quad \text{for } i = 1, \dots, L \quad (1)$$

where V_i is the integrator output voltage at each clock cycle i , D_i is the digital comparator output, and V_{ref} is the reference voltage. V_0 and D_0 are initialized to 0.

It has been proven [12] that

$$V_{in} = \frac{\sum_{i=1}^L D_i \cdot V_{ref} + V_{res1}}{L} \quad (2)$$

where the first term gives the ADCs estimated value of V_{in} , and the second term is the estimation error such that the residue after L cycles is $V_{res} = V_L - D_L V_{ref}$. In conventional extended conversion, the residue is measured by a coarse conversion circuit. However, the hybrid algorithmic- $\Sigma\Delta$ approach provides a feedback path to reuse the existing $\Sigma\Delta$ hardware to measure the residue. Furthermore, multiple feedback phases can be implemented to measure the residue of each phase. For M feedback phases,

$$V_{resj} = \frac{\sum_{i=jL+1}^{(j+1)L} D_i \cdot V_{ref} + V_{res(j+1)}}{L} \quad \text{for } j = 1, \dots, (M-1) \quad (3)$$

Reducing expressions (2) and (3) gives the final data reconstruction equation for the hybrid algorithmic- $\Sigma\Delta$ with M conversion phases of L first-order $\Sigma\Delta$ cycles:

$$V_{in} = \left(\frac{\sum_{i=1}^L D_i}{L} + \frac{\sum_{i=L+1}^{2L} D_i}{L^2} + \dots + \frac{\sum_{i=(M-1)L+1}^{ML} D_i}{L^M} \right) \cdot V_{ref} \quad (4)$$

$$V_{in} = \left(\sum_{j=1}^M L^{-j} \sum_{i=(j-1)L+1}^{jL} D_i \right) \cdot V_{ref}$$

C. Characteristics

Resolution: In the ideal case, each L cycles of a first-order $\Sigma\Delta$ conversion phase achieves $\log_2(L)$ bits of resolution. For M phases, the optimal resolution R is

$$R = M \cdot \log_2(L) \quad (5)$$

Speed (Conversion Time): First-order $\Sigma\Delta$ conversion requires L steps in each phase plus one additional step to reset the integrator and initialize the conversion. Thus, the total number clock cycles, N , required for M phases is:

$$N = 1 + M \cdot L \quad (6)$$

Hybrid Operation: From a component topology point of view, the core circuits are those of a first-order $\Sigma\Delta$ converter, and the additional front-end SaH and analog MUX show a striking similarity to the algorithmic converter shown in Figure 1a. Furthermore, the conversion result in (4) contains a summation of digital values, D , that is representative of first-order $\Sigma\Delta$ conversions and a binary weighted summation over M that is representative of an algorithmic ADC. Thus, the new hybrid algorithmic- $\Sigma\Delta$ converter essentially has two conversion loops: an inner first-order $\Sigma\Delta$ conversion loop and an outer algorithmic feed-back loop.

D. Behavioral Verification

Behavior of the hybrid algorithmic- $\Sigma\Delta$ converter has been simulated and verified in MATLAB. Figure 3(a) shows a case of $M=3$ phases and $L=16$ cycles each phase. The triangle wave is the integrator output, and the square wave is the comparator output. It can be seen that the first-order $\Sigma\Delta$ conversion is interrupted at the end of each phase and the residue is generated, sampled and fed back as input to the

next phase. Figure 3(b) shows the simulated input/output transfer function that verifies 12-bit resolution can be achieved when $L=16$ and $M=3$.

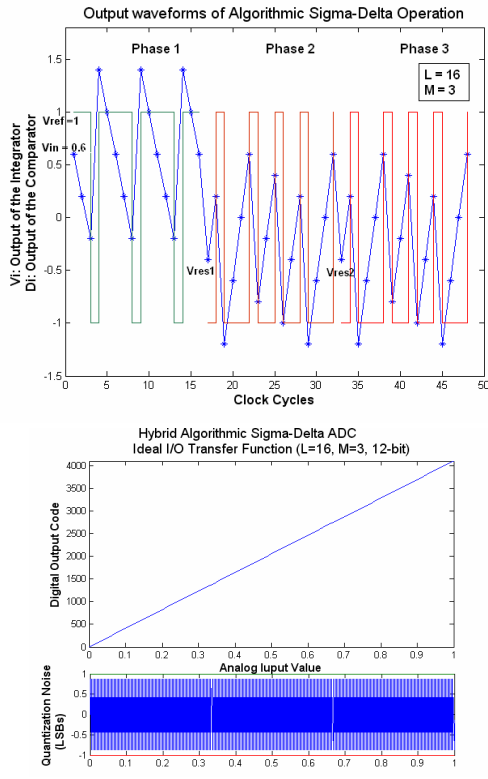


Figure 3. Behavioral verification of hybrid algorithmic- $\Sigma\Delta$ conversion. (a) output waveforms. (b) Transfer function and quantization noise.

III. BEHAVIORAL ANALYSIS

A. Architecture Level Reconfigurability

The hybrid algorithmic- $\Sigma\Delta$ implements L first-order $\Sigma\Delta$ counting steps in each of M algorithmic feedback phases. If L is large and M is small (longer counting conversion and fewer residue feedbacks), the system behaves more $\Sigma\Delta$ -like, with high resolution but slow speed; the number of required clock cycles increases logarithmically with respect to resolution. If L is small and M is large (less counting but frequent residue feedback), the system behaviors more algorithmic-like, with relatively low resolution but high speed; the total number of clocks increases linearly with respect to resolution. Because speed and resolution vary with M and L , the system can be dynamically reconfigured at the architectural level by adjusting M and L , which can be fully determined by the clocking scheme. This allows the system to be easily tailored to application demands in real time.

B. Resolution, Speed and Power Tradeoffs

The relationship between resolution and conversion time and the circuit parameters L and M , shown in (5) and (6), is

not as straightforward as other ADC topologies. As a result, the architectural reconfigurability of the hybrid algorithmic- $\Sigma\Delta$ ADC offers a unique capability to adjust circuit performance and address the speed/resolution/power tradeoff. Figure 4 shows some of the wide range of configurations possible, mapping values of L and M to achievable resolutions and require clock cycles.

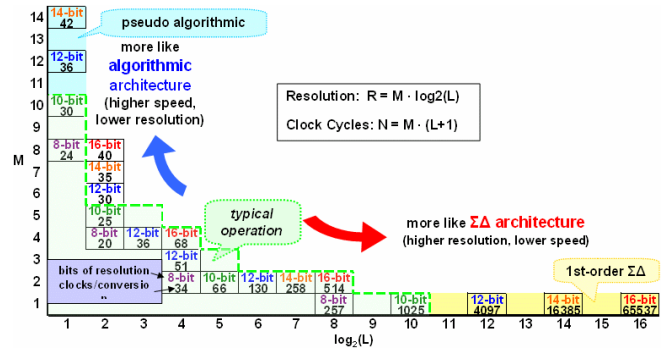


Figure 4. Speed and resolution combinations by varying M and L .

To better visualize the configurability of the hybrid algorithmic- $\Sigma\Delta$ architecture, consider Figure 5, which shows how the resolution and power consumption can vary as the conversion speed is increased. To maintain low power consumption, the circuit would retain a $\Sigma\Delta$ -like configuration, and increasing speed would require reducing resolution (solid lines). Alternatively, the resolution could be reduced less dramatically by introducing some algorithmic-like phases at the cost of increased power consumption (dashed lines). To retain high resolution with increased speed, more feedback phases must be enabled, significantly increasing power consumption (dotted lines). The diverse combinations of performance achievable with the hybrid algorithmic- $\Sigma\Delta$ ADC provide tremendous value to systems with varying signal characteristics.

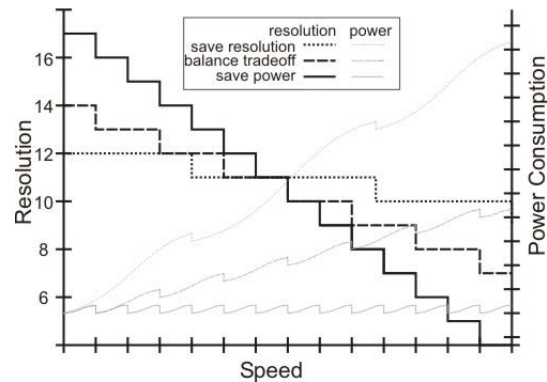


Figure 5. Operational space of the hybrid algorithmic- $\Sigma\Delta$ ADC.

IV. DYNAMIC RECONFIGURATION IN SENSOR APPLICATIONS

The hybrid algorithmic- $\Sigma\Delta$ architecture's capability for real-time reconfigurability is especially well suited for sensor systems where variability of signal characteristics over time

or space provides an opportunity to improve system performance. The examples below demonstrate the benefit of the hybrid algorithmic- $\Sigma\Delta$ ADC in two potential applications.

Figure 6 represents a multi-channel sensor application where it is desirable to monitor all channels while minimizing power consumption. Here, the hybrid algorithmic- $\Sigma\Delta$ ADC can be configured to scan all signals with low resolution to locate inactive channels. The ADC could then measure with high resolution only the active channels, optimizing conversion speed to minimize power.

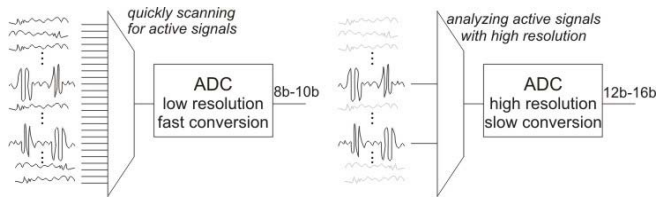


Figure 6. An example multi-channel sensor application.

Figure 7 shows a typical output from a gas vapor sensor, which exhibits periods of high signal activity and periods of relatively minimal activity. To accurately measure the peaks, a high resolution ADC is needed. However, a high resolution ADC would consume unnecessary power when the signal is not quickly changing. Dynamic reconfiguration of ADC resolution could optimize performance.

The data in Figure 7, recorded by a real sensor, was analyzed using two methods. First, a 16-bit $\Sigma\Delta$ ADC configuration was applied. The ADC output very closely tracks sensor data with constant power consumption. Second, the hybrid algorithmic- $\Sigma\Delta$ was applied using a simple algorithm that dynamically adjusts the configuration during operation. The resolution and power consumption were reduced, by increasing M and decreasing L when the output was below a certain threshold. When the signal was above the threshold, the ADC was reconfigured to maximize resolution, effectively operating the same as the first case 16-bit $\Sigma\Delta$ ADC. As shown in Figure 7, the dynamically reconfigured hybrid algorithmic- $\Sigma\Delta$ tracked the input almost as well as the 16-bit $\Sigma\Delta$ ADC, but the power was significantly reduced during the periods the signal was below the threshold. Overall, dynamic reconfiguration provided a 78% power savings.

V. CONCLUSION

A reconfigurable ADC architecture that can dynamically adjust speed, resolution, and power consumption to match data characteristics was presented. The new hybrid algorithmic- $\Sigma\Delta$ ADC combines features of the first-order $\Sigma\Delta$ ADC and the algorithmic ADC topologies to achieve flexibility of operation well suited to many sensor applications.

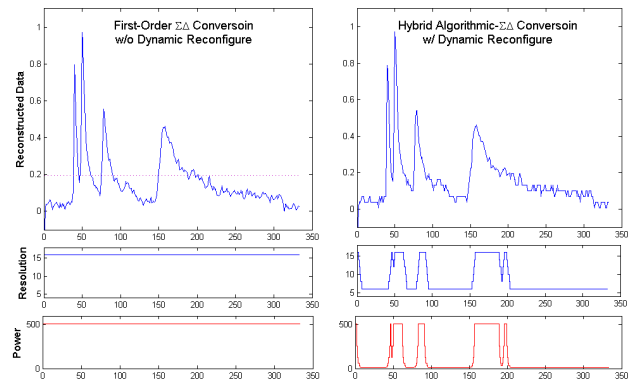


Figure 7. Hybrid algorithmic- $\Sigma\Delta$ ADC operating on sensor data under two configurations. (left) First-order $\Sigma\Delta$ conversion with 16-bit resolution. (right) Dynamic reconfiguration of resolution/power. The top plots show the ADC outputs, which both closely follow the input. The middle and bottom plots show the resolution and normalized power consumption, respectively, as a function of time.

REFERENCES

- [1] K.D. Wise, K. Najafi, R.D. Sacks, and E.T. Zellers, "A wireless integrated microsystem for environmental monitoring," in Digest of Technical Papers, ISSCC, 2004, pp. 434-537.
- [2] K. D. Wise, D. J. Anderson, J. F. Hetke, D. R. Kipke, and K. Najafi, "Wireless Implantable MicroSystems: High-density Electronic Interfaces to the Nervous System," Proc. IEEE, vol. 92, pp. 76-97, Jan. 2004.
- [3] Mortezaapour, and E.K.F. Lee, "A reconfigurable pipelined data converter," Proc. IEEE ISCAS 2001, vol. 4, pp. 314 - 317, May. 2001.
- [4] Hui Liu, and M. Hassoun, "A 9-b 40-MSample/s reconfigurable pipeline analog-to-digital converter," IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 49, pp. 449 - 456, July 2002
- [5] K. Gulati and H.-S. Lee, "A low-power reconfigurable analog-to-digital converter," in Proc. ISSCC, 2001, pp. 54-55.
- [6] M.D. Scott, B.E. Boser, and K.S.J. Pister, "An ultralow-energy ADC for Smart Dust," IEEE J. Solid-State Circuits, vol. 38, pp. 1123 - 1129, Jul. 2003.
- [7] M. Schienle, C. Paulus, A. Frey, F. Hofmann, B. Holzapfl, P. Schindler-Bauer, and R. Thewes, "A fully electronic DNA sensor with 128 positions and in-pixel A/D conversion," IEEE J. Solid-State Circuits, vol. 39, pp. 2438 - 2445, Dec. 2004.
- [8] P.W. Li, M.J. Chin, P.R. Gray, and R. Castello, "A ratio-independent algorithmic analog-to-digital conversion technique," IEEE J. Solid-State Circuits, vol. 19, pp. 828 - 836, Dec. 1984.
- [9] S. Rabbii and B. Wooley, "A 1.8V digital-audio sigma-delta modulator in 0.8 μ m CMOS," IEEE J. Solid-State Circuits, vol. SC-32, no. 6, pp. 783-796, Jun. 1997.
- [10] E. Fogleman *et al.*, "A 3.3-V single-poly CMOS audio ADC delta-sigma modulator with 98-dB peak SINAD and 105-dB Peak SFDR," IEEE J. Solid-State Circuits, vol. SC-35, no. 3, pp. 297-307, Mar. 2000.
- [11] L. Breems, E. van der Zwan, and J. Huijsing, "A 1.8mW CMOS $\Sigma\Delta$ modulator with integrated mixer for A/D conversion of IF signals," IEEE J. Solid-State Circuits, vol. SC-35, no. 4, pp. 468-475, Apr. 2000.
- [12] P. Rombouts, W. DeWilde, and L. Weyten, "A 13.5-b 1.2-V micropower extended counting A/D converter," IEEE J. Solid-State Circuits, vol. 36, pp. 176-183, Feb. 2001.