Compact Impedance Spectroscopy for High Density Sensor Arrays

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Abstract: Impedance Spectroscopy (IS) is a powerful technique for characterizing materials and interrogating many sensors, particularly within evolving nanotechnologies. The instrumentation to support emerging sensor applications has, however, lagged far behind the materials and sensor development. This paper presents a mixed-signal integrated circuit suitable for chip-scale implementation of IS instrumentation to support high density sensor arrays within a microsystem platform. An IS cell was implemented and fabricated in a 0.5\(\mu\)m CMOS process and occupies 205\(\mu\)m x 108\(\mu\)m. Test results show that the IS system operates correctly, but is limited by noise in the integrator. An alternative integrator is also proposed to address this.

Keywords: Impedance Spectroscopy, Sensor Array, Frequency Response Analyzer, Lock-in Amplifier

I. Introduction

Impedance Spectroscopy (IS) has established itself as a critical technique for sensor instrumentation, especially in the field of micro and nano-scale sensing. Examples of current applications of IS include particle detection for on-chip fluidics [1], blood cell sorting [2][3], DNA sensors [4], and protein-based sensors [5]. IS can be used as an option to greatly extend the information obtained from Chemiresistors (CR) for vapor detection.

An IS system measures a sensor's impedance (complex resistance) across a range of frequencies. This allows a great deal of information about materials and material interfaces to be extracted. For instances, some chemiresistors (CR) exhibit both a resistive and capacitive response to vapors, and IS allows both components of the CR response to be determined with a single measurement. Other sensors absolutely require IS analysis, because their impedance model is too complex for either independent resistive or capacitive measurement. For instance, biosensors based on tethered Lipid Bilayers (tBLM) exhibit a model with at least two capacitances and a resistive component [6], and the resistive response, which is the key sensor value, dominates only within a small range of frequencies that shifts with material properties. Using IS, the desired resistance value within the complex impedance model can be readily identified and measured.

To reach their full potential, many of the sensors that require IS would be placed in high density arrays. For example, DNA sensors require hundreds of known DNA strands in an array, and monitoring of some vapors requires several CRs with different functionalized coatings to fully analyze the vapor. For these systems, hundreds of IS measurement may need to be performed simultaneously. The amount of raw data generated by these high density arrays requires that the response be computed/compresses before it is sent off chip [7]. Also, some of these sensors have sensitivities below what can be measured using conventional off-chip instrumentation due to coupled noise in the leads. By placing the sensor and instrumentation on the same silicon, much of that noise can be eliminated. Finally, full chip integration will enable low-power, low-cost, and even portable applications to be developed for these sensors.

Despite the emerging demand for these sensors, the lack of on-chip instrumentation to supports their specific needs is hampering further application of these sensors. Nearly all development of IS-based sensors still makes use of expensive and bulky bench top IS systems or PCB based solutions [8]. This paper describes the design of an IS system tailored specifically to meet the needs of a high density sensor array with fully on-chip instrumentation. Section II presents possible solutions for IS instrumentation and the system level implementation selected. Section III presents the circuit design of the system. Test results are given in Section IV, and the conclusion is given in Section V.

II. System Level Implementation

The most popular method for performing IS is to stimulate the sensor with a broadband pulse and then digitize and process the response using the Fast Fourier
Transform (FFT), which converts the broadband response to a frequency domain response. This solution is simple to implement on a computer. However, the hardware and bandwidth requirements are much too intensive for use with sensor arrays on a single chip.

Another popular IS method, known as the Frequency Response Analyzer (FRA), can be realized by a lock-in amplifier that computes the real and imaginary portions of a sensor response at each frequency point. This method can be implemented fully in the analog domain allowing for a very compact on-chip system.

To serve the needs of high density sensor arrays, the IS electronics must be compact enough to be instantiated many times on a single chip. Thus size is the primary constraint, and the FRA method has been chosen for this design due to its smaller size. A more detailed discussion of the possible IS implementations and their relative merits can be found in [7].

The basic system architecture of the FRA system is shown in Figure 1. Here, the sensor is stimulated with a sine wave. The output of the sensor is then multiplied by the original sine wave and a cosine wave. The results of these multiplications are:

\[
\begin{align*}
  &A \sin(\omega t + \phi) + C \times B \sin(\omega t) = \\
  &\frac{AB}{2} \{\cos(\phi) + \cos(2 \omega t + \phi)\} + BC \sin(\omega t) \\
  &A \sin(\omega t + \phi) + C \times B \cos(\omega t) = \\
  &\frac{AB}{2} \{\sin(\phi) + \sin(2 \omega t + \phi)\} + BC \cos(\omega t)
\end{align*}
\]

where \(A\) and \(C\) are the amplitude and dc offset of the sensor response, respectively, and \(B\) is the amplitude of the stimulus signal. It can be seen that the dc portions of the multiplier outputs are proportional to the real and imaginary response of the sensor. The integrator isolates this dc component. Thus, the final outputs of the system are the real and imaginary responses of the sensor at the frequency of the input signals.

### III. Circuit Design

The FRA cell requires three major components: multipliers, integrators and a current mirror. The current mirror is used to copy the sensor output to each multiplier. The full system also requires a dual phase sine wave generator that will not be covered in this paper.

Analog multipliers are generally designed to have high linearity, in order to suppress harmonics in the output. However, in this IS system, all frequency components of the multiplier output above dc will be removed by the integrator, and thus a high linearity multiplier is not needed. In trading off linearity for reduced size, the multiplier, shown in Figure 2, can be implemented with a very simple differential pair that is biased in the sub-threshold region.

When biased in the sub-threshold region, a transistor's \(g_m\) is proportional to its drain current, and multiplication is naturally achieved, because the small signal current is the product \(V_{gs}\) and \(g_m\). The output of the multiplier in Figure 2 is given by

\[
I_{out} = I_{tail} \tanh \left( -\kappa \left( V_{in+} - V_{in-} \right) \right)
\]

where \(I_{tail}\) is \(I_{in}\) plus the bias current from M1. When the argument of the hyperbolic tangent is small, the function is approximately equal to its argument, thus

\[
I_{out} \approx I_{tail} \times \left( V_{in+} - V_{in-} \right) \left( -\kappa \right) \left( \frac{1}{2U_T} \right)
\]

In this design, the linearity requirements of the multiplier have been shifted to the integrator, which must also maintain small size. Not only does the integrator need to be accurate and small, it also needs to be able to operate over a wide range of output values. Each signal must be integrated over multiple cycles of the input signal, thus for low frequencies or large real/imaginary responses, the integrated value can grow rapidly. Two different integrator topologies that meet these requirements are the switched current integrator and the logarithmic integrator.
The switched current integrator, shown in Figure 3, uses two current-mode sample-and-hold (S/H) circuits to store and sum the inputs. The advantage of this system is that the stored current can range over at least three decades, thus providing a very wide integration range. The drawback of this approach is that charge injection error from the S/H switches can be significant. To reduce the charge injection, a high accuracy S/H with charge injection compensation \[9\] was selected. This reduces charge injection error but does not eliminate it. The switched current integrator was used to construct an IS system, where the total cell (2 integrators, 2 multipliers, a mirror, and signal routing) size was 205 \(\mu\)m \(\times\) 108 \(\mu\)m. Test results from the fabricated system showed that the multiplier worked well, but noise in the switched current integrator was unacceptably high.

Alternatively, the logarithmic integrator \[10\], shown in Figure 4, attempts to increase integrating range by compressing values logarithmically at the input. Transistors M1 and M2 perform the logarithmic compression, and M9 performs the exponential expansion. In addition to increasing the range of operation, this approach has the added advantage of reducing power consumption, which is particularly important in high density array applications.

The logarithmic conversion, however, also provides a source of significant error. Because the output voltage will be exponentiated, small internal errors will be greatly amplified. However, the differential structure of the integrator eliminates common mode noise, including contributions from M7 and M8. The only error sources then become noise contributions from M3-M6 and size mismatch due to fabrication variation. The extent of this noise contribution is not yet known, however a test chip is currently being fabricated to determine this.
The actual range over which the logarithmic integrator can integrate is determined by the size of the capacitor, because $V_{\text{out}}$ must remain below the nMOS threshold voltage. Due to size constraints, only a small capacitor can be used, thus the integration range is not very large. The range, however, can be extended nearly indefinitely by converting the system to an oscillator. By adding a current mode comparator at the output which feeds back to the integrator reset, the integrated value can be encoded as the frequency of the reset signal. This also provides the advantage of producing a digital output, thus analog to digital conversion is added with only the additional expense of a counter and current mode comparator.

While this configuration is very similar to a simple relaxation oscillator [11] it is much more compact. The capacitor is the dominant component in both systems, but the log domain capacitor is much smaller. A relaxation oscillator designed to operate at 100kHz, with a maximum input of 300nA requires a capacitor of about 1pF (assuming the capacitor may charge across a 3V range). A logarithmic oscillator designed to operate under the same conditions would require a capacitance of only 100fF, thus reducing the size of the largest component by a factor of 10. Also, the op-amp and comparator of the relaxation oscillator are replaced with the smaller logarithmic integrator and current mode comparators. As an added advantage, because the logarithmic integrator is operating entirely in the sub-threshold domain, its power consumption should be significantly less than that of a standard relaxation oscillator. Using the logarithmic oscillator then provides a trade-off between the extremely compact switched current integrator, with high noise and the very large, low noise relaxation oscillator.

The final key component for the FRA cell is a current mirror, which copies the sensor response to both multipliers. There are three key requirements for this mirror. First, it must make identical copies of the current, so that both multipliers receive the same value. Second, it must be able to mirror a purely ac input current, because many sensors have a series capacitance, which acts as a dc block. Third, it must have a very low input impedance so as not to load the sensor and change its response. The first is easily addressed with a cascoded mirror. The second requirement can be solved by injecting a dc current sufficient to insure that total input current is positive. These two solutions are shown in Figure 5.

The third requirement, preventing loading of the sensor, demands more careful consideration. A simple diode connected input, such as is shown in Figure 5, has an input impedance of $1/g_m$. For small currents and transistors, this is too large for many sensors. To decreases the input impedance, a Flipped Voltage Follower Current Sensor (FVFCS) [12], as shown in Figure 6, can be used. This mirror has an input impedance of

$$r_i = \frac{1}{g_m g_{m2} r_{o1}} \quad (5)$$

Thus the input impedance can be reduced without adding significantly to the area or complexity of the mirror. This also means that the frequency response of the mirror will be much less affected than it would have been with a more complex solution. A final advantage of this system is that the voltage at the input node is now set by $V_{ds}$ instead of $V_{gs}$, which puts the voltage closer to the ground rail. This can be significant in low voltage systems that are trying to achieve a large voltage swing across the sensor.
IV. Test Results

The multiplier and switched current integrator were fabricated in a standard 0.5μm CMOS process. A single IS cell (2 multipliers, 2 integrators, 1 mirror, and routing) occupies 205μm x 108μm. The key test results are presented here, however, complete results are given in [13].

A parallel RC load, as shown in Figure 7, was used to emulate a sensor element. In this model, $R_s$ and $C_s$ are the actual sensor components and $R_p$ is the parasitic resistance of the system. $R_s$ was set to 1MΩ and $C_s$ to 220pF and 100pF. $R_p$ was estimated to be approximately 100mΩ. The ideal response of this emulated sensor is shown in Figure 8.

The multiplier was tested by connecting the RC loads to the multiplier input and digitally integrating the multiplier output. The results of this IS measurement are shown in Figure 9. Comparison to Figure 8 shows that the multiplier produced an accurate response.

The switched current integrator was then connected to the multiplier output. The resulting IS measurements are shown in Figure 10. It is clear that the noise introduced by charge injection in the integrator is excessive, although the response still shows approximately correct slopes for each measurement.

The log domain integrator has not yet been fabricated, but simulation results are shown in Figure 11. The output, encoded as time, can be treated as linear if the dc input is limited to a reasonable range.
V. Conclusion

This paper presented the necessary components for an extremely compact Impedance Spectroscopy system capable of supporting sensor arrays with a fully on-chip solution. These components are a first step towards a compact low-cost, low-noise instrumentation system that will enable many powerful applications for the new IS based sensors being developed.


