A Mixed-Voltage Sensor Readout Circuit With On-Chip Calibration and Built-In Self-Test

Andrew Mason, *Senior Member, IEEE*, Abhijeet V. Chavan, and Kensall D. Wise, *Life Fellow, IEEE*

***Abstract*—This paper reports a mixed-voltage mixed-signal chip for interfacing multiple capacitive transducers to embedded processors in integrated microsystems. A programmable switched-capacitor readout circuit accommodates capacitive sensors from 16 fF to 40 pF and allows self-test and online calibration. The 20 mm^2 chip has a sensitivity of 1.25 mV/fF and is realized in a 1 μm n-well BiCMOS 2 P/2 M process that permits high-voltage operation, large-value resistors, and nonvolatile on-chip memory. An on-chip charge pump generates voltages up to 30 V that permits transducer electrostatic self-test. In normal operation mode, the chip provides a fast sensor readout consuming only 90 nJ of energy, making it suitable for portable applications.**

***Index Terms*—Capacitive sensor, electrostatic force feedback, sensor interface, sensor self-test, switched-capacitor (SC).**

I. Introduction

THE PROLIFERATION of real-time sensing applications has driven the need for cost-effective, highly accurate interface circuits. This is especially true in portable microsystems [1], [2], where capacitive transducers are preferred for their low power and electrostatic self-test capabilities. The readout circuits for capacitive sensors that have been reported can be broadly classified as analog [3]–[15], sigma-delta [16], [17], and digital/oscillator-based [18]–[22]. These circuits offer a range of performance and are either tailored to specific sensors or have built-in flexibility for use with several sensors. However, as the applications of sensors expand, there is a growing need to address sensor reliability and testability. Because testing is a significant factor ($>25\%$) of sensor cost, an important aspect of next-generation sensor interface circuits is their ability to minimize the expense associated with offset and gain adjustments and other calibration and temperature compensation (CTC) operations. Careful partitioning is necessary to determine the most suitable architecture for efficient CTC, and analog [22], [23], digital [24], or hybrid methods can be used. In the hybrid case, calibration, namely setting the dc offset and range (gain), is done on-chip using nonvolatile memory, while digital compensation of temperature sensitivities is performed in an off-chip microsystem controller using polynomials evaluation. In a production environment, two-temperature CTC is adequate due to the linear nature of the temperature drift.

This paper reports a chip specifically designed to support the readout, calibration, and self-test of multiple capacitive sensors within a single microsystem. The architecture of the chip is based on an analog interface for sensor output data but also employs a serial bus interface for addressing multiple sensors and for programming specific elements on the interface chip that implement CTC functions. The chip achieves high resolution and low-noise capacitive readout in a highly programmable platform that can apply fixed offset and gain settings from on-chip EPROM or, alternatively, allows online modification of readout parameters. Furthermore, the chip permits a variety of self-test methods, including the ability to electrostatically actuate external transducers with up to 30 V dc. The unique combination of features supported by this chip allows the development of low cost, highly-autonomous microsystem for applications that demand information from multiple capacitive sensors, including environmental awareness and personal/asset security monitoring.

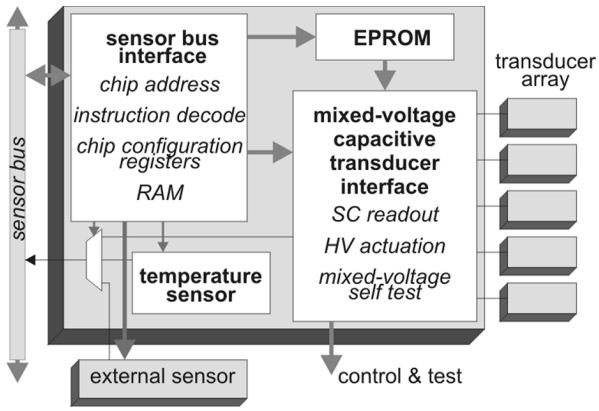

Fig. 1. Functional block diagram of the mixed-voltage capacitive sensor interface chip.

II. Chip Architecture

Fig. 1 highlights the primary functional blocks of the chip, comprising a sensor bus interface, an EPROM, a CMOS temperature sensor, and a unique, multifunctional, mixed-voltage capacitive transducer interface circuit. The overall chip architecture assumes implementation within an

Manuscript received September 7, 2006; revised February 1, 2007; accepted February 19, 2007. This work was supported in part by the Microsystems Technology Office of the Defense Advanced Research Projects Agency (DARPA) under Contract DABT63-95-C-0111. The use of facilities now supported by the Engineering Research Centers Program of the National Science Foundation under Award Number EEC-9986866 is gratefully acknowledged. The associate editor coordinating the review of this paper and approving it for publication was Dr. Patrick Ruther.

A. Mason is with the Department of Electrical and Computer Engineering, Michigan State University, East Lansing, MI 48824 USA (e-mail: mason@msu.edu).

A. V. Chavan is with Guidant Corporation, St. Paul, MN 55112-5798 USA (e-mail: abhi.chavan@guidant.com).

K. D. Wise is with the Center for Wireless Integrated MicroSystems, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109 USA (e-mail: wise@umich.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSEN.2007.897957

integrated microsystem, where precision digital calibration and data compensation can be performed by an embedded microcontroller. The transducer interface block includes a three-stage switched-capacitor (SC) transducer readout chain with a fully differential charge-integrator front end, two sets of programmable capacitor arrays for electronic trimming, a voltage controlled oscillator (VCO)-based charge pump and a digital-to-analog converter (DAC) used for mixed-voltage self-test, and a high-voltage-compatible multiplexer for multiple transducer inputs. The entire circuit is highly programmable, accepting configuration data either through the bus interface or via on-chip EPROM. The on-chip temperature sensor measures the ambient environment and permits digital compensation of secondary transducers sensitivities within the microsystem. An on-chip mid-rail voltage reference provides the analog ground reference.

The sensor bus interface block connects this chip to a nine-line sensor bus capable of linking several front-end sensor nodes to an embedded microcontroller with minimal hardware within each node [1]. Serial input data (4b chip address, 8b instruction, and 16b data word) received by the interface chip selects a sensor element to be read or writes to on-chip static RAM. During a read instruction, the chip data output is generated by either the on-chip temperature sensor, one of five capacitive transducers multiplexed into the SC readout circuitry, or an external sensor containing its own readout circuitry. During a write instruction from the bus, data is stored in on-chip RAM for precision control of external actuators or circuit blocks on the chip including the DAC, high-voltage generator, SC readout circuit, and temperature sensor. In addition, the on-chip self-contained 65-bit EPROM [25] can be used to store predetermined transducer calibration coefficients to set the gain and offset of the SC circuit. Five 8b offset and three 10b gain settings can be stored on chip; more precise calibration/compensation can be done digitally in the processor. The bus interface block also includes a pass-through to external sensors, consisting of a data line, a 3b address, and read/write enable signals. This allows the microsystem to access, through this interface chip and the sensor bus, a wide variety of sensors that otherwise would not be bus compatible.

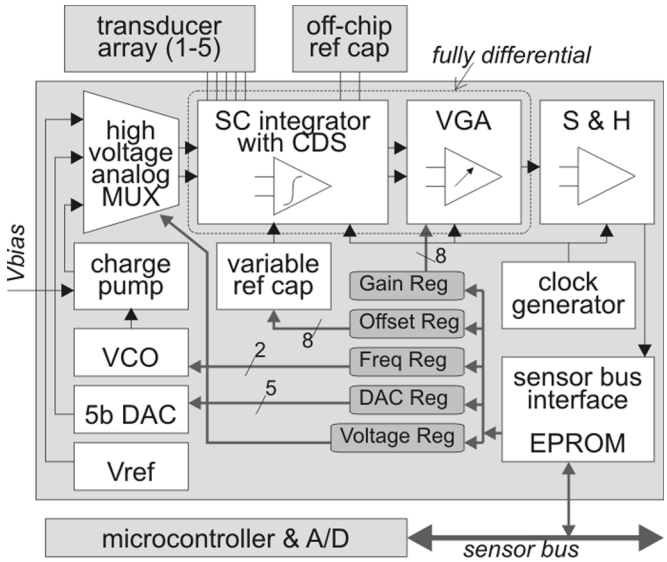

Fig. 2. Functional schematic for the highly configurable, mixed-signal, mixed-voltage, switched capacitor sensor readout circuit with self-test and calibration capabilities.

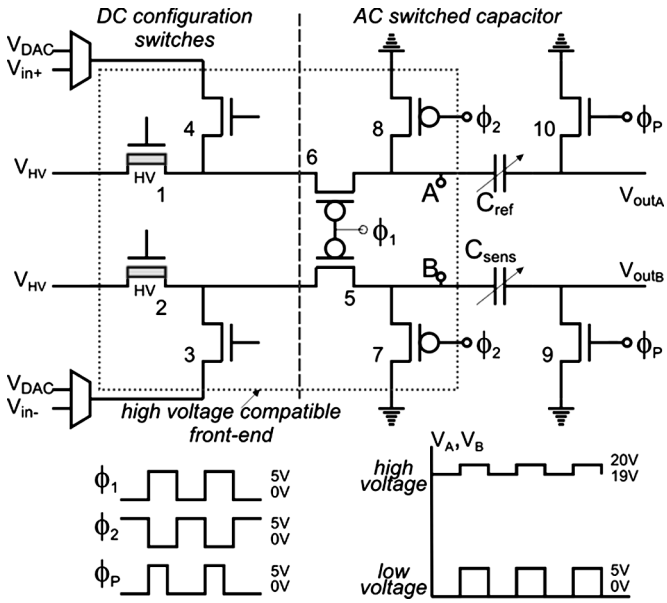

Fig. 3. Mixed voltage switching front end for the switched capacitor sensor readout circuit.

III. High-Voltage Front End

The use of electrostatic forces for actuating different structures in micromechanical systems is well established but has been limited to relatively low voltages in sensors containing monolithic readout circuitry due to the difficulty of integrating high-voltage circuits on a chip. The readout chain discussed here has the ability to use higher voltages for sampling the transducer capacitance. This high-voltage capability is provided for use in self-test and for optional operation in a closed-loop force-feedback configuration. Fig. 2 illustrates the circuits that control and implement the analog data path on the chip.

During low-voltage (5 V) operation, the SC integrator input voltage is selected from the on-chip voltage reference generator or the output of the 6b DAC. Alternatively, during high-voltage operation, an on-chip charge pump provides up to 30 V. It is thus necessary to provide proper isolation between the low-voltage circuitry and high-voltage section of the front end. This isolation is achieved by a switching path composed of high-voltage CMOS transistors fabricated with thicker gate oxides and more lightly doped sources and drains. The gate switching voltages and output voltage transitions under low- and high-voltage conditions are shown in Fig. 3. Transistors 1–4 have dc gate signals to program the configuration of the high-voltage analog multiplexer. Transistors 5–8 are involved in clocked switching of the SC circuit input. The clock voltages on these pMOS gates are limited to 5 V to minimize charge injection effects. When the input is selected to be from a low voltage source (V_{in+}, V_{in-} or V_{DAC}), the input will be at most 5 V and switches 5, 6 can turn completely off when the gate signal, ϕ_1, reaches 5 V. However, when V_{HV} is selected as the input, pMOS transistors 5, 6 will continue to source current when their gate voltage, Vg,

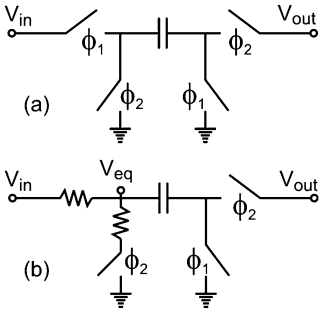

Fig. 4. Switched-capacitor front-end switching model for (a) low-voltage and (b) high-voltage operation.

reaches 5 V because $\mathrm{V_{HV}} > \mathrm{Vg} + |\mathrm{Vt}|$. In this case, nodes A and B will only be partially discharged because devices 5, 7, and 6, 8 are all on and form carefully ratioed voltage dividers, with $(\mathrm{W/L})_{5,6} \approx 20(\mathrm{W/L})_{7,8}$. For example, if the HV input is 20 V during the sampling phase, then nodes A and B will drop to 19 V during the integration phase for an average dc bias of 19.5 V.

The SC switching circuit can be represented as shown in Fig. 4(a) for low-voltage operation, and as shown in Fig. 4(b) for high-voltage operation. The average current in these two cases is given as

$$I_{\mathrm{avg}} = \frac{C_s(V_{\mathrm{in}} - V_{\mathrm{out}})}{T} \tag{1}$$

$$I_{\mathrm{ave(hv)}} = \frac{C_s(V_{\mathrm{in}} - (V_{\mathrm{out}} - V_{\mathrm{eq}}))}{T} \tag{2}$$

where V_{eq} is the resultant voltage due to the partial discharge of capacitor C_s, and C_s is either C_{ref} or C_{sens} from Fig. 3. For a sensor capacitance of 10 pf, a clock frequency of 100 kHz and V_{in} of 2.5 V, (1) gives $I_{\mathrm{avg}} = 5\ \mu$A. Alternatively, if V_{in} is set to 20 V, (2) evaluates to $I_{\mathrm{avg(hv)}} = 1\ \mu$A.

The resistor equivalent of the SC is the same in both cases except that a smaller amount of charge is integrated in each clock period during high-voltage operation. The resulting dc bias can be used, for example, to apply a force F on the moving plate of a capacitive transducer as described by

$$F = -\frac{\varepsilon_o A V^2}{2g^2} \tag{3}$$

where A is the area, V is the dc bias, and g is the gap across the capacitor plates. At an applied bias of 30 V and an initial gap of 1 μm, about 310 mN of force is generated across a 1 mm-diameter sensor. This applied force can be used for electrostatic self-test or for modifying the operating range of the transducer.

IV. Switched-Capacitor Readout

A. Performance Considerations

The chip contains a three-stage SC readout circuit that can multiplex up to five sensor elements at its input. As shown in Fig. 5, this circuit features programmable capacitor arrays capable of calibrating gain and offset over a wide range of base capacitances (16 fF–40 pf) and sensitivities (20.8 μV/fF–1.25 mV/fF). The first stage includes a fully differential charge integrator based on a self-biased folded-cascode amplifier that uses continuous-time current-summing common-mode feedback (CMFB) for dc stabilization, reduced charge injection effects, and improved bias stability and common mode rejection [26]. With dc input sampling, the output of the first-stage charge integrator is given by

$$\Delta V_o = \left(\frac{C_s}{C_f} V_{\mathrm{in+}} - \frac{C_R}{C_f} V_{\mathrm{in-}}\right) \tag{4}$$

where the parameters are defined in Fig. 5. ΔV_o is limited to 2.5 ± 0.5 V.

The clocking scheme uses correlated double sampling (CDS) to suppress flicker noise and amplifier offset effects. Due to CDS, the power spectral density of the noise is multiplied by

$$\left|H_{\mathrm{CDS}}(e^{j\omega t})\right|^2 = 4\sin^2\left(\frac{\omega T}{4}\right) \tag{5}$$

where ω is the input signal frequency and $T = 1/f_{\mathrm{clk}}$ is the clock period. Thus, CDS eliminates the dc offset and also suppresses noise at dc and around $2f_{\mathrm{clk}}, 4f_{\mathrm{clk}}$, etc. The effects of minimum-sized nMOS switch channel charge injection and clock feed through are cancelled to first order by the fully differential scheme [27]. The other major sources of noise are the $\mathrm{kT/C_T}$ noise and amplifier thermal noise, where $\mathrm{C_T}$ is the equivalent capacitance at the amplifier input node. The $\mathrm{kT/C_T}$ noise is minimized due to the large capacitance used for integration and gain. Thermal noise cannot be eliminated and needs to be quantitatively evaluated and minimized. This noise can be estimated by multiplying the amplifier thermal noise by the gain and integrating over the entire bandwidth. The output of the first stage feeds a differential gain stage with single-ended output conversion. Considering the integration and gain stages together, the thermal noise is approximated as [28]

$$\frac{\overline{\nu_{\mathrm{tot}}^2}}{\Delta f} = \frac{2}{f_{\mathrm{clk}}}\left[\left(\overline{\nu_{\mathrm{int}}^2} + \overline{\nu_{\mathrm{gain}}^2}\right) A_g^2 \left(\mathrm{BW}\frac{\pi}{2}\right)\right] \tag{6}$$

where ν_{int} is the input referred rms noise of integrator stage, ν_{gain} is the input referred rms noise of gain stage, A_g is the gain in the gain stage, and BW is the unity gain bandwidth. This is numerically estimated to be 594 nV/$\sqrt{\mathrm{Hz}}$, which is well below the required resolution.

B. Calibration and Self-Test

The chip has several features for online self-test and drift correction. Time-dependent drift in the circuitry itself can be measured, independent of the input transducer, using an array of on-chip reference capacitors. For self-testing movable-electrode transducers, a charge pump generates a high-voltage ($\leq$ 30 V) dc bias for electrostatic actuation. The programmable output of the charge pump can be used to set several test points, allowing any transducer gain drift to be measured. The other selectable input to the front end (Fig. 2) comes from a 6b DAC. This DAC is a binary-weighted current-mode converter [29] that uses a folded cascode OTA at the output to obtain an analog voltage level. The DAC voltage reference is scalable between 3.5 and 5 V, which in turn scales the least significant bit (LSB) and allows the minimum voltage step to be programmed between 55 and 78 mV. If a field self-test detects minor drift in the circuit or the transducer, software selection of a different DAC input

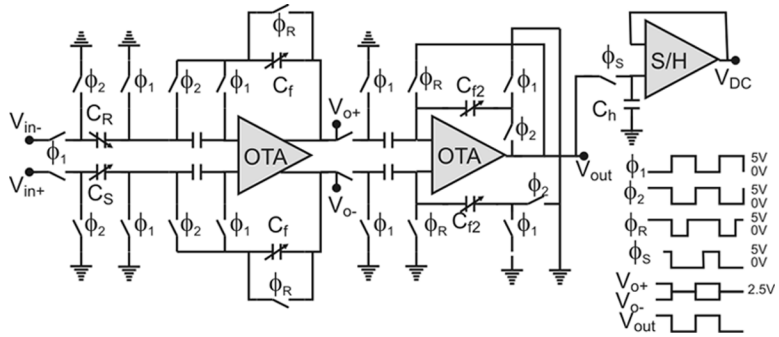

Fig. 5. Three-stage balanced input differential switched capacitor readout chain and clock signal timing.

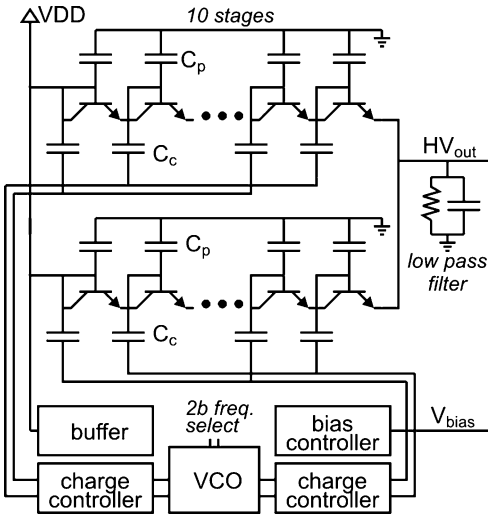

Fig. 6. Structure of the BiCMOS charge pump circuit with two parallel ten-stage pumps.

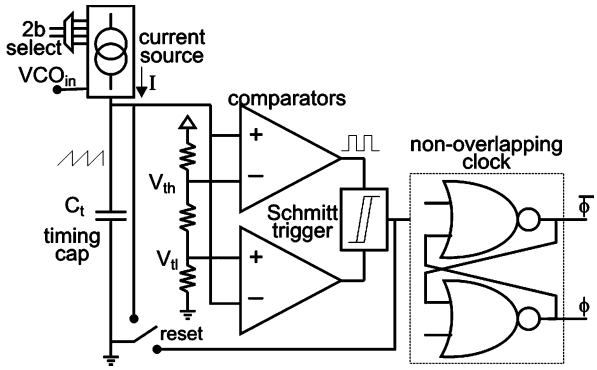

Fig. 7. Voltage-controlled oscillator used in the charge pump.

voltage changes the values of $V_{\rm in}+$ and $V_{\rm in}-$ in (4), allowing the output to be brought back to its original calibrated value.

The block level architecture of the charge pump is shown in Fig. 6. The BiCMOS charge pump is based on the Dickson pump configuration [30] and uses vertical bipolar transistors for high-voltage generation with adequate current drive/recovery capacity. For an ideal charge pump with N stages, the output voltage is given as

$$HV_{\rm out} = N\left[\left(\frac{C_c}{C_c + C_p}\right)V_\Phi - V_d\right] + V_{\rm DD} - V_d \qquad (7)$$

where C_p is the parasitic capacitance at each stage, V_ϕ is the amplitude of the clock, C_c is the charging capacitance at each stage, and V_d is the BJT diode drop (~ 0.7 V) at each stage. For a ten-stage charge pump with a clock amplitude of 5 V, a parasitic capacitance of 2 pF, and a stage capacitance of 20 pF, (7) gives an output voltage of 43.39 V. However, this assumes that the output impedance is infinite and no output current is required. When an output current is required, the voltage is reduced by

$$\Delta HV_{\rm out} = \frac{N \cdot I_{\rm out}}{(C_c + C_p) f_{\rm vco}} \qquad (8)$$

where $I_{\rm out}$ is the output current and $f_{\rm vco}$ is the VCO charge-pump frequency. Thus, to ensure the output voltage can reach 30 V, two parallel charge pump circuits have been implemented (Fig. 6). This doubles the current delivery capability and effectively halves any reduction in the output voltage due to finite output impedance.

Fig. 7 shows the VCO used in the charge pump. It consist of a programmable 2–33 MHz Schmitt-based relaxation oscillator to provide eight different output voltages up to 30 V that can be selected online. The VCO has two modes of operation. The first is the fixed-frequency mode and the other is the variable-frequency mode. In the fixed-frequency mode, the VCO frequency is programmable to four different values using a programmable current source that controls the charge supplied to the oscillator capacitor, as shown in Fig. 7. The fixed-frequency operation mode is used for dc self-test. The oscillator design uses a grounded-capacitor configuration that results in a VCO output frequency (assuming identical charging and discharging currents) given by

$$f_{\rm vco} = \frac{I}{2\Delta V_{\rm ref} C_t} \qquad (9)$$

where C_t is the timing capacitance and $\Delta V_{\rm ref} = V_{\rm th} - V_{\rm tl}$ as seen in Fig. 7. For example, when $V_{\rm th} = 3.33$ V, $V_{\rm tl} = 1.66$ V, $C_t = 6$ pF and the programmable current source is set to $\mathrm{I} = 100\ \mu$A, the frequency is 5 MHz. If the current is changed to 150 μA, the frequency becomes 7.5 MHz. The trigger points are set by the reference voltage level generated by a fixed resistive divider. The Schmitt trigger noise contribution is inversely proportional to the slope of the comparator output waveform, which is designed to be very high, making the Schmitt noise very small. The dominant factor in the jitter is the uncertainty in the switching point of the comparator as determined by the

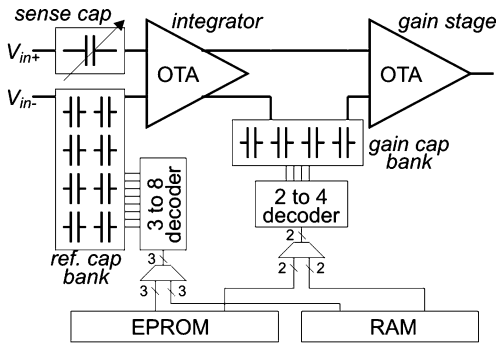

Fig. 8. Organization of memory and programmable elements for offset and gain calibration.

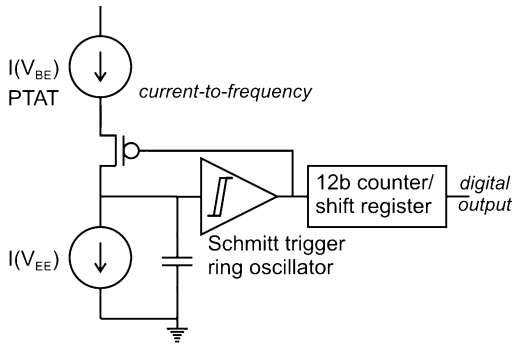

Fig. 9. Simplified schematic of the on-chip, range/sensitivity controllable, CMOS temperature sensor with digital output.

slope of the waveform across the capacitor [31] and is experimentally determined to be 4.66 ppm in this design.

As is evident from (8) and (9), we have a number of factors at our disposal to achieve dynamic control of the high-voltage output. The $V_{\rm bias}$ in Fig. 6 is adjustable from 0 to 5 V and produces a variable-amplitude charging clock (V_ϕ) for half the stages in the charge pump. It is kept fixed at $V_{\rm DD}$ for the remaining stages. This provides the ability to set the charge pump output range as desired. When (9) is substituted into (8), we have a frequency-dependent charge pump output. This permits the use of a tunable VCO to control the charge pump voltage level. At maximum current output, the charge pump can generate up to 10 mW of output power as a current driver.

The chip utilizes embedded memory to digitally configure much of its analog operation, including the high-voltage circuitry and the readout offset and gain. A 65b EPROM provides nonvolatile storage of multiple configuration parameters. EPROM outputs are multiplexed with on-chip SRAM that can be written through the bus interface circuit. Thus, the chip can either operate using preset parameters stored in EPROM, or the microsystem can choose to upload new parameters to the SRAM. Selection of EPROM or SRAM is included within the sensor read command sent through the sensor bus. Fig. 8 shows the connections of memory to programmable capacitor banks that control the offset and gain of the capacitance readout circuit, illustrating a portion of the chip's programmability.

C. Temperature Sensor

Many transducers display undesirable temperature sensitivities that can be removed using digital processing algorithms within the microsystem [1]. A temperature sensor has been integrated on-chip to facilitate compensation and provide data for general use. The temperature sensor shown in Fig. 9 uses vertical bipolar transistors and high-value resistors to generate a current that is proportional to absolute temperature (PTAT). The PTAT current is mirrored to four branches and scaled in binary weights to provide a 4b programmable current source that charges the input node of a Schmitt ring oscillator. The oscillator output pulses are counted on-chip to generate a 12b digital temperature code with an acquisition time of 1 ms. The temperature sensor is highly programmable, via digital control of charge and discharge currents, to maximize sensitivity over a broad range of temperature scales. For three example temperature ranges (a narrow 25 °C human body temperature range, a broader −30 °C to 70°C environmental range, and a very wide 300 °C range) the circuit provides an output sensitivity (one LSB of the counter) of approximately 0.009 °C, 0.026 °C, and 0.07°C, respectively.

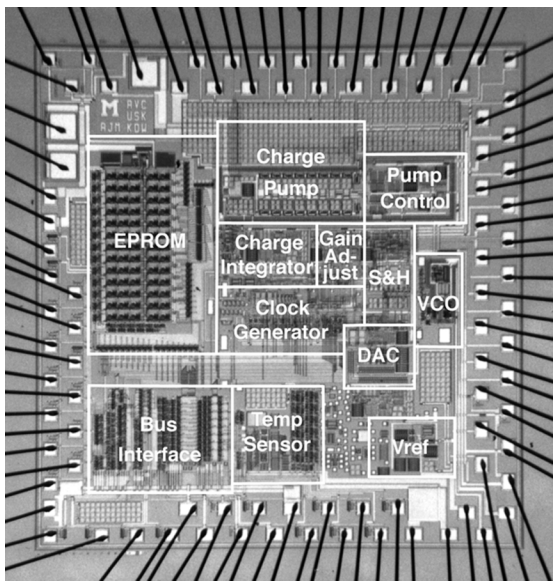

Fig. 10. Die photograph of the 4.5×4.5 mm capacitive interface chip with major functional blocks labeled. The high-voltage charge pump capacitors are shown across the top of the chip and consume roughly 6% of the chip area.

V. Test Results

The chip was realized in a 1 μm n-well BiCMOS 2 P/2 M process that permits high-voltage operation, large-value resistors, and nonvolatile on-chip memory. Fig. 10 shows a photograph of the 20 mm^2 chip, with the main functional blocks labeled. Additional bond pads are included for probing internal points on the chip and are not required for normal operation. The chip was tested at probe level and the measured characteristics of the analog readout circuit are given in Table I. Fig. 11 verifies proper operation of the switched capacitor readout circuit, showing the integration and reset cycle at the output of the second stage ($V_{\rm out}$ in Fig. 5) and the variation of the output voltage for different values of sense capacitance. To demonstrate the chip's ability to dynamically adjust readout gain, Fig. 12 shows the chip output voltage verses increasing values of the digital parameter that sets gain, where $C_{\rm s}$ and $C_{\rm r}$ are the sense and reference capacitors, respectively, tested at two different differential values. To test charge pump operation,

TABLE I
SUMMARY OF CAPACITIVE READOUT CIRCUIT TEST RESULTS

Parameter	Measured Value
Switched capacitor sensitivity	1.25mV/fF
Sampling rate	10-50kHz
Base capacitance range	16fF – 40pF
Gain range	20.8μV/fF – 1.25mV/fF
Charge pump output range	8 – 30V
OTA gain (singled ended)	75dV
OTA output swing	3V (differential) 3.9V (single ended)
OTA slew rate	0.6V/μsec
Pressure resolution	25.7mTorr (12b A/D)

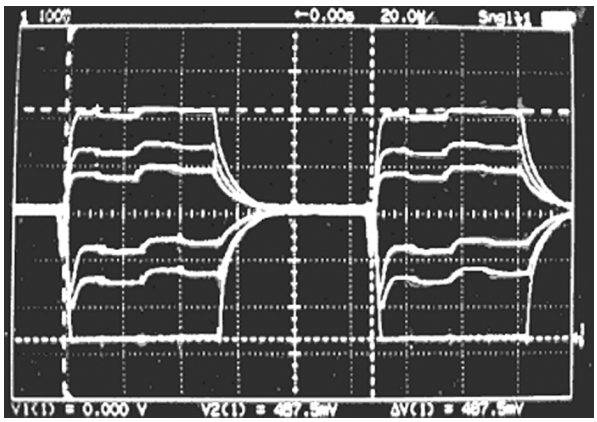

Fig. 11. Voltage transitions at the output of the gain stage (second stage) for five different sense capacitance values.

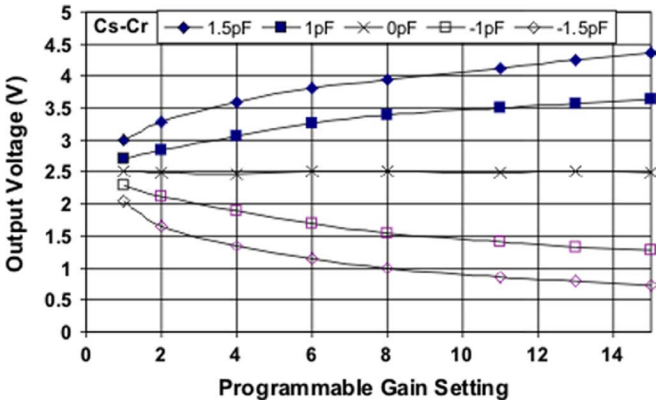

Fig. 12. Output voltage versus digitally programmable gain settings at different sense and reference capacitor ratios; voltages above 2.5 V are for $Cs > Cr$, while those below 2.5 V are for $Cs < Cr$.

its output voltage was measured for different VCO frequencies. Fig. 13 shows that the output voltage changes from 10 to 17 V when the VCO frequency changes from 2 to 8 MHz. In its typical operation mode, the chip consumes about 220 μA from a 5 V supply with a 50 kHz SC clock. This amounts to 90 nJ of energy for a single readout making it suitable for portable applications.

To verify the chip could be employed in a highly integrated multisensor microsystem, it was also extensively tested within the prototype microsystem illustrated in Fig. 14 with a MEMS barometric pressure sensor array [32], a MEMS humidity sensor [33], and the on-board temperature sensor. The two external

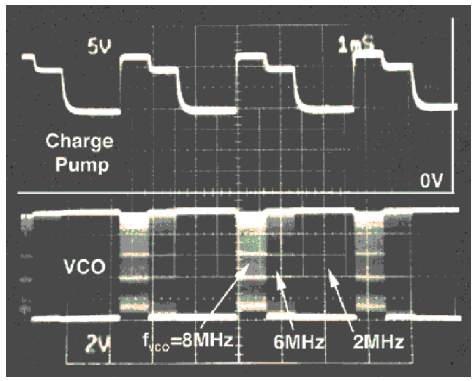

Fig. 13. Charge pump output voltage as a function of VCO frequency.

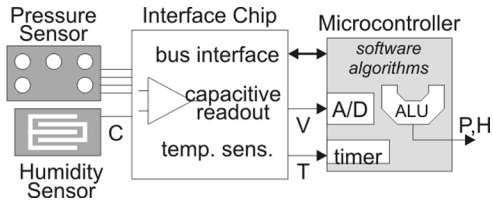

Fig. 14. Prototype microsystem implementation for testing the capacitive sensor interface chip.

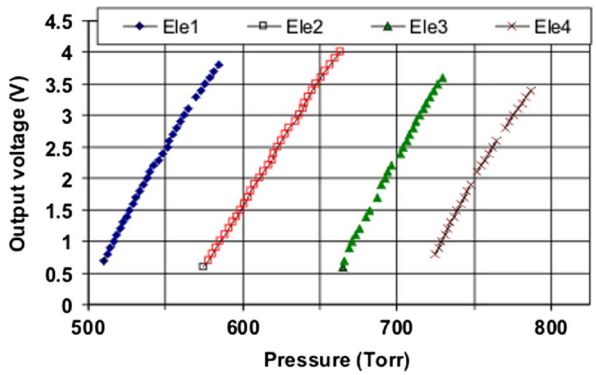

Fig. 15. Output voltage as a function of pressure for four elements of a multi-range pressure sensor array.

sensors have very different nominal capacitances and sensitivities, thus demonstrating the versatility of this adaptive circuit. The output voltage as a function of applied pressure is shown in Fig. 15 for four different elements on the sensor array simultaneously interfaced through the readout chip. With gain adjustable over two orders of magnitude, Fig. 16 shows output voltage of one pressure sensor element at four different gain settings. Similarly, Fig. 17 shows the output voltage measured from the humidity sensor verses humidity at three different gain settings.

After establishing the digital settings most appropriate to set the temperature sensor within the three ranges described above, the on-chip temperature sensor output was measured and the results plotted in Fig. 18. Analysis of test results suggests the accuracy of the sensor is better than 0.2 °C at and below room temperature decreasing to approximately 1 °C at temperatures over 100 °C due to secondary effects in the circuit or inability to hold stable temperatures in the test chamber. The uncompensated pressure sensor system temperature coefficient of offset

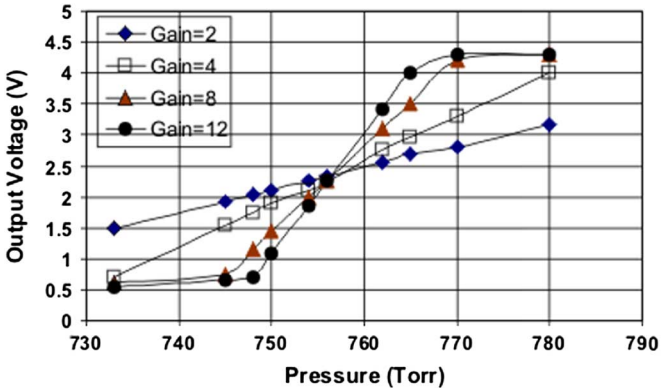

Fig. 16. Variation of output voltage for different digital gain settings versus pressure.

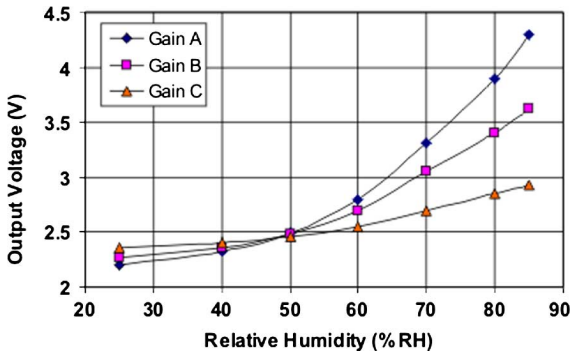

Fig. 17. Output voltage for different gain settings versus humidity.

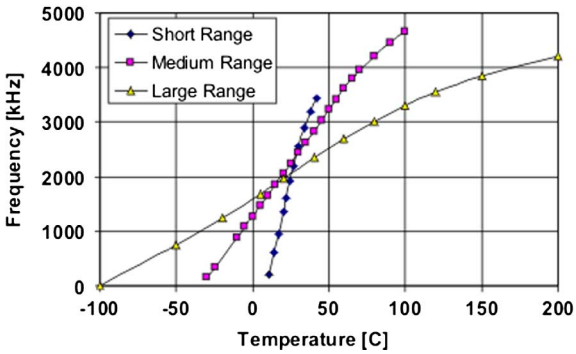

Fig. 18. Temperature sensor output for three different temperature range configurations: 15 °C–40 °C, −30 °C–70 °C, and −100 °C–200 °C.

(TCO) was found to be 3900 ppm/°C with a circuit contribution of <50 ppm/°C, and the system temperature coefficient of sensitivity (TCS) was measured as 1000 ppm/°C with a circuit contribution of <15 ppm/°C. After modeling temperature sensitivities, the system TCO was reduced to <1 ppm/°C using digital compensation via bivariate polynomial evaluation in the microsystem controller.

VI. Conclusion

A sensor interface chip has been described that combines mixed-voltage capacitive readout, high-voltage output drive, sensor bus interface, embedded EPROM, and on-chip temperature sensing into a highly configurable, highly self testable, interface solution for low-power multisensor microsystems. The bus interface allows a single microsystem to communicate with multiple sensor nodes and permits online control of the interface chip configuration parameters. The fully balanced low-noise capacitive readout circuit provides 1.25 mV/fF sensitivity for up to five sensing elements utilizing a highly adaptive structure that can read out base capacitances ranging from 16 fF to 40 pF and produce gain ranging from 20.8 μV/fF to 1.25 mV/fF. The VCO-controlled charge pump and mixed voltage front end enable the chip to drive up to 30 V outputs for electrostatic test of external sensors. The entire readout chain is specifically tailored to permit self-test and online adjustment of readout calibration parameters, which can be stored in the embedded 65b EPROM or uploaded to SRAM through the sensor bus. The on-chip, range-programmable BiCMOS temperature sensor samples the ambient environment to permit digital compensation in the microsystem controller. This 20 mm^2 chip uniquely demonstrates a successful method for incorporating mixed voltage (3–30 V) capabilities alongside highly sensitive, configurable, and testable capacitive interface circuitry.

Acknowledgment

The authors would like to thank Delphi Delco Electronics Corporation for assistance with simulation models and wafer fabrication.

References

[1] A. Mason, N. Yazdi, A. V. Chavan, K. Najafi, and K. D. Wise, "A generic multielement microsystem for portable wireless applications," *Proc. IEEE (Invited)* , vol. 86, no. 8, pp. 1733–1745, 1998.

[2] D. F. Lemmerhirt and K. D. Wise, "Chip-scale integration of data-gathering microsystems," *Proc. IEEE*, vol. 94, no. 6, pp. 1138–1159, 2006.

[3] G. Yeh, I. Dendo, and W. Ko, "Switched capacitor interface circuit for capacitive transducers," in *Proc. Int. Conf. Solid-State Sensors and Actuators*, Philadelphia, PA, Jun. 7–11, 1985, pp. 60–63.

[4] A. Kjensmo, A. Hanneborg, J. Gakkestad, and H. von der Lippe, "A CMOS front end circuit for capacitive pressure sensor," *Sens. Actuators A*, vol. 21, pp. 102–107, 1990.

[5] M. Yamada, T. Takebayashi, S. Notoyama, and K. Watnabe, "A switched capacitor interface for capacitive pressure sensors," *IEEE Trans. Instrum. Meas.*, vol. 41, no. 1, pp. 81–86, Feb. 1992.

[6] B. Boser and R. T. Howe, "Surface micromachined accelerometers," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1995, pp. 337–344.

[7] F. Schnatz, U. Schoneberg, W. Brockherde, P. Kopystynski, T. Mehlhorn, E. Obermeir, and H. Benzel, "Smart CMOS capacitive pressure transducer with on-chip calibration capability," *Sens. Actuators A*, vol. 34, pp. 77–83, 1992.

[8] F. M. L. van der Goes and G. C. M. Meijer, "A universal transducer interface for capacitive and resistive sensor elements," *Analog Integrated Circuits and Signal Process.*, vol. 14, no. 3, pp. 249–260, 1997.

[9] H. K. Trieu, M. Knier, O. Koster, H. Kappert, M. Schmidt, and W. Mokwa, "Monolithic integrated surface micromachined pressure sensors with analog on-chip linearization and temperature compensation," in *Proc. Int. Conf. Micro. Electro. Mech. Syst.*, Jan. 23–27, 2000, pp. 547–550.

[10] N. Yazdi, A. Mason, K. Najafi, and K. D. Wise, "A generic interface circuit for capacitive sensors in low-power multi-parameter microsystems," *Sens. Actuators: A*, vol. 84, pp. 351–361, 2000.

[11] D. Preethichandra and K. Shida, "A simple interface circuit to measure very small capacitance changes in capacitive sensors," *IEEE Trans. Instrum. Meas.*, vol. 50, no. 6, pp. 1583–1586, Dec. 2001.

[12] H. Kapels, R. Aigner, and C. Kolle, "Monolithic surface-micromachined sensor system for high pressure applications," in *Proc. Int. Conf. Solid-State Sens. Actuators*, Munich, Germany, Jun. 10–14, 2001.

[13] G. Chao, L. Xiujun, and G. C. M. Meijer, "A system-level approach for the design of smart sensor interfaces," in *Proc. IEEE Conf. Sensors*, Oct. 2004, pp. 210–214.

[14] J. Wu, G. K. Fedder, and L. R. Carley, "A low-noise low-offset capacitive sensing amplifier for a 50 μg/sqrt Hz monolithic CMOS MEMS accelerometer," *IEEE J. Solid-State Circuits*, vol. 39, pp. 722–730, 2004.

[15] W. Bracke, P. Merken, R. Puers, and C. van Hoof, "Design methods and algorithms for configurable capacitive sensor interfaces," *Sens. Actuators A*, vol. 125, no. 1, pp. 25–33, 2005.
[16] M. Yamada and K. Watanabe, "A capacitive pressure sensor interface using oversampling $\Sigma\Delta$ demodulation techniques," *IEEE Trans. Instrum. Meas.*, vol. 46, pp. 3–7, Feb. 1997.
[17] C. Hierold, B. Clasbrumme, D. Behrend, T. Scheiter, M. Steger, K. Oppermann, H. Kapels, E. Landgraf, D. Wenzel, and D. Etuodt, "Implantable low power integrated pressure sensor system for minimal invasive telemetric patient monitoring," in *Proc. Int. Micro. Electro. Mech. Syst. Workshop*, Jan. 25–29, 1998, pp. 568–573.
[18] J. Kung, H. Lee, and R. Howe, "A digital readout technique for capacitive sensor applications," *IEEE J. Solid-State Circuits*, vol. 23, no. 4, pp. 972–977, Aug. 1988.
[19] T. Nagata, H. Terabe, S. Kuwahara, S. Sakurai, O. Tabata, S. Sugiyama, and M. Esashi, "Digital compensated capacitive pressure sensor using CMOS technology for low pressure measurements," in *Proc. Int. Conf. Solid-State Sens. Actuators*, 1991, pp. 308–311.
[20] K. Mochizuki, K. Watanabe, T. Masuda, and M. Katsura, "A relaxation oscillator based interface for high-accuracy ratiometric signal processing of differential capacitance tranducers," *IEEE Trans. Instrum. Meas.*, vol. 47, no. 1, pp. 11–15, 1998.
[21] M. Smith, L. Bowman, and J. Meindl, "Analysis, design and performance of a capacitive pressure sensor IC," *IEEE Trans. Biomed. Eng.*, vol. 33, no. 2, pp. 163–173, Feb. 1986.
[22] O. Machul, D. Hammerschmidt, W. Brockherde, B. Hosticka, E. Obermeier, and P. Krause, "A smart pressure transducer with on-chip readout, calibration and nonlinear temperature compensation based on spline functions," in *Proc. IEEE Int. Solid State Circuits Conf.*, 1997, pp. 198–199.
[23] G. Horn and J. Huijsing, "Programmable analog signal processor for polynomial calibration," in *Proc. ESSCIRC*, Neuchatel, Switzerland, 1996, pp. 400–403.
[24] S. B. Crary, W. G. Baer, J. C. Cowles, and K. D. Wise, "Digital compensation of high performance silicon pressure transducers," *Sens. Actuators A*, vol. 21–23, pp. 70–72, 1990.
[25] R. Reed, "Memory having programmed margin verification feature," U.S. Patent 5796655, 1998.
[26] D. Senderowicz, S. F. Dreyer, J. H. Huggins, C. F. Rahim, and C. A. Laber, "A family of differential NMOS analog circuits for a PCM codec filter chip," *IEEE J. Solid-State Circuits*, vol. 17, no. 6, pp. 1014–1023, Dec. 1982.
[27] K. Hsieh, P. Gray, D. Senderowicz, and D. Messerschmitt, "A low-noise chopper-stabilized differential switched capacitor filtering technique," *IEEE J. Solid-State Circuits*, vol. 16, pp. 708–715, Dec. 1981.
[28] P. R. Gray and R. G. Myer, *Analysis and Design of Analog Integrated Circuits*, 3rd ed. New York: Wiley.
[29] D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley, 1997.
[30] J. F. Dickson, "On-chip high voltage generation in NMOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid State Circuits*, vol. 11, pp. 374–378, 1976.
[31] A. A. Abidi and R. G. Myer, "Noise in relaxation oscillators," *IEEE J. Solid State Circuits*, vol. 18, no. 6, pp. 794–802, Dec. 1983.
[32] A. V. Chavan and K. D. Wise, "A multi-lead vacuum-sealed capacitive pressure sensor," in *Proc. Dig. Solid-State Sens. Actuator Workshop*, Hilton Head, SC, Jun. 1998, pp. 212–215.
[33] U. Kang and K. D. Wise, "A high-speed capacitive humidity sensor," in *Proc. Dig. Solid-State Sens. Actuator Workshop*, Hilton Head, SC, Jun. 1998, pp. 183–186.

Andrew Mason (S'90–M'99–SM'06) received the B.S. degree in physics (Highest Distinction) from Western Kentucky University, Bowling Green, in 1991, the B.S.E.E. degree (Hon.) from the Georgia Institute of Technology, Atlanta, in 1992, and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 1994 and 2000, respectively.

From 1997 to 1999, he was an Electronic Systems Engineer at a small aerospace company, and from 1999 to 2001, he was an Assistant Professor at the University of Kentucky. In 2001, he joined the Department of Electrical and Computer Engineering, Michigan State University, East Lansing, where he is currently an Assistant Professor. His research addresses many areas of mixed-signal circuit design and the fabrication of integrated microsystems. Current projects include adaptive sensor interface circuits, bioelectrochemical interrogation circuits, post-CMOS fabrication of electrochemical sensors, and integrated circuits for neural signal processing.

Dr. Mason received the Michigan State University Teacher-Scholar Award in 2006. He serves on the Sensory Systems and Biomedical Circuits and Systems Technical Committees of the IEEE Circuits and Systems Society and the on the Technical Program Committee for IEEE International Conference on Sensors.

Abhijeet V. Chavan received the B.S.E.E. degree (Highest Distinction) from Maharaja Sayajirao University, Baroda, India, in 1983, the M.S.E.E. from Syracuse University, Syracuse, NY, in 1989, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 1999.

From 1983 to 1987, he was a Design Engineer with Siemens A.G. responsible for industrial automation products. From 1988 to 1991, he was with Coherent Research, Inc., NY, working on VLSI content addressable memory (CAM)-based associative processor development, object oriented programming, and NASA SBIR programs on VHDL compilers. From 1991 through 2003, he held various engineering and project management positions with Delphi Delco Electronics Systems working on the design, fabrication, and testing of MEMS sensors, VLSI, and mixed-signal semiconductor circuits. His work at Delphi involved areas such as engine management systems, monolithically integrated thermal infrared and capacitive sensor systems, calibration/compensation ASICs, special packaging techniques for sensors, and application of automotive sensor technology to the medical field. At present, he is Manager of Research and Technology at Boston Scientific responsible for design and development of chronically implanted medical devices and diagnostic sensors in the Cardiac Rhythm Management field. He has multiple U.S. patents and publications in the fields of circuits, sensors, and implantable medical devices.

Kensall D. Wise (S'61–M'69–S'83–F'86–LF'07) received the B.S.E.E. degree (Highest Distinction) from Purdue University, West Lafayette, IN, in 1963, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1964 and 1969, respectively.

From 1963 to 1965 (on leave 1965–1969) and from 1972 to 1974, he was a Member of Technical Staff at Bell Telephone Laboratories, where his work was concerned with the exploratory development of integrated electronics for use in telephone communications. From 1965 to 1972, he was a Research Assistant and then a Research Associate and Lecturer in the Department of Electrical Engineering, Stanford University, working on the development of integrated circuit technology and its application to solid-state sensors. In 1974, he joined the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, where he is now the J. Reid and Polly Anderson Professor of Manufacturing Technology and Director of the NSF Engineering Research Center for Wireless Integrated MicroSystems. His present research interests focus on the development of integrated microsystems for health care and environmental monitoring.

Dr. Wise is a member of the United States National Academy of Engineering. He organized and served as the First Chairman of the Technical Subcommittee on Solid-State Sensors of the IEEE Electron Devices Society (EDS). He was General Chairman of the 1984 IEEE Solid-State Sensor Conference, Technical Program Chairman of the IEEE International Conference on Solid-State Sensors and Actuators (1985), and IEEE-EDS National Lecturer (1986). He served as General Chairman of the 1997 IEEE International Conference on Solid-State Sensors and Actuators. He received the Paul Rappaport Award from the EDS (1990), a Distinguished Faculty Achievement Award from the University of Michigan (1995), the Columbus Prize from the Christopher Columbus Fellowship Foundation (1996), the SRC Aristotle Award (1997), and the 1999 IEEE Solid-State Circuits Field Award. In 2002, he was named the William Gould Dow Distinguished University Professor at the University of Michigan.