Characterization of a Configurable Sensor Signal Conditioning Circuit for Multi-Sensor Microsystems

Jichun Zhang and Andrew Mason
Electrical and Computer Engineering, Michigan State University, East Lansing, MI 48824, USA
{zhangjic, mason}@egr.msu.edu

Abstract
This paper describes the sensor signal conditioning circuitry within a transducer interface chip containing a digital communication interface, configuration memory, and programmable analog and digital outputs for actuator control. The highly configurable sensor readout circuits provide front-end signal conditioning for a wide range of capacitive, resistive, voltage, and current output devices. The mixed-mode interface supports up to eight sensors simultaneously and is ideally suited for multi-sensor microsystems. The circuit provides high resolution for each readout mode, including less than 1fF for capacitive sensors, and introduces a versatile bridge circuit for single element, half-bridge, or full-bridge resistive sensors. Operation ranges for the configurable interfaces are reported along with the performance specifications for the fully functional 2.2x2.2mm chip fabricated in 0.5μm CMOS.

INTRODUCTION
The compatibility between IC fabrication processes and microsensor design provides new opportunities for tight integration of sensing elements and electronic components [1]. This has lead to a trend towards miniaturizing and combining Micro-Electro-Mechanical Systems (MEMS) and associated interfaces, signal processing and networking. In the resulting integrated microsystems there is strong motivation for modular components that enhance the versatility, utility and manufacturability of the microsystem [2]. In this approach, the sensor interface circuit is a key component that converters low-level sensor outputs to useful electronic signal, performs signal conditioning, and provides communication to a microsystem controller. Sensor interfaces have received much attention in recent literature [3-7]. However, most of these efforts focus on interfaces for specific or limited subsets of the sensors available with modern technologies. Many current and anticipated applications for low power microsystems require a combination of sensors and actuators to properly interface to the broad diversity of physical, biochemical, etc. real world phenomena. Such applications include distributed sensing and control systems, industrial process automation, instrumentation, and environmental monitoring. In order to support various multi-parameter microsystem configurations and the wide range of transducers they might employ, a mixed-mode multi-sensor signal conditioning and actuator control circuit is necessary.

The mixed signal circuit presented in this paper satisfies all the requirements of a universal transducer interface for multi-parameter microsystems, which include: i) readout for a variety sensors with a various spans and sensitivities, ii) on-line offset and gain control, iii) digital and analog actuator control, iv) communication with the main microsystem controller, v) support of plug-n-play function, vi) support of self-test and self-calibration, vii) low power dissipation, and viii) no external components required. This paper describes circuitry for low-level signal conditioning of capacitive, resistive, voltage and current mode sensors contained within a multifunctional transducer interface chip [8].

CIRCUIT ARCHECTURE
Figure 1 shows the block diagram of the configurable multi-sensor signal conditioning circuit. The circuit includes an analog signal router controlled by a sensor mode register, four front-end readouts blocks, a programmable gain stage, a sample & hold stage, two DACs, a voltage reference and a two-phase non-overlapping clock generator.

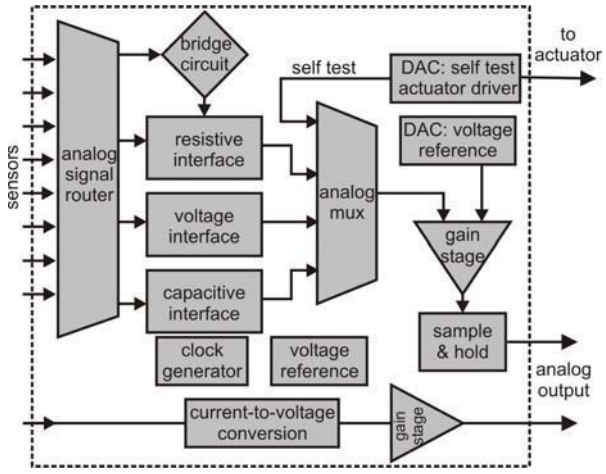


Figure 1. Diagram of the mixed-mode multi-sensor readout circuit block.

Compared to the previously reported versions of this interface circuit [7,8], a configurable resistive bridge and a current readout interface have been added to form a more versatile interface. The analog multiplexer and switches used to program the reconfigurable circuits have also been optimized to improve performance.

Resistive interface

Typically resistive sensors develop a voltage that varies with resistance using a full resistive bridge that converts an imbalance in resistor values to a voltage. However some resistive sensors do not contain the full resistive bridge built in to the transducer and some may not include a reference resistor. A versatile resistive interface, as shown in Figure 2, has been developed to accommodate all of these configurations by utilizing a configurable potion of an on-chip, programmable-resistance bridge.

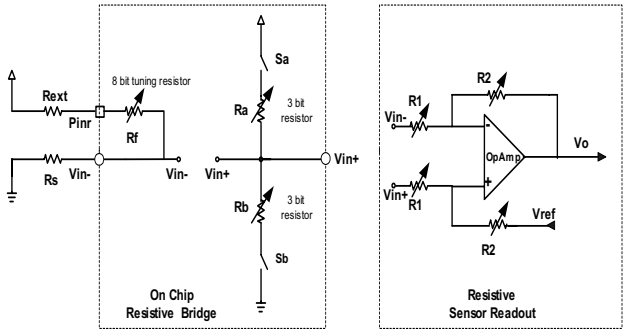


Figure 2. Resistive sensor readout.

The on-chip bridge contains two 3-bit (5KΩ to 35KΩ) programmable resistors and one 8-bit (50Ω - 8.75KΩ) binary-weighted tuning resistor. The circuit can interface with external full bridge, half bridge resistive sensors, or a single resistor as follows:

External full bridge: Switches Sa, Sb are off and external reference, R_{ext}, is unconnected. The two outputs of the sensor bridge are connected directly to Vin+ and Vin-.

External half bridge: Switches Sa, Sb are on to activate the on-chip reference branch. External reference, R_{ext}, is unconnected. The output of the half bridge sensor is connected to Vin-.

External single resistor: Switches Sa, Sb are on to activate the on-chip reference branch. R_{ext} is added externally for rough control of the reference resistor and an 8-bit on-chip tuning resistor is used for fine control.

The bridge output voltage is applied to the input of a closed loop differential amplifier. The gain of this amplifier is given by the ratio of *R2* to *R1*, where *R1* and *R2* are 2-bit and 4-bit programmable controlled, respectively. For an opamp used in resistive readout, a high gain is required to ensure precision operation, large output voltage swing is required to accommodate a large output signal, and the output needs to be buffered to drive current into a resistive load. The output voltage for single resistive sensor readout can be expressed as:

$$V_{out} = V_{ref} + \frac{\frac{R_s}{R_{ref}} - \frac{R_b}{R_a}}{\left(1 + \frac{R_s}{R_{ref}}\right)\left(1 + \frac{R_b}{R_a}\right)} \cdot V_{dd} \cdot \frac{R_2}{R_1} \qquad (1)$$

In full bridge and half bridge configurations, the output voltage of the resistive readout is determined by:

$$V_{out} = V_{ref} + (V_{in-} - V_{in+}) \cdot V_{dd} \cdot \frac{R_2}{R_1} \qquad (2)$$

Capacitive and voltage interfaces

The capacitive and voltage readout blocks are based on those we have previously reported [7], but this version of the chip includes modifications to the physical design of passive elements that improve matching and increase the sensitivity compare to prior implementations. The output voltage of the capacitive and resistive readout blocks can be expressed as:

$$V_{out} = \begin{cases} V_{ref} + k_c \cdot (C_s - C_{ref}) \\ V_{ref} + k_v \cdot (V_{in} - V_{ref}) \end{cases} \qquad (3)$$

where k_c is the sensitivity coefficient for capacitive readout, k_v is the gain setting for voltage readout, *Cs* is the sensor capacitance, *Cref* is the on-chip reference capacitance, *Vin* is the sensor voltage output, and *Vref* is the analog ground.

Current interface

The current readout interface, designed for amperometric sensors, is shown in Figure 3. It includes a low noise switched capacitor integrator and programmable gain stage with offset cancellation [9]. During phi1, the offset charge is stored on both *Cs* and *Cf*. During phi2, the offset charge on *Cs* enters *Cf* with opposite polarity and then the total offset charges cancel each other. The current readout block is programmable and designed to measure currents from 10nA to 10uA with high linearity.

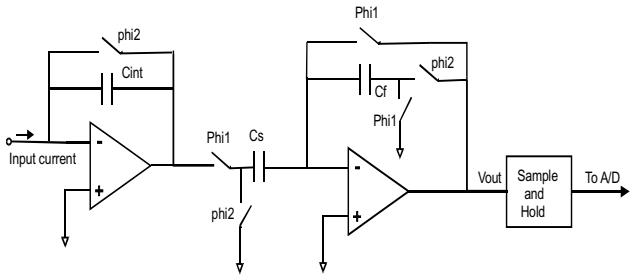


Figure 3. Diagram of current sensing block.

DESIGN CONSIDERATIONS AND REALIZATION

Significant attention was paid to the physical design of this mixed signal circuit. Common centroid layout techniques were used to reduce input offsets and match passive component values. Charge injection was also reduced by using delayed clocks on switches in the circuit design [8]. All switches in the critical signal path were realized as CMOS switches to reduce resistance and allow full voltage swings. Separate power and ground rails were created for the digital and analog blocks to reduce supply noise. Sensitive signal paths were surrounded by a guard ring with ample substrate contacts.

The overall interface chip, which includes the mixed-mode sensor signal conditioning circuit, was fabricated in 0.5um CMOS process. Figure 4 shows the chip photo of the 2.2x2.2mm die. To minimize the power consumption, the chip uses several power lines allowing only the blocks necessary for specific applications to be powered up. With all block powered at 3.3V, the chip draws 3.3mA.

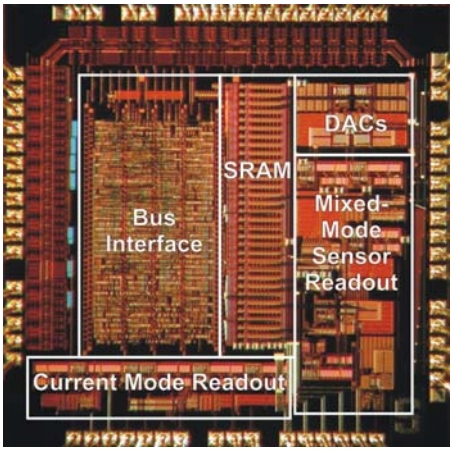
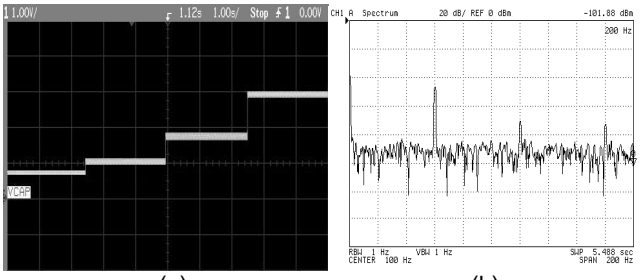


Figure 4. Die photo of the overall sensor interface chip, which includes the circuitry reported here along with a sensor bus interface block and on-chip memory.

MEASURED RESULTS

The performance of the mixed-mode multi-sensor circuit has been carefully evaluated. The circuit was designated to operate with a 50 kHz clock, and both the non-overlap time of the clock phases and the clock delays were 250ns. Simulation results indicate the circuitry works from 10kHz to 100kHz. Capacitive readout measurements were performed at 50kHz while the remaining blocks were verified at 10kHz. Figure 5 (a) shows the output waveform for capacitive readout, which agrees with the simulation very well. Figure 5 (b) shows the measured noise level of capacitive readout with about -90dBm noise power. The spikes in Figure 5(b) are due to 60Hz power supply noise and associated harmonics. Measured response of the capacitive interface is plotted in Figure 6 at several PGA gain settings while fixing the off chip (sensor) capacitance and varying the on-chip reference in 50fF steps. The response is very linear with sensitivity of 1mV/fF, 2mV/fF, and 4mV/fF at setting of 1V/V, 2V/V, and 4V/V, respectively, in the PGA stage.

Voltage readout and half bridge resistive readout were evaluated by applying a 100Hz test signal to the inputs of analog signal router. By controlling the sensor mode register, output waveforms corresponding to voltage and resistive readouts, respectively, are plotted in Figure 7. The attenuation capability of the voltage interface was 0.125 to 1.0V/V. This signal can be further scaled by the PGA stage with a programmable gain range of 0.035 to 31.75V/V. Functionality of the resistive interface was confirmed and measurements showed a sensitivity of 2mV/50Ω at unity gain in the PGA for a nominal sensor/reference value of 22kΩ.



(a) (b)

Figure 5. (a) Sample-and-hold output for capacitive readout with 2.5pF reference and sensor capacitances of 1.66pF, 2.0pF, 2.5pF, and 3.3pF. (b) Noise level of capacitive readout with about –90dBm noise power.

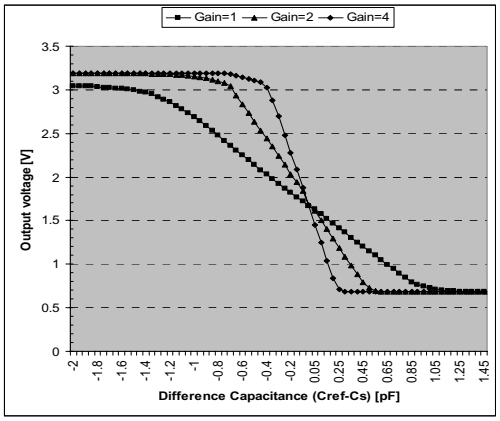
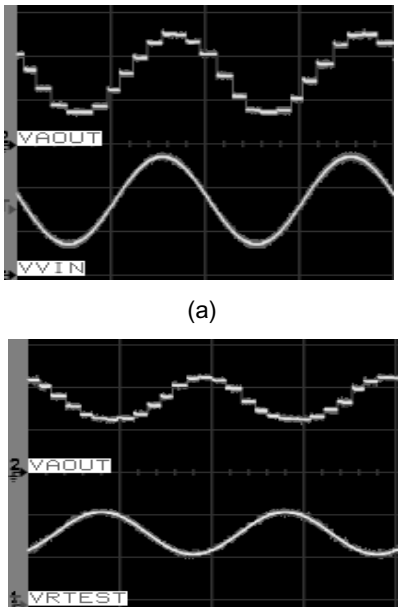


Figure 6. Measured performance of capacitive readout at different gain settings in the PGA stage.



(a)

(b)

Figure 7. Voltage (a) and resistive half bridge (b) readout at the sample-and-hold output with unity gain.

Figure 8 shows a spectrum analysis of (a) a 100Hz input signal and output signals for (b) voltage readout and (c) resistive readout. This measurement verifies that the circuits have good noise performance and that the unity gain setting is very close to 1V/V. The gain variation is due to resistance mismatch of the programmable resistors in the prestage amplifier.

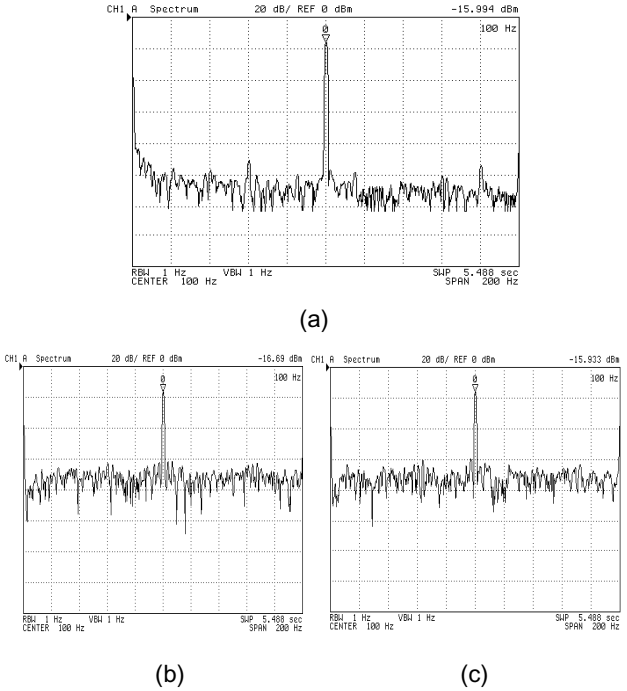


Figure 8. Spectrum analysis of (a) input test signal; input signal power –15.99dBm, input noise level –110dBm; (b) output of voltage readout; output signal power –16.69dBm, output noise level –75dBm; (c) output of resistive readout; output signal power –15.93dBm, output noise level –78dBm.

At maximum gain settings, this circuit provides sensitivity of 30mV/fF for capacitive readout and 18mV/Ω for resistive readout (single sensor element configuration). The capacitive interface can resolve capacitance variations of less than 1fF in a 10Hz bandwidth and resistance variations of less than 10Ω with a nominal sensor resistance of 22kΩ (resistive resolution varies directly with nominal sensor resistance). The current mode block provides high sensitivity current-to-voltage conversion and can be programmed to operate over various ranges of nominal sensor output current, from 10nA to 10uA.

CONCLUSIONS

A configurable signal conditioning circuit for readout of capacitive, resistive, voltage, and current output sensors has been presented. The circuit supports up to eight sensor inputs and features highly programmable gain and offset control ideally suited for multi-sensor microsystems. The entire 2.2x2.2mm chip, including self-test and actuator control DACs, dissipates 3.3mW but can be configured for lower power consumption by disabling some circuit features. Tests of the fabricated circuit verify proper functionality and high readout sensitivity and resolution, including 30mV/fF with better than 1fF resolution for capacitive readout and 18mV/Ω with better than 10Ω resolution for resistive readout.

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