CMOS Monolithic Chemiresistor Array with Microfluidic Channel for Micro Gas Chromatograph

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Abstract—A monolithic chemiresistor (CR) array micro-system with microfluidic channel for micro gas chromatograph (μGC) is presented in this paper. A CMOS readout chip was designed for amplifying and conditioning the signal of a 4x2 MPN-coated CR array fabricated on the surface of the CMOS chip. A micro glass lid with input and output capillary tubes was developed as a gas flow channel and mounted on the CMOS array, providing an interface to a micro flow column in a μGC platform. After all of the CMOS-compatible processing, the monolithic CR array was tested within a GC platform, and both the CR array and circuit were demonstrated to function as designed.

I. INTRODUCTION

Gas chromatography (GC) is a technology that permits detection, classification and quantification of gas and vapor mixtures, showing wide application in environmental monitoring, military surveillance, and healthcare diagnostics[1, 2]. Traditional GC instruments demonstrate high detection specificity and sensitivity; however due to their bulky size and high cost, they are not suitable for on-site detection. Miniaturization of the GC to a portable platform referred to as a micro gas chromatograph (μGC) brings significant benefits in terms of speed, sensitivity, and cost [3], and opens new sensing applications that were impossible with traditional GC instruments.

A GC consists of three main components: pre-concentrator (PCF), flow column and detector. The PCF collects the sample and increases the concentration of target. The flow column then spatially separates the analytes with assistance of resistive heaters. Finally the detector generates a temporal electrical signal corresponding to the concentration and arrival time of target analytes. Typically, the detector consists of sensor arrays that produce unique responses to different analytes and instrumentation electronics that provide amplification, signal conditioning, and communication of sensor data to external systems. Considerable research has been devoted in the past couple of decades to the miniaturization of a μGC platform with notable success in miniaturization of several components including micro PCFs, micro columns, and micro sensors [3-5]. However, monolithic integration of the entire detector subsystem remains an open challenge.

Thiolate-monolayer-protected gold nanoparticle (MPN) coated chemiresistor (CR) arrays have been reported as a suitable technology for μGC because of advantages including facile fabrication, low-temperature operation, high sensitivity and favorable scaling behavior that permits miniaturization without loss of sensitivity[6, 7]. However, at its detection limit, the response of the MPN-coated CRs is easily overwhelmed by environmental noise. One solution to significantly reduce noise coupled through wiring is to directly fabricate CR arrays on surface of the instrumentation chip. Such a monolithic detector chip would also provide further miniaturization for the μGC system. A monolithic detector would require a microfluidic flow channel on the surface to connect with other μGC components and ensure the sample remains in close proximity to the miniaturized sensor array. This paper reports the first known monolithic implementation of an MPN-coated CR array detector subsystem for μGC applications. The integrated microsystem combines a CR array, a CMOS readout circuit, and a microfluidic channel within a single chip. Compatibility challenges in integrating these diverse components are analyzed and solutions are presented. The design and implementation of readout circuitry, on-chip CR array, and microfluidic chamber are then discussed. The performance of each component is described, and a fully integrated monolithic CR array microsystem is demonstrated within a GC platform.

II. COMPATIBILITY CHALLENGES

Several important compatibility challenges were discovered in integrating CR sensor arrays, CMOS readout circuits, and microfluidic channels into a single chip. Experimental observations and the solutions developed are presented in this section.

First, experimental efforts to form interdigitated electrodes (IDEs) for a MPN-coated CR array on the surface of CMOS chips demonstrated a problem related to the flatness of the chip’s surface. Because the MPN-CR sensor electrodes are formed using thin metal layers with 600nm thickness, they require an extremely flat surface to avoid trace discontinuities in the electrodes and their connections to on-chip contact openings. However, most CMOS processes, including AMI 0.5μm process used in this research, do not planarize the surface after the top-most metallization, and top metal routings create sharp steps in the surface topography. To solve this challenge without additional process steps to planarize the chip’s surface, two options were explored. One was to eliminate any top metal routing within the sensor area, and the other was to cover the entire sensor area with the top metal
layer. Both options are equally disruptive to routing of CMOS circuitry, but the second option was chosen because creating a top-metal plateau beneath the sensor electrodes helps achieve metal fill factor requirements.

Second, fabrication of the MPN-coated CRs requires an electron beam lithography (EBL) crosslinking process that, when applied to on-CMOS CRs, was observed to cause defects in the circuits beneath the sensor area. The defect principle can be explained as follows: the high-energy electron beam can stimulate electron-hole pairs in the thin gate oxide. Compared to the higher mobility of electrons, holes have a high probability to be trapped in oxide defects, creating a layer of positive charge in the gate oxide [8]. The trapped charge $Q_{ox}$ creates a shift in the transistor’s threshold voltage $\Delta V_{th}$ which is given by

$$\Delta V_{th} = -\frac{Q_{ox}}{C_{ox}}$$  \hspace{1cm} (7)

where $C_{ox}$ is the gate oxide capacitance. Shifts in threshold voltage can have a major impact on analog circuits and, as was observed, can cause an entire analog block to fail. To solve this problem, several options were identified. Annealing has been shown to be a promising solution to remove trapped charge [8]. Alternatively, a grounded metal layer above the circuits could possibly isolate the substrate from EBL effects. Finally, because high-energy electrons travel only a very limited distance (~10 $\mu$m) from their point of impact, the EBL exposure region could be physically separated from the circuit region without losing significant silicon area.

To evaluate the effect of the EBL on CMOS circuit and test the potential solutions identified above, a test chip with a transistor array was designed and exposed under a 30keV electron beam with a dose of 150 $\mu$C/cm$^2$. Fig. 1(a) shows three transistors’ threshold voltage shift after EBL, one without any metal covering, one with one metal layer and one with two metal layers. All metals were grounded during the EBL process. All options show significant threshold shift, indicating the grounded metal cannot block the high-energy electrons. Fig. 1(b) shows the threshold voltage shift of a transistor after EBL exposure and after subsequent annealing for 8 hours at 200°C. The annealing attenuated but could not completely eliminate the EBL effect. Fig. 1(c) shows the threshold voltage shift of three transistors at different distances from the EBL exposure spot. The results demonstrate that the EBL-induced threshold shift decreases significantly with distance from the point of exposure, with 120 $\mu$m distance proving sufficiently safe. In conclusion, the best solution is to separate the circuit region from CR array region by a distance of at least 120 $\mu$m.

The third compatibility challenge relates to the placement of the sensor region on the chip’s surface. As described below, the design chosen for the microfluidic channel requires minimizing the number of wire bonds to provide more chip surface area to attach a lid. To solve this challenge, a serial peripheral interface (SPI) was implemented for digital communication to minimize the number of I/O signals, and all of the required bond pads were placed on one side of the chip, simplifying placement of the microfluidic lid.

III. CMOS MONOLITHIC ARRAY IMPLEMENTATION

Based on challenges analyzed and schemes chosen, a monolithic CR array microsystem that satisfies these constraints is illustrated in Fig 2. A silicon chip containing CMOS readout circuitry serves as the substrate of the microsystem. The functional readout circuit is placed apart from CR array region to avoid EBL damage. An array of MPN-coated CRs is placed in the middle of the chip surface to facilitate post-wire-bonding microfluidic chamber fabrication. The CRs are connected through overglass contact openings to the underlying CMOS electronics. A microfluidic glass lid with capillaries is mounted on the surface of the chip and serves as a vapor flow chamber, providing an interface to the micro column in the $\mu$GC system. Wirebonded pads are only placed on one side of the chip, to facilitate chamber mounting.

A. Readout Circuity Implementation

The normalized resistance change ($\Delta R/R_0$) of an MPN-coated CR sensor is directly related to the concentration of target vapors. However, the sensor response portion of the CR, $\Delta R$, is small and buried within the large total value $\Delta R + R_0$. Furthermore, $R_0$ varies widely from sensor to sensor. To acquire $\Delta R/R_0$ with high resolution and wide dynamic range, a baseline resistance cancelation approach that subtracts $R_0$ from the total CR resistance and digitizes the $\Delta R$ portion was adapted and implemented by an 8-channel readout IC chip containing a subtraction and gain block, a wide-range programmable exponential current bias, an 8-bit DAC for analog memory (AM), a digital communication and control circuit. Details of this circuit design were reported previously [9].
B. On-CMOS CR Array Implementation

A 4x2 electrode array with individual electrode separation of 200µm was fabricated on the surface of the CR readout chip. Due to the highly resistive nature of the nanoparticle films, IDEs, fabricated via EBL, are adapted to bring the CR resistance into the megohm range. The 75×75 µm² active area of each CR is comprised of 62 pairs of electrodes of 300 nm width and spacing. The IDEs are defined by a liftoff process of evaporated metal consisting of a 50 Å adhesion layer of titanium (Ti) followed by 600 Å of gold (Au). The IDEs are fabricated on an area of the chip where there are 20×20 µm² contact pads used to connect the CRs to the embedded circuitry. Because these contact pads are recessed from the surface by several microns, it is not possible to connect to them with EBL. Contact pads on the CRs are connected to the contact pads via photolithography and a liftoff procedure of 100/1000 Å of Ti/Au.

Due to the small size of the chip, traditional deposition methods, such as air brushing or syringe coating of MPNs, could not be used. To precisely control the placement of the films, deposition was done with a Microfab Jetlab 4 micro-dispensing system. Even with this deposition system, the minimum size of the dried film is larger than the area of the IDEs and range from 100 - 200µm in diameter. The resulting films are also highly non-uniform. As each droplet dries on the surface, a coffee stain pattern [10] is formed where the majority of the nanoparticles settle in a thick ring, leaving the interior with a significantly thinner film. To account for this, we aim at the edge of the coffee stain, the thickest portion of the film, directly on top of the desired IDE. CRs with thicker MPN films have lower noise, which makes them more desirable for use as a sensor [11]. Since the spacing between IDEs is 200µm, each sensor could be coated with a distinct MPN films. These MPNs have an average Au core diameters ranging from 3.9-4.5nm and were synthesized using the method of Rowe et al [12].

C. Microfluidic Lid Implementation

A microfluidic gas flow chamber was implemented on the surface of the monolithic CR array chip, providing an interface to the micro column in µGC system. The first step in the packaging process is the mounting of the chip within a silicon “extension carrier” (EC) (Fig 4). This EC serves to secure the chip in an adjacent position to the input and output capillary tubes, and to provide a surface for the lid to be sealed over both the gas detection chip and the capillaries, creating a microfluidic chamber over the chemiresistor array.

The EC has been fabricated through deep reactive ion etching with thick photoresist as the masking material, achieving an etching depth equal to the thickness of the CR array chip. The first step of packaging assembly is to mount the chip within the EC’s inner cavity, which has a width 1.1 mm greater than the chip dimensions; this design increases the packaging’s tolerance for variation in chip size and layout. After this step, capillaries with an outer diameter of 380 µm are then secured in the EC’s trenches, which contain a tapered “stop” that reduce the trench width to 200µm, prohibiting the capillaries from contacting the chip. Once the chip and the capillaries are properly secured to the EC through the application of non-sorbent epoxy and the chip is wirebonded to a standard 40 pin DIP header, the assembly is then sealed with a lid containing a microfluidic channel.

The lid has a length of 3.8 mm which spans the distance between the input and output capillaries. Soda-lime glass was chosen as the material for the glass wafers to prevent sorption of the target analytes and to allow for easier alignment during the packaging assembly. The inner chamber of the lid has length of 2.2 mm and width of 600 µm. This soda-lime lid was wet etched with an amorphous silicon mask, creating microfluidic channel with a controlled surface roughness of less than 30 nm. The packaged microfluidic chamber is subsequently tested for leaks by passing helium through the channel and probing with a helium detector.

IV. RESULTS

The 8-channel CR array readout chip was fabricated in AMI 0.5µm CMOS process. Test results show it consumes 66µW per channel with a 3.3V supply and achieves 125ppm resolution over the resistance range from 60kΩ to 10MΩ, providing a 120dB dynamic range. Eight IDEs were fabricated on the surface of the chip. Four were coated with MPNs using thiolate ligands derived from 1-octanethiol (C8) and four from 1-mercapto-6-phenoxyhexane (OPH). Fig. 5 shows a photograph of CR instrumentation chip with on-CMOS MPN-CR array. The chip was then packaged and the microfluidic CR array was attached. Fig. 6 shows the final device in a DIP-40 carrier.

Fig. 4. Conceptual schematic of assembled microfluidic chamber.

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Fig. 5. Die photograph of 2.2×2.2mm CR-array readout chip with on-CMOS MPN-coated CR array.
A CMOS monolithic CR array with a microfluidic flow channel for μGC has been developed. The CR readout circuit contains eight readout channels and achieves 125ppm resolution over the resistance range from 60kΩ to 10MΩ for 120dB dynamic range. A 4x2 MPN-coated CR array was fabricated on the surface of the readout chip. A microfluidic lid was implemented on chip to interface the detector with a μGC sample flow network. Functionality of the monolithic detector was demonstrated by successfully measuring multiple analytes in a GC flow column. These results verify the feasibility of integrating the detector microsystem into a highly miniaturized low noise μGC platform.

REFERENCES


