Die-level Photolithography and Etchless Parylene Packaging Processes for on-CMOS Electrochemical Biosensors

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Abstract— **Integrated sensor arrays on CMOS instrumentation chips are attractive to many biological and biomedical sensor applications. However, the packaging of CMOS circuitry for use within a liquid environment remains as an open challenge. Reliable post-CMOS electrode fabrication and packaging processes that are critical to the development of integrated electrochemical biosensors are presented in this paper. A die-level photolithography process was developed that provides uniform coverage for accurate patterning over 87% of a 3×3mm^2 silicon substrate. In addition, a new process has been developed to package post-CMOS fabricated electrode arrays. This etchless parylene packaging reduces processing time and improves fabrication yield. These techniques enable realization of on-CMOS biosensors operating in liquids.**

I. INTRODUCTION

Miniaturized sensor arrays are capable of parallel analysis of multiple parameters. Because of the distinct advantages of microsystem platforms, there has been a trend to integrate sensor arrays onto the surface of silicon chips and perform measurements using on-chip CMOS electronics [1-3]. Such platforms provide a great opportunity to expand lab-on-chip solutions that replace bulky bench top sample analysis tools with simple, low power, portable instruments. The fabrication compatibility between many bio/chemical sensor interfaces and CMOS technology makes a CMOS instrumentation circuit an outstanding candidate for a silicon-based lab-on-chip solution [4]. However, there are challenges that must be overcome to realize the integration of sensor arrays and CMOS electronics, including electrode fabrication on a CMOS substrate and packaging chips for liquid environments. Although standard fabrication processes including photolithography work well on large-area wafers (~cm) [5-7], many post-CMOS fabrication applications require die-level processing with only millimeter-sized CMOS substrates.

Several approaches to permit the use of CMOS circuitry within liquid environments have been reported [8-13]. These methods utilize epoxy adhesives or PDMS to seal the electrical wires and to create microfluidic structures. However, the epoxy encapsulation has reliability issues due to poor adhesion to the chip substrate, stress imposed on wire bonds. Another approach involves the use of parylene as the encapsulation material [14]. However, the micromachining laser used to ablate parylene during patterning is hard to control and potentially damaging to the circuits and sensing region underneath; the ultrasonic bath used to lift-off the parylene could also compromise sealing around the wire bonds.

In this paper, the first known experimental characterization of millimeter-sized die level photolithography for post-CMOS fabrication is presented, and a new etchless parylene process that simplifies packaging is introduced. The new packaging process improves upon our prior work [15] by eliminating plasma etching of parylene to reduce processing time and improve fabrication yield. These processes were implemented on a CMOS electrochemical instrumentation chip, and the functionality of the underlying CMOS chip was proven to be unaffected by the post-CMOS processing. These techniques enable the integration of bio/chemical sensors and CMOS electronics where measurements are taken at the surface of the millimeter-sized CMOS chip.

II. CHALLENGES

A. Die level processing

When integrating sensors on CMOS electronics we inevitably encounter smaller size die. Compared with the wafer level process, few were reported on the die level process. For such small substrates, the edge bead effect, which describes a thick buildup of photoresist along the substrate edge, becomes a significant challenge to photolithography and greatly reduces the patternable, uniformly covered area. In post-CMOS fabrication, recessed contact pads on the peripheral cause even more severe edge bead effect. A better understanding of this phenomenon is needed to overcome the challenges to patterning small substrates.

B. Packaging

The packaging is needed to enable both the electronics and biointerface as functional, the packaging process should be compatible with their respective requirements. Operation of the CMOS biosensor array in an aqueous environment establishes a critical requirement to insulate all surfaces of the CMOS device in contact with the liquid. Also, the sensing area on the chip surface should be accessible to the liquid environment. A chip-in-package approach utilizing wirebonded die was adopted in our prior work [15], establishing a need for a protective insulating material capable of coating all surfaces of the 3D chip structure, including chip

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sidewalls and wirebonds. The insulating material should withstand cleaning procedure without contaminating sensing electrodes. Parylene was chosen as the insulation material because of its excellent bio-compatibility, chemical resistivity and isotropic coating property. Our previous reported experiment used soluble epoxy and parylene was etched by oxygen plasma etching that allowed on-chip cleaning and biosensor measurement. However, the process was complicated procedures and requires a specific epoxy and long time plasma etching. In this work, we use a method without using both soluble epoxy and oxygen plasma etching, which is called etchless parylene packaging process.

III. EXPERIMENTS

A. Die level processing

Silicon substrates of 1.5×1.5mm^2 and 3×3mm^2 were prepared as typical sizes of CMOS dies by dicing a silicon wafer. The centrifugal effect is the main factor to spread a thin layer of photoresist by spin coating and alleviate edge bead effect. The centrifugal force increases as spin radius and angular speed increase. Therefore, to investigate these factors a 3-inch supporting silicon wafer was used and spin-coated with Shipley 1813 photoresist. The silicon dies were placed on the wafer and bonded by baking the photoresist on a hotplate at 110°C for 1min.

To minimize process variations, all test dies were bonded to the same wafer and photolithography experiments were performed simultaneously. To ensure the supporting wafer was centered on the spinner, a tiny silicon chip was bonded to the backside of the silicon wafer as a centering guide. The setup is as shown in Fig. 1. The test dies were placed at radii of 0mm, 10mm, 20mm and 34mm, respectively, to investigate

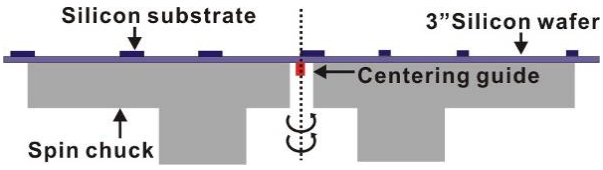

Fig. 1. Side view of the spin coating setup.

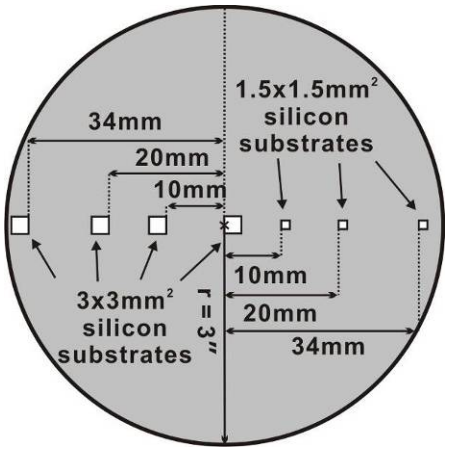

Fig. 2. The locations of 1.5×1.5mm^2 and 3×3mm^2 the silicon substrates with respect to the center on the 3 inch silicon wafer.

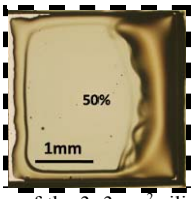

Fig. 3. Photoresist coverage of the 3×3mm^2 silicon substrate at 0mm from wafer center with large edge bead.

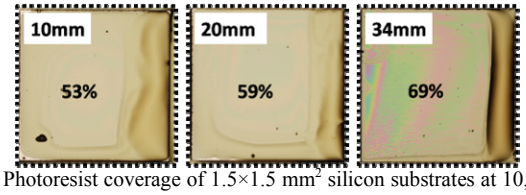

Fig. 4. Photoresist coverage of 1.5×1.5 mm^2 silicon substrates at 10, 20 and 34mm from the center with percentage of uniform area.

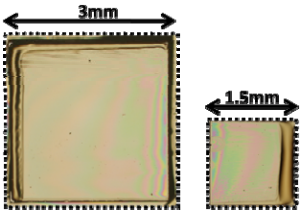

Fig. 5. Photoresist coverage of 3×3mm^2 and 1.5×1.5mm^2 silicon substrates at the same distance (34mm) from the center.

the effect of spinning radius as shown in Fig. 2. The side of the die was oriented orthogonal to the radius ensuring exactly same conditions. Shipley 1813 photoresist was then dispensed on each silicon substrate die and the supporting wafer was spun at 3000rpm followed by a 1min soft-bake at 110°C. Due to the photoresist edge bead effect, a significant edge buildup was observed for the substrate at 0mm. A commercial image analysis software was used to calculate approximate the area with a uniform coating and only about 50% of the surface was uniform as shown in Fig. 3. As the spinning radius increased, uniform coating was observed on a greater percentage of the die area as shown in Fig. 4. The area percentage improved from 53% at 10mm radius up to 69% at 34mm radius. By comparing the results between 1.5×1.5mm^2 and 3×3mm^2 substrates at the same spin radius, it was determined that larger perimeters provided better uniformity and less edge bead effect as expected which is shown in Fig. 5. The edge bead effect was worst on the trailing edge relative to the direction of rotation and slightly better on the interior edge than the exterior edge with respect to the center. The substrates were patterned using a photomask with an array of 20µm circles at 50µm pitch, and the best result was obtained from the 3×3mm^2 substrate at 34mm radius, as shown in Fig. 6. For this substrate, all shapes that were more than 130µm from the edge were properly patterned, and on two edges patterns could be formed up to the edge of the die, resulting in reliable patterning of 87% of the surface area. This experimental result was utilized to design and fabricate post-CMOS electrode arrays for biosensor applications.

B. *Etchless parylene packaging*

In our prior work [15], a special acetone soluble epoxy, Crystalbond 509 (SPI supplies) was used and parylene was etched by oxygen plasma. In this work, a new method was developed that eliminates parylene etching to simplify the process.

After fabrication of sensing electrode on a CMOS die, the die was wire bonded to a ceramic package (Fig. 7(a)). A smaller silicon chip made by dicing saw, 1.5mm×1.5mm in this experiment, which is big enough to cover the sensing area was coated with Shipley 1813 photoresist and flip-bonded over the electrode area (Fig. 7(b)). Besides bonding, the photoresist can also protect the electrode from the silicon chip. The packaged chip was then coated with a thin 2μm layer of parylene using PVD (PDS 2035CR, Specialty Coating Systems) (Fig. 7(c)). The parylene covers every surface of the package and the chip. The silicon chip was then taken off using a sharp tweezer and the photoresist was washed away by acetone and DI water. The photoresist was not baked so that the silicon chip could be easily pulled off but it is viscous enough to ensure bonding and sealing. The ~2μm thin parylene could be torn off without affecting surrounding coating. Now the packaging is ready as shown in Fig. 7(d).

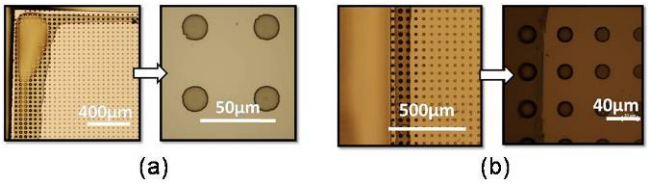

Fig. 6. 20μm diameter circle array with 50μm period photoreisist patterned on 3×3mm^2 substrates at 20mm (a), 34mm (b) from the center of the wafer.

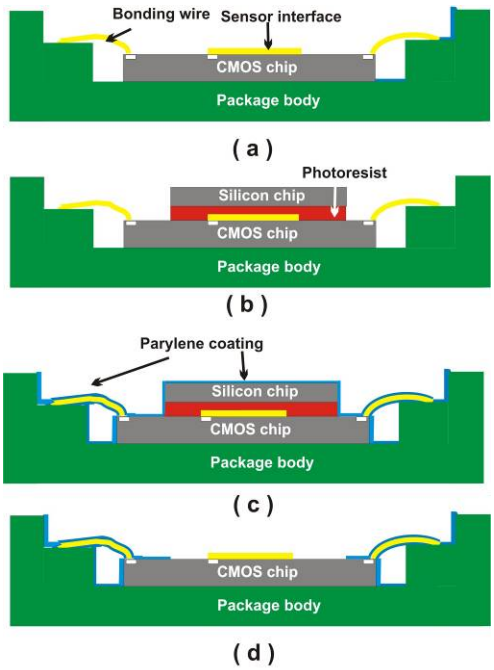

Fig. 7. Process flow of the packaging of chip without etching of parylene. (a) The CMOS chip with sensor interface fabricated on it was wire bonded to package. (b) 1.5×1.5mm^2 silicon chip was bonded over CMOS chip using photoresist. (c) 2μm parylene was deposited on the package and chip. (d) Silicon chip is taken off and photoreisist is rinsed off.

IV. RESULTS

A 3×3mm^2 CMOS impedance extraction chip [16] was designed and manufactured in 0.5μm process by MOSIS foundry. The bonding pads were designed at only 2 sides of the die. The electrode was formed by using the lift-off process. Negative photoresist was patterned followed by thermal evaporation of titanium/gold (50Å/1000Å). Then photoresist was rinsed off by acetone, methanol and DI water. During photolithography patterning, according to our die process experiment in section III.A, the chip was placed in a way so that the bonding pads are along the radial direction on the substrate thus the edge bead on bonding pads were minimized. This metallization step created routings between electrodes and surface contacts to CMOS electronics, and it covered all surface CMOS metal, including bondpads, to eliminate chemical reactions between the CMOS aluminum alloy and the alkali photoresist developer, which has been observed to contaminate the surface electrodes. The die-level electrode fabrication steps are illustrated in Fig. 8. Different electrode designs were fabricated for needs of different sensing scenarios as shown in Fig. 9.

After the electrode was fabricated the etchless parylene packaging was performed with the chip and the result is as shown in Fig. 10. In our prior work [15], firstly, the parylene removal was solely dependent on the oxygen plasma etch rate. The etch time could last longer and elevated chamber temperature could soften the epoxy Crystalbond 509, whose softening point was at 71°C, which needs cooling. Secondly,

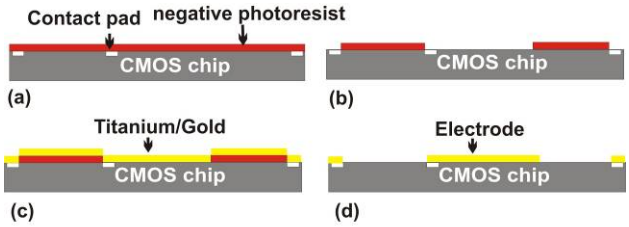

Fig. 8. Process flow for post-CMOS lift-off electrode fabrication: Negative photoresist is spin-coated (a) and developed (b). Titanium/gold is deposited by physical vapor deposition (c). Photoresist is then rinsed off to leave the electrode (d).

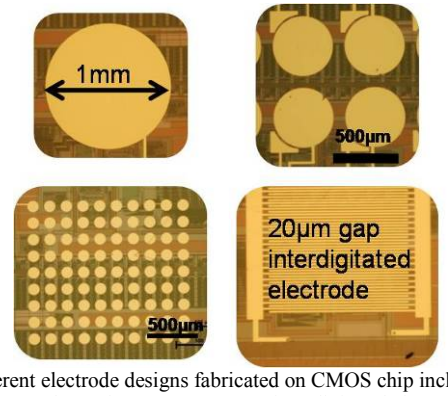

Fig. 9. Different electrode designs fabricated on CMOS chip including 10×10 100μm diameter electrode array, 20μm gap interdigitated electrode and electrodes for electrochemical measurements.

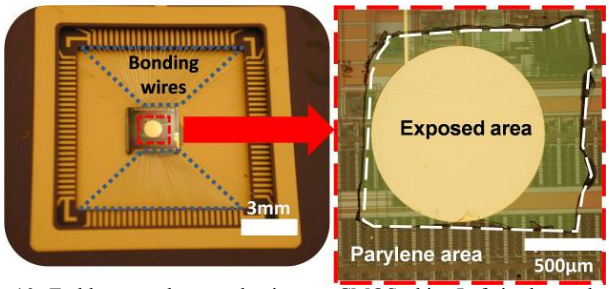

Fig. 10. Etchless parylene packaging on CMOS chip. Left is the packaged chip in 108 PGA package, and right is the close-up view of the electrode except which everywhere else is covered by parylene.

when the PDMS/silicon cylinder was pressed against the chip surface it could scratch the electrode surface. In this work, Crystalbond 509 was not involved. The adhesive photoreisist acts as a liquid cushion against the silicon chip. Because of these changes, this work was noticeably faster and simpler than previous work and thus improves the process yield.

The parylene coverage on the sidewall and corner coverage was also inspected. SEM images were taken for an identical sized silicon chip that was in the same parylene deposition process. One corner was intentionally removed to show the silicon chip beneath, as shown in Fig. 11. The images clearly showed that the parylene completely coated all the edges and corners.

To verify the post-CMOS processes did not affect performance of the underlying CMOS electronics, the CMOS impedance extraction chip was tested after processed with electrodes and packaging. The sigma-delta module of the chip was tested and it functioned as expected after the packaging process.

V. Conclusion

Millimeter-sized die level process has been characterized to investigate edge bead effect and find feasible fabrication area and optimum spin-coating condition. The result is used for post CMOS electrode fabrication. A new fabrication process of etchless parylene patterning has been developed for packaging that enabled simple and quick packaging. Functionality of CMOS electronics is not affected by the packaging process. These process techniques can be applied to a wide range of on-CMOS biosensor integration.

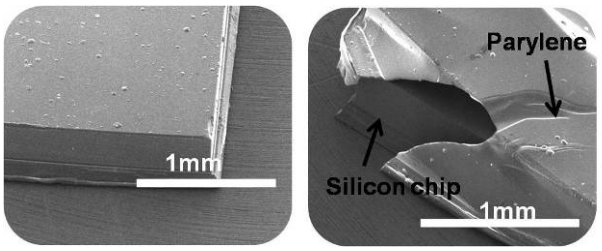

Fig. 11. SEM images of silicon chip coated by parylene. Parylene perfectly covers the silicon chip as shown in the image on the left. The image on the right shows the silicon beneath the parylene coating.

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