Low Cost MEMS Processing Techniques

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Abstract
This paper presents low cost techniques for the fabrication of microstructures using a limited set of equipment available in many university labs. The techniques developed can be used to process bare silicon wafers or to complete post-CMOS processing of fabricated integrated circuit die. Techniques for low cost mask generation have been investigated and implemented. These low cost masks have been used for all aspects of microfabrication, from photolithography to etching of MEMS structures. Die-level post-CMOS processing has also been conducted on chips fabricated at a foundry through the MOSIS service. On these chips, post-processing techniques have been performed to realize metallic electrodes on top of the integrated circuit chips as well as preparation steps for generating free standing thermally isolated microstructures utilizing low cost masking procedures.

CMOS Post-Fabrication Processing Steps
The engineering word is seeing a new trend with the combination of mechanical elements, transducers, and electronics on a common silicon wafer through microfabrication. This recent field is referred to as Microelectromechanical Systems or MEMS. However, most services that offer such capabilities are limited in their scope or can be quite expensive. In terms of saving money, any MEMS steps that can be performed “in-house” are always desired. This approach to fabricating MEMS is not a trivial option and there are downsides to this approach. Most academic cleanrooms do not have multi-metal/multi-poly fabrication capabilities, which limits the scope of the electronics that can be fabricated in these facilities. In addition to this, most cleanroom facilities at the university level are very limited in their ability to produce small feature-size electronics. Sub-micron feature sizes are basically not available unless an outside foundry service is used. This is an important point since most control and readout circuitry for MEMS devices are quite advanced and require large chip areas and without proper circuitry MEMS devices are useless. Another critical consideration is process compatibility. Many times a foundry service is used to produce the circuit chip and post-processing steps will be performed on these chips to realize MEMS structures. The post-processing steps required in most all cases are not trivial and careful design and post-processing procedure characterization are required to generate working MEMS microsystems. This paper focuses on MEMS post-processing techniques and methods for achieving acceptable results while keeping costs to a minimum.

Post CMOS Processing
Post CMOS processing consists of steps taken on silicon wafer or die after circuitry has been fabricated. Multiple procedures can be performed post CMOS such as photolithography, material etching, and material deposition. There are several key points that must be carefully
considered when performing these process steps to insure proper operation of the CMOS circuitry.

- The steps taken must be compatible with CMOS technology.
  - Low temperature
  - Prevent contamination
- The wafer must be well protected, i.e. protecting specific die areas and features from etching solution
- There must be consistency in the process steps

Traditionally in circuit design little consideration needs to be given to such issues as post-CMOS photolithography, but when designing MEMS systems this is a consideration that needs addressed when designing functionality for the system. Each step along the way, not only does the circuitry need to be properly designed and tested, but the MEMS portion of the design also needs very careful design planning, especially when the chip will be processed after fabrication to realize one working system on-chip. Photolithography, material etching, and material deposition have been implemented on fabricated wafers. Techniques for performing these steps and key issues for each are discussed [1].

**Photolithography**

Lithography is the most expensive, complex, and critical process in mainstream microelectronic fabrication. As mentioned, lithography is very expensive and accounts for upwards of one-third of the total fabrication cost. To put this into perspective a Pentium 4 processor has approximately 20 masks required, each with a cost of around 1 million dollars. In addition to mask cost, each of these masks needs to be carefully aligned to prior layers, which is a very complex and time consuming process with feature sizes that are around 0.15µm.

Figure 1 shows a simple system for optically exposing a wafer during processing procedures. Some type of an optical source is used to shine light through a mask. The image from the mask is then projected onto the wafer surface, which is then coated with some photosensitive material known as photoresist.

![Figure 1: Basic photolithographic setup.](image-url)
Mask aligners are the optical tools used to pass the image of a mask onto a silicon surface. There are several types of aligners used for microfabrication; however, the only one to be discussed is the contact aligner since that is the aligner used in many university level cleanrooms. The contact aligner is the simplest type of aligner. In contact alignment printing, the mask is pressed against the photoresist-coated wafer during exposure. The biggest advantage of these systems is the small features that can be generated using relatively inexpensive equipment. In a typical contact system, the mask is held image side down in a frame just below the microscope objectives of the system. Adjustment screws are used to move the wafer with respect to the mask for alignment purposes. Once the wafer is aligned to the mask, they are put into contact with each other, the microscope is retracted, and the wafer/mask is ready to be exposed to the light source. The wafer is then exposed to the high intensity light.

The mask used in the photolithographic process is a key component in the fabrication process. The mask is typically a glass plate that is transparent to ultraviolet light. Traditionally, the pattern of interest is generated on the glass by depositing a very thin layer of metal, usually chromium or gold. These masks produce very high quality images and are capable of micron/sub-micron features. However, these masks are quite expensive when trying to build microfabrication capabilities at the university level with each mask costing around $500 each. Table 1 shows typical mask options and cost when a contact aligner is the exposure tool of choice. There are several options available for low-cost photolithographic masks. Transparency masks through commercial printing services offer the lowest cost and quickest turnaround, usually the same day. The methods for producing several types of masks will be discussed.

<table>
<thead>
<tr>
<th>Mask Technology</th>
<th>Minimum Feature Size (Line Width)</th>
<th>Mask Cost</th>
</tr>
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<tbody>
<tr>
<td>Traditional Chromium or Gold</td>
<td>Sub-Micron</td>
<td>$500 per 4x4 inch mask for 1 µm feature size</td>
</tr>
<tr>
<td>Transparency Mask</td>
<td>25 µm</td>
<td>$15 per 10x12 inch transparency sheet</td>
</tr>
<tr>
<td>Microfiche</td>
<td>$1–5 µm</td>
<td>$20 per ten reductions</td>
</tr>
</tbody>
</table>

**Transparency Masks**

One option that is available for generating masks quickly and inexpensively is transparency mask technology. Transparency masks are sufficient when the features being generated are of 50+ micron size. Using a 3600 or better, photoreproduction quality laser or linotype printer, one can generate a transparency with geometries defined down to the tens of microns in resolution. This transparency is then taped to a piece of glass and can be used for photolithography. The process for developing these masks is very straightforward. The masks are designed using any drawing program that produces high resolution images. These files are then sent to a printing service; the file type required may vary with the printing service. Depending on the polarity of the mask, positive or negative, light can either pass through the patterned regions or pass through the regions outside of the pattern onto the photoresist. The printer used for this research was a high quality laser printer with 2500 dpi at Advanced Imaging, Inc. in Lansing, MI.
Masks generated from the printing service and their photolithographic results are shown in Figure 2. Patterns have been successfully transferred from these masks. It can be seen that for larger feature sizes the shapes on the mask are clear and well defined, but as their sizes are scaled down, the shapes become distorted and less distinct. For example, Figure 2, top left, should be a circle on the end of the line. In the final three dark field pictures it is difficult to see the desired patterns. This is due to shadows generated under the mask from the light source.

Figure 2: Transparency masks generated through commercial printing service. 
**Top:** Left: 80µm circular electrode pattern with 60µm line width. Right: Alignment marks with smallest feature an L-shaped 5µm line clearly not printed. 
**Center:** Left: Array of square and circular electrodes varying in size from 80µm to 120µm in size. Larger sizes show defined shapes and edges. Right: Two dark field 300µm x 300µm squares, results show poor definition of dark field patterns. 
**Bottom:** Left: 100µm diameter dark field pattered circles. Clear regions appear shaded due to shadows from light source. Right: 75µm diameter dark field pattered circles. Circular shape is much less defined and further investigation showed that 50µm circles could not be produced. 
*Note: Clear field masks yield more consistent results.*
Microfiche Masks

A newer idea that has been developed for low cost masking is the use of microfiche[2-4]. The attractiveness of microfiche for masking lies in the quality of the patterns that can be generated: There are some important points that must be considered. First of all, the regularity of patterns generated using microfiche should be much better that patterns of comparable size generated using a high resolution printer. The limit in feature size with microfiche masking must be determined. Most importantly, these patterns must be able to be transferred using photolithographic techniques.

The process of generating masks for microfiche fabrication is very similar to generating patterns for high resolution printing. The mask patterns can be designed using any drawing program that produces high resolution images, although resolution is not that critical since these images will be reduced by 25 to 42 times, depending on the reduction ratio for the micrographics service. Masks for microfiche were generated using a drawing program and then printed out on a HP LaserJet 2200DN printer. This printer is capable of 1200dpi resolution, which translates to a minimum feature size of around 100\( \mu \text{m} \). The smallest feature transferred the microfiche was around 5\( \mu \text{m} \), part of the alignment mark shown in Figure 3. This particular line was drawn with a width of 125\( \mu \text{m} \) since the reduction ratio was 25:1. The masks generated were negatives of the 8.5x11 inch originals. The quality of the mask shapes generated using this reduction technique are exceptional, especially when compared to results from the printing service with shapes of comparable size, as shown in Figure 4.

Figure 3: Microfiche mask patterns generated in 25:1 reduction onto film Top: Clear field and dark field alignment marks with 5\( \mu \text{m} \) L-shaped minimum feature size. Bottom: Circular electrode pattern with 15\( \mu \text{m} \) line size and circular electrodes with sizes 25\( \mu \text{m} \), 35\( \mu \text{m} \), and 45\( \mu \text{m} \).
Photoresist patterning was also performed from these masks to verify feature sizes that can be obtained with microfiche masks. All masks were successfully patterned with minimum feature sizes of around 10µm. These results agree with prior research. A 42x reduction service was not used, but results suggest that feature sizes could be further reduced using such a service. Patterns generated from microfiche masks are shown in Figure 5. The quality of these patterns is quite good. The masks were patterned by spinning on positive photoresist, S1813 Shipley, at 3000rpm for 30 seconds. The wafer was then soft baked at 80°C for 5 minutes. The mask was then exposed in a Karl Suss contact aligner for 30 seconds and then developed for 45 seconds. As seen in the pictures, it is somewhat clear that the pattern was slightly over developed. This problem is easily fixed by reducing photoresist development time.

Post-CMOS Compatible Film Deposition
In standard CMOS fabrication, film deposition is the procedure by which various layers of conductive and insulating materials are deposited onto the surface of a silicon wafer. There are two major types of deposition techniques, physical vapor deposition and chemical vapor deposition.

Physical vapor deposition is capable of depositing many materials onto a surface. The material to be deposited is placed in a chamber that is pumped down to vacuum, the material is then transformed into a gas phase by a variety of methods. In this fashion, atoms of the source
material are able to be transferred to the target. It is necessary for the molecular species of the source material to be in a gaseous phase and there are three standard techniques utilized to create this condition; evaporation, sputtering, and ion beam deposition. Physical vapor deposition is typically used to deposit most metals, insulators, and semiconductor films in standard IC processes.

One method for transforming the source material into the gas phase is to use evaporation techniques. The source material is heated so that it melts and then evaporates and there are three approaches, thermal evaporation and electron-beam evaporation, used to achieve this goal. Thermal evaporation is the easiest of the three and requires the most basic system. The material to be deposited is placed inside a crucible in a vacuum chamber and the crucible is then heated until the material evaporates. Heating of the crucible is accomplished in several fashions, but resistive and inductive heating techniques are the most common in practice. The temperature required to evaporate the material depends on the vapor pressure of the material and on the pressure. The downfall to this method of deposition is that few materials can be deposited in this fashion. Deposition is limited to metals such as Al, Au, and metals with higher vapor pressures.

Another common technique used to evaporate materials and the one of choice for this research is electron-beam evaporation. A high-energy electron beam is used to heat and melt the source material in e-beam evaporation. Higher temperatures can be achieved using this technique and because of this, a wider range of materials can be deposited. In addition to metals with lower vapor pressures, some insulators can be deposited. Also, since the crucible is not directly heated as much, the possibility of contamination through e-beam evaporation is lowered when compared to thermal evaporation. For these reasons, e-beam evaporation is commonplace in the IC industry today.

The third method of physical vapor deposition is sputtering. Basically sputtering consists of bombarding the source material with an ion beam. The ion beam is generated through an arc discharge in a pressure range of 1-100 µTorr, with voltages of 500-1000V. The ion beam is then formed into a narrow column, accelerated and then impinged upon the source. As the ions hit the source, the source atoms are knocked off and land on the substrate. Sputtering is the best of the three PVD methods for a few reasons. First, sputtering offers excellent cleanliness and control to the deposition process. Another key feature is the fact that both deposition of

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*Figure 5: Patterns generated in photoresist using microfiche masks. Features are quite well defined and minimum features of approximately 10µm were achieved.*
materials and etching can be performed at the same time. This is accomplished by focusing the ion beam on the wafer to achieve etching. Multiple ion beams can be used in this fashion to achieve deposition and etching. Sputtering is also very desirable due to the wide range of materials that are able to be deposited, insulators such as silicon oxide that in other cases must be thermally grown can be deposited.

A key feature of each PVD technique is the fact that the temperature of the source material in each is raised significantly, but the temperature of the substrate is typically maintained at or near room temperature. This is of particular importance when dealing with MEMS post-processing. The temperature of fabricated devices cannot be raised too much or the Al used in the fabrication process may melt.

The alternative to physical vapor deposition is chemical vapor deposition. Chemical vapor deposition is used to deposit thin films onto a substrate from a gas phase. Several types of chemical vapor deposition techniques are available; low pressure chemical vapor deposition, plasma-enhanced chemical vapor deposition, and photo chemical vapor deposition. Most all of these techniques raise the substrate temperature above 300°C, so these are performed at higher temperatures than the physical vapor deposition techniques already discussed and can cause problems especially in fabricated circuitry. Chemical vapor deposition techniques are mostly used for the deposition of insulators and semiconductor materials due to the conformal nature of the deposition. Due to temperature, complexity, and contamination issues that may arise due to CVD techniques, these techniques are not favorable for use in post-CMOS fabrication.

**Post-CMOS Compatible Etching Techniques**

The etching process in CMOS and MEMS fabrication consists of removing a selected material by adding a substance to the environment, usually a liquid or gas that will selectively attack a target material. When discussing etching it is useful to begin with a discussion of prime factors in the etching process. The main factor is the etch rate, which is defined as thickness etched over time. A high etch rate is usually desired in the manufacturing environment, but if the etch rate is too high, the process may be very difficult to control and reproduce. It is very common to have etch rates on the order of hundreds or thousands of angstroms per minute. Another important factor is the etch rate uniformity which is measured in percentage variation of the etch rate. This is often quoted across the wafer and from one wafer to another. Another very important etching factor, especially in MEMS design is the selectivity of the etchant. Selectivity is the ratio of the etch rates of various materials, such as a PR mask or an underlying layer, referenced to the film that is being patterned. In many cases photoresist is used as the making layer in CMOS fabrication so etchants must be selected that do not etch PR. In post CMOS processing careful planning must be implemented when generating a design for post-CMOS processing. One consideration must be given to substrate damage. For example, p-n junctions have been shown to degrade under certain types of etching. The amount of degradation depends not only on the etch process, but also on the depth and type of junction. Etchants must be chosen for post-CMOS processing that will not effect the active circuitry and this may prove difficult in certain scenarios.

The first consideration to be taken into account when choosing an etchant for post-processing is whether to use an isotropic or an anisotropic etchant. Some etchants are purely isotropic, which

means they will etch the target material at the same rate in all directions. Many times these etchants are avoided, if possible, since there can be considerable reduction in feature sizes, especially as layer thickness become larger. The other type of etchant, anisotropic, is often preferred since the exact pattern and dimension of the mask can be patterned onto the thin-film material. Often times, the masking layer is attacked by the etchant only at a greatly reduced rate. So for long etches, mask erosion and undercut may be a problem. Examples of these etching techniques are seen in Figure 6.

![Undercut](image)

Figure 6: Etching topologies: A. Isotropic etching, B. Anisotropic or directional etching, and C. Mask erosion and undercut.

The next major consideration is whether to choose a wet or dry etching process. Wet etching is a purely chemical process that, if not performed carefully, can have serious drawbacks: a lack of anisotropy, poor process control, and excessive contamination to the system. However, wet etching can be highly selective and often does not damage the substrate. As a result it continues to be used for a wide range of applications. A more complete overview of wet etching can be found elsewhere[5]. Wet etching is used to pattern a wide variety of materials. A table of common wet etchants and the materials they etch is found in Table 1.

<table>
<thead>
<tr>
<th>Material</th>
<th>Wet Etchant</th>
<th>Masking Material</th>
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<tbody>
<tr>
<td>SiO₂</td>
<td>Buffered Hydrofluoric Acid (BHF)</td>
<td>Photoresist</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td>Hot Phosphoric Acid</td>
<td>Silicon Dioxide</td>
</tr>
<tr>
<td>Al</td>
<td>Phosphoric + Acetic + Nitric Acid</td>
<td>Photoresist</td>
</tr>
<tr>
<td>Cr</td>
<td>Hydrochloric Acid (HCl)</td>
<td>Photoresist</td>
</tr>
<tr>
<td>Au</td>
<td>Potassium Iodine (KI)</td>
<td>Photoresist</td>
</tr>
<tr>
<td>Si (Isotropic)</td>
<td>HF + HNO₃ + Acetic (1:3:8)</td>
<td>Silicon Dioxide or Silicon Nitride</td>
</tr>
<tr>
<td>Si (Anisotropic)</td>
<td>KOH, TMAH, EDP</td>
<td>Silicon Dioxide or Silicon Nitride</td>
</tr>
</tbody>
</table>

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Isotropic etching is sufficient for many applications, but some technologies including MEMS require directional specific etching to realize structures. Many times the bulk silicon is etched away from patterned areas to create such structures. Common anisotropic wet etchants for silicon etch the (100) and (110) directions much faster than the (111) directions and the specific etch rates have been reported [6-12]. This type of etching is widely used when creating MEMS structures post-CMOS, especially when electronics on-chip are located near structural elements to prevent device contamination and malfunction. Isotropic etchants and the issues involved with post-CMOS processing on MOSIS die will be discussed in further detail later in the next section.

**MOSIS Post-CMOS Processing**

As previously mentioned the fabrication of circuitry for control of a MEMS system is usually always performed by a fabrication service. In this research the MOSIS service is used for the base fabrication of the MEMS system. MOSIS is a low-cost prototyping and small-volume production service for VLSI circuit development. Since 1981, MOSIS has fabricated more than 50,000 circuit designs for commercial firms, government agencies, and research and educational institutions around the world [13].

The process being used is AMI Semiconductor’s (AMIS) C5F/N 0.5 micron process. This is a non-silicided CMOS process with 3 available metal layers and 2 poly layers, and a high resistance layer. Stacked contacts are supported. The process is for 5 volt applications. PiP (poly2 over poly) capacitors (950 aF/µm²) are available but not used for this research. This is a planarized process which does add some degree of difficulty into the design and post-fabrication processing which will be discussed. In addition to this issue, the circuit die to be fabricated are 3mm x 3mm x 500µm which poses several problems. These and other issues will be discussed as the processing techniques already discussed are applied to the MOSIS die. Trial experiments were performed on 2.2mm x 2.2mm x 500µm die to gain some insight into the post-processing steps on MOSIS die and to workout some critical issues involved with these steps.

**Photolithography**

As previously mentioned lithography is the most expensive, complex, and critical process in mainstream microelectronic fabrication. When applying this technique these issues become apparent. The very first step to be performed on MOSIS die will be photolithography. The post-processing flow will consist of deposition of biosensor electrodes and then etching procedures to generate thermally isolated regions.

The first photolithography step that must be performed on the die is the spinning of PR. Normally on the wafer level when the PR is being spun across a large uniform surface such as a full wafer, uniformity of the PR layer across the wafer is not an issue. When dealing with individual MOSIS die, however, uniformity of the PR layer on the die surface is a crucial requirement. In the first experiments a die was attached to the surface of a wafer and patterning of PR was attempted. The wafer was placed on the spinner and PR was spun on and after the necessary steps, patterning in the mask aligner was attempted. Initial patterning yielded poor results and after investigation it was found that the PR layer was not uniform across the surface of the die. Due to the viscosity and surface tension of the liquid PR at the corners of the die caused by the height of the die above the wafer, the PR was thicker at the four corners. As
mentioned, patterning of the PR was inconsistent and results were poor. This issue needed to be resolved in order to ensure repeatability and consistency to the post-processing procedure. There are a couple of solutions to this problem. One solution is to use a spray-on type PR layer. This technique was not chosen because the chemicals required can be quite expensive when compared to conventional photoresists and it would require learning and characterizing a new process. Another option that was selected is to design a die holder for post-processing steps that leaves the die surface level with the holder during the spinning process. Preliminary experiments were conducted using die a die storage container, which is typically provided by the CMOS foundry service (e.g., MOSIS) but can also be purchased commercially. The die storage container, shown in Figure 7a, was sanded down to make the height of the container walls even with the die surface. This approach yielded much better uniformity across the die and the PR could be effectively patterned with adequate consistency. Patterns generated using this technique for metal deposition and lift-off processes are presented in the next section. For even better uniformity, a substrate (glass slide, Si wafer, Teflon block, etc.) machined with recesses to hold individual die while maintaining a planar surface for PR application is currently being explored.

Figure 7: Die holder used for uniform PR application (a) conventional die storage container, and (b) cross-section of a custom machined die holder.

Metal Deposition
Post-CMOS deposition of metallic or insulating layers processing is needed for many MEMS structures or other microsystem applications, including formation of electrochemical electrodes. Electron beam evaporation was used to deposit various metal layers to verify that materials could be patterned onto MOSIS die using standard IC process steps. This technique was selected because it is very reproducible and does not produce thermal complications since the die is held near room temperature. The system used is very precise and identical results can be achieved from one sample to the next. As shown in Figure 8, metal layers have been deposited on the top of a MOSIS die. The patterns were successfully transferred to the die surface, but there were some inconsistencies in the transferred pattern for smaller features with rectangular shapes. The results improve with better PR uniformity provided by using the die holders as discussed above.

Etching
The final step in processing the MOSIS die was to perform etching steps to generate thermally isolated structures for the temperature control. There are two possibilities for generating thermal isolation regions on a MOSIS die. The first is a backside etching technique, shown in Figure 9, which seems attractive because of the relative simplicity of this process. However, this is not the most desirable technique when electronics are on the chip. Often with backside etching, the etch is allowed to proceed for a long period of time until the etch stops on some layer, usually an
insulator. This is problematic for an integrated circuit chip, since the etch would dissolve the necessary doped layers for transistor operation. Thus, a simple one step anisotropic etch would not work. In order for backside etching to work, a two step etch procedure would be required. The first etch would be a one region, timed bulk etch that would not require careful alignment and would need to be stopped at some depth below the surface where electronics would not be affected. The second etch would be consist of separate anisotropic etch regions that would need to be masked by some layer that is not affected by the etchant and then aligned to features on the frontside to create appropriate thin film regions. This is a complex procedure that would be very difficult to duplicate without expensive equipment.

![Figure 8: Chromium patterns (glossy donut-shape) generated on MOSIS die using a post-CMOS lift-off technique.](image)

The second option is to use a frontside processing procedure utilizing process layers as the appropriate masking and sacrificial layers to realize a thermally isolated structure. Ideally the CMOS process layers could be designed to leave an opening to the silicon surface after fabrication steps. Normally this would consist of drawing layers of Active, Contact, Via, Via2, and Overglass. These layers generate the appropriate openings in passivation layers between the silicon surface and the top of the chip in a 2-metal CMOS process. For a CMOS process with

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larger feature sizes, such as the Orbit 2.0 micron N-well process, a stack of these drawn layers would provide an opening to the silicon surface. However, more advanced near- and sub-micro processes require planarization steps to facilitate alignment and formation of small device features. Because of the nature of a planarized process and related design rule restrictions, direct openings to the silicon substrate can not be obtained from the foundry. Oversized contacts or vias result in materials being deposited into these open region. Figure 10 shows a structure designed to expose the silicon substrate through a stack of insulator openings. However, when fabricated in a planarized process, residual materials remain inside the passivation openings blocking the path to the substrate and making frontside etching impossible. This material can be etched away, but it is difficult to mask the rest of the die to protect against the harsh chemicals used to perform such an etch.

Figure 10: Microstructure design with residual materials left in designed openings to silicon substrate. Residuals result from a planarized process.

To overcome the problems associated with post-CMOS frontside etches in a planarized process, it is necessary to design the layouts for the deposited insulation and metal layers in such a way that they do not violate design rules yet still allow wide openings to the silicon substrate to be formed. In ongoing research, a method has been devise to pattern the insulator/metal layer stack in such a way that it can be completely removed by post-CMOS etching with a single masking step. In this approach, the insulators become sacrificial layers present only to maintain compatibility with the planarized process. Results of this approach will be reported once the methods have been validated experimentally and characterized.

Conclusion
Post-CMOS MEMS processing utilizes many of the same techniques as standard IC fabrication. Several low-cost techniques for performing die-level post-CMOS processing steps with limited equipment available in many university labs have been developed and discussed. Microfiche masks were identified as a economical method to obtain feature sizes on the order of a micron. Techniques for performing photolithography on individual pre-processed die have been presented. Post-CMOS deposition and etching procedure have been discussed, including identification of critical constraints in submicron planarized processes. Successful post-CMOS fabrication requires both careful design of the CMOS layout layers as well as proper application of masking, deposition, and etching steps which can be preformed on individual circuit die.
References


