

Kaushal R. Gandhi

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OBJECTIVE A full-time position in the field of computer engineering with special interests in low-power microarchitecture, reliable circuit design, and circuit-parameter modeling.

EDUCATION *Bachelor of Technology*, Electrical Engineering
Indian Institute of Technology, Madras, India July, 2001
Master of Science, Computer Science and Engineering
State University of New York (S.U.N.Y) at Buffalo, NY September, 2003
Ph.D., Electrical and Computer Engineering
Michigan State University, East Lansing, MI, Expected: December, 2006

PUBLICATIONS *Journal Papers*

1. *K.R. Gandhi* and N.R. Mahapatra, "Improving energy efficiency in integer datapath circuits via operand encoding and operation bypass," (under preparation for submission to ACM TACO)
2. *K.R. Gandhi* and N.R. Mahapatra, "Fast circuit-level energy modeling for accurately evaluating value-based, low-power microarchitectural design techniques," (under preparation for submission to IEEE Computer Architecture Letters)

Conference and Workshop Papers

1. *K.R. Gandhi* and N.R. Mahapatra, "Value-aware operation bypass in functional units for simultaneous energy and soft-error minimization," (under review)
2. *K.R. Gandhi* and N.R. Mahapatra, "Exploiting data-dependent slack using dynamic multi-VDD to minimize energy consumption in datapath circuits," Proc. 9th Design, Automation and Test in Europe Conference (DATE 2006), Munich, Germany, Mar. 6-10, 2006.
3. *K.R. Gandhi* and N.R. Mahapatra, "Dynamically exploiting frequent operand values for energy efficiency in integer functional units," Proc. 18th International Conference on VLSI Design (VLSID 2005), pp. 570-575, Kolkata, India, Jan. 3-7, 2005.
4. *K.R. Gandhi* and N.R. Mahapatra, "A study of hardware techniques that dynamically exploit frequent operands to reduce power consumption in integer function units," Proc. 21st IEEE International Conference on Computer Design (ICCD 2003), pp. 426-428, San Jose, CA, Oct. 13-15, 2003.
5. *K.R. Gandhi* and N.R. Mahapatra, "A detailed study of hardware techniques that dynamically exploit frequent operands to reduce power consumption in integer function units," Proc. Second Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD 2003), held in conjunction with 30th International Symposium on Computer Architecture (ISCA 2003), pp. 76-84, San Diego, CA, Jun. 8, 2003.

COMPUTER SKILLS *Languages & Software:* C, C++, Perl, Verilog, VHDL, Assembly language (MIPS, x86, SPARC), VLSI-CAD (Cadence Virtuoso, Spectre, Verilog-XL, OCEAN scripting), ModelSim, Matlab, Dreamweaver, CSS, HTML, SimpleScalar, SHADE, and ILOG CPLEX.
Operating Systems: Solaris, Unix/Linux, Windows.

PROFESSIONAL EXPERIENCE *Teaching Assistant* Fall 2005, Spring 2006
Computing Concepts and Competencies, Dept. of Computer Science and Engineering, Michigan State University, East Lansing MI. Taught concepts related to word processing, spread sheets, databases, and web design.
Teaching Assistant Spring 2005
Electronic Design Automation (Senior-level), Dept. of Electrical and Computer Engineering, Michigan State University, East Lansing MI. Taught the laboratory component

of the course; VHDL programming and implementation of hardware designs on Xilinx Spartan 2/3 FPGA boards.

Teaching Assistant

Spring 2005

Advanced VLSI Design (Graduate-level), Dept. of Electrical and Computer Engineering, Michigan State University, East Lansing MI. Designed two projects for the course; (1) Sizing inverters in an inverter chain to optimize delay and power and (2) Implementing operand value exploitation in a 32-bit ripple carry adder to reduce dynamic energy consumption.

Research Assistant

Spring 2002–Fall 2004

Dept. of Computer Science and Engineering, S.U.N.Y, Buffalo, NY; Dept. of Electrical and Computer Engineering, MSU, East Lansing, MI.

- Exploiting data-dependent slack in arithmetic circuits.
- Dynamically exploiting operand values for low-power datapath circuits.
- Input aware energy modeling for arithmetic units.
- Soft error modeling for combinational circuits.
- Hardware and software countermeasures against differential power analysis attacks.
- Reuse cache to implement operation bypass in microprocessors

PROJECT EXPERIENCE

Computer Architecture

- Performance comparison between Traditional SMT and Mini-threaded SMT
- Estimating data-dependent slack in the execute stage of an out-of-order superscalar processor
- An analysis of the potential for data type encoding based on frequency and bit-width characteristics

VLSI Design

- Full custom implementation of low-power integer arithmetic units using Cadence design tools to exploit operand values
- Optimal partitioning of arithmetic units to maximize energy savings through operation bypass
- Design of arithmetic units that dynamically switch between multiple supply voltages to exploit data-dependent slack

Design Automation

- An input aware energy model for integer arithmetic circuits
- Soft error modeling for combinational logic circuits

Computer Security

- Obfuscating power signatures of combinational circuits to prevent DPA attacks
- Software countermeasures to hide data flow and control flow characteristics

PROFESSIONAL MEMBERSHIP AND SERVICE

- Student member of IEEE and ACM since 2002.
- Member of ACM-SIGARCH and ACM-SIGDA.
- Reviewer for ACM/IEEE Design Automation Conference (DAC).
- Secondary reviewer for Intl. Conf. on Dependable Systems and Networks (DSN), Intl. Conf. on Computer Design (ICCD), IEEE Intl. SoC Conference (SOCC), Intl. Conf. on VLSI Design, and Great Lakes Sym. on VLSI (GLSVLSI).

HONORS AND AWARDS

- Selected to present a poster on Ph.D. research at the EDAA Ph.D. forum held in conjunction with DATE 2006.
- MSU Graduate School Research Enhancement Award, Fall 2004.
- Nominated as vice president of MSU India Club, 2004-05.
- ACM-SIGARCH Fellowship to attend the 30th International Symposium on Computer Architecture (ISCA-30) in San Diego, CA, May 2003.
- Central Board of Secondary Education Notional Prizes and Certificates for being in the top 0.1% in Science in the All India Secondary School Examination, 1995.

REFERENCES Available upon request