Buck-Boost DC-AC Converters Suitable for Renewable Applications

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Abstract – The operational limitations of the voltage and current transfer ratios are inherent to conventional current source converters (CSCs) and voltage source inverters (VSCs), which prompts the multiple-stage power conversion solution for applications that demand a wide voltage or current transfer ratio. In response to the undesired characteristics of the multiple-stage solution, such as augmented component count and the resulting higher cost and reduced reliability and efficiency, Z-source converters (ZSCs) have been proposed as a viable single-stage solution alternative to the solution of cascading multiple converters in series. In spite of the wide operating range featured by ZSCs, a fourth-order symmetrical lattice network constituting the DC link of existing ZSCs introduces additional design complexities, which hinders a broad adoption of the Z-source converter. This paper presents a unified framework for topological development of a family of power converters that are capable of operating over an expanded operating range that is comparable to the existing Z-source inverters. With a notable difference, the resultant topologies contrast existing ZSCs with significantly reduced complexity, in particular, the considerably reduced order of passive components. The reduced complexity renders the proposed topologies most suitable for applications that demand high efficiency, reliability and cost effectiveness. Renewable energy is one of the specifically targeted application areas.

Index Words: dynamic stiffness, pulse width modulation, static stiffness, Z-source converter

I. INTRODUCTION

For modern switching-mode power conversion processes that involve alternate current (ac), the predominant converter topologies, namely voltage source converters (VSCs) and current source converters (CSCs), have been adopted to a broad spectrum of applications, such as electric drives in industrial processes and Flexible AC Transmission System (FACTS) devices in power systems. As illustrated by Fig. 1a, a typical three-phase VSC topology consists of a six-switch bridge and a capacitor across the dc link rails and three inductors in series with the switching phase-leg poles on the ac side. Being a dual to the VSC topology, a typical CSC topology, as illustrated in Fig. 1b, consists of a six-switch bridge, a smoothing dc-link inductor, and three filter capacitors across the ac terminals. The converters in Fig. 1 can be utilized as inverters or rectifiers depending on the direction of power flow being from dc to ac or from ac to dc.

The understanding of both VSC and CSC has been well established. With pulse width modulation (PWM) of the switching bridge, the output magnitude of the fundamental component of the line-line voltage of the VSC will be unable to exceed the voltage across the dc link capacitor. In a dual manner, the fundamental component of the output line current of the CSC will be limited to the magnitude of the dc link inductor current. The limited voltage transfer ratio and current transfer ratio that are inherently associated with VSCs and CSCs have become a technical barrier in certain circumstances, where a wide operating range is needed. For instance, in renewable energy applications, the intermittency of renewable sources results in the fluctuation of converted electric energy output and accordingly the variation of the output voltage and/or current at the terminals of energy conversion devices, such as photovoltaic cells and electric generators for solar and wind applications, respectively. On the other hand, the voltage of power grids that the converted energy is fed to remains a relatively constant magnitude under normal operating conditions. As a result, a power converter capable of operating over a wide voltage/current transfer ratio is highly desired to maximize the captured energy and accordingly to reduce effect energy cost and to shorten the payback period for the investment in the generation assets.

In order to achieve expanded of voltage and current transfer ratios that are unavailable to conventional current source CSCs and VSCs, Z-source converters (ZSCs) have been proposed as a viable solution [1-3] alternative to the multiple-stage solution of cascading multiple converters in series. The ZSC topology features a dc link consisting of a symmetrical lattice network, i.e. two inductors and two capacitors as illustrated within the dotted box in Fig. 2. This lattice network was primarily studied in the field of filter design to synthesize specified network transfer functions [4-6]. In the context of power conversion, the fourth-order symmetric lattice network constituting the DC link of existing Z-source inverters introduces undesired complexities, which not only result in high component-count, but also exert extra burden in modeling the system and designing suitable control, as evidenced by the analyses attempted in [7, 8]. Hence, a broad adoption of the ZSC in practical applications has been hindered. Hence, the topologies that are capable of achieving the performance comparable to ZSCs’ without invoking extra complexities are technically appealing.
complexity renders the proposed topology best suitable for applications that demand high efficiency, reliability and cost effectiveness. Renewable energy is one of the targeted application areas.

This paper is organized as follows. The concept network stiffness, namely static stiffness and dynamic stiffness, is laid out in Section II as the theoretical foundation for the topology development. Section III presents the operating principle of the one of the derived topologies in the application context of dc/ac inverter. A carrier-based PWM modulation strategy is explained in Section IV. Section V presents detailed numerical simulation results that verify the theoretical analysis followed by the conclusions in Section VI.

II. TOPOLOGICAL PREMISE – DYNAMIC STIFFNESS

In general, a power converter is a set of interconnected components consisting of power switches and passive components, namely capacitors and inductors. The component set can be further divided into two subsets: one subset for power switches and the other subset for passive components only. For the sake of topological synthesis, it suffices to neglect the second order effects of the passive components and assume the subset of passive components to be time-invariant. On the other hand, the subset of power switches is time varying due to the turn-on and turn-off of the switches. The operation of the power switches is subject to the fundamental Kirchhoff’s voltage law (KVL) and Kirchhoff’s current law (KCL) that the underlying electric network needs to satisfy at any instant of time. This requirement can be examined primarily at the boundary between the subset of passive components and the subset of power switches, which will be explained with reference to the conventional VSCs and CSCs.

The operation of conventional VSCs and CSCs has been well established. Here, their operating principles are revisited with a focus on illustrating the interaction between the passive components and the power switches. In addition, this discussion will provide completeness for further discussion of their topological difference from ZSCs. The operation of the bridge of power switches in VSCs (Fig. 1a) is simultaneously determined by the boundary between the bridge and the dc link capacitor and by the boundary between the bridge and the ac inductors. The dc link capacitor excludes the switching states when both the upper and the lower devices in the same phase-leg are turned on, which leads to the violation of the KCL. The ac inductors exclude the switching states when both the upper and the lower devices are turned off, which results in the violation of KCL under the assumption of continuous conduction of the ac inductor currents. A simultaneous satisfaction of both boundary conditions implies a bridge represented by three single-pole-double-throw (SPDT) switches, as illustrated in Fig. 3a. A similar analysis can be carried out for the CSC in Fig. 1b. As a result, the bridge in CSC is represented by two single-pole-triple-throw (SPTT) switches such that the boundary conditions are constantly satisfied in the sense of avoiding violation of KCL and KVL.

This paper first revisited the topological theory that underlies ZSCs and brings about the concept of dynamic stiffness that characterizes the fundamental difference lying between ZSCs and conventional VSCs and CSCs. The newly proposed concept of dynamic stiffness provides a unified framework for developing a family of topologies that feature expanded operating range in terms of voltage and current transfer ratios. The derived converter topologies offer a buck-boost capability comparable to Z-source inverters, but with a significantly reduced complexity of the dc link design in relation to the existing Z-source inverters. The reduced
For simplicity of further discussion, the notion of voltage stiffness and current stiffness at the boundary of interest are introduced. A network is said to be voltage-stiff between two nodes if the voltage between these two nodes has to be continuous. In other words, a short circuit of two voltage-stiff nodes will result in a violation of KVL. As a dual, a network is said to be current-stiff for a branch if the current through the branch has to be continuous. An open-circuit of a current-stiff branch will lead to violation of KCL. For both cases of VSC and CSC, it is worth noting that the stiffness property, either voltage stiff or current stiff, at the boundaries does not depend on any switching state of the power switches and stays the same over time. Hence, static stiffness is held at the boundaries, which contrasts the case of the ZSC.

For the ZSC topology illustrated in Fig. 2, the property of the current-stiffness of the ac inductors requires at least one switch in each phase-leg be turned on at any instant of time, which is similar to the case of VSC in Fig. 1a. However, unlike VSC, the stiffness property of the lattice network at the boundary between the dc link and switching bridge will depend on the switching state of the diode to the left of the lattice network. Without degradation of operating the diode as a switching device, i.e. continuous-on or continuous-off, it is necessary to assume that the diode is connected to a voltage-stiff network. Without loss of generality, a voltage source is assumed to be in series with the diode for the following discussion.

When the diode is on, the conduction path that consists of two capacitors and the voltage source results in the voltage-stiff property at the boundary adjacent to the switching bridge, which is illustrated in Fig. 4a. When the diode is off, the two parallel current conduction paths, each of which consists of series connection of an inductor and a capacitor of the lattice network, result in the current-stiff property since an open-circuit of the branch connecting the lattice network with the switching bridge will lead to violation of KCL. Due to the dependence of the stiffness of the network on the time-varying switching-state of the diode, a dynamic stiffness best characterizes the boundary conditions of a ZSC, which set ZSC topology distinguished from VSC or CSC topology that rather features static stiffness. In addition, the dynamic stiffness property of ZSC leaves the graphical representation of the operational constraints as Fig. 3 for VSC and CSC a challenging task.

With the intention of simplifying the passive components while preserving the property of dynamic stiffness of the existing ZSC, a passive network may be constructed to be of lower order compared against the existing ZSC’s forth-order lattice network. As a minimized-complexity case, a first-order passive network is considered. As illustrated by Fig. 5a, a passive network consisting of single inductor can be used to replace the lattice network of ZSC. An ideal single-pole-single-throw (SPST) switch replaces the diode in ZSC to capture the topological essence in general. The semiconductor realization of the SPST will depend on the voltage/current constraints given a specific application, as will be illustrated by the inverter and rectifier examples. Fig. 5b
illustrates the voltage stiffness property when the switch is on while Fig. 5c illustrates the current-stiffness property when the switch is off. As a dual to Fig. 5a, a first-order passive network consisting of a single capacitor is illustrated in Fig. 6a. The voltage stiffness due to the capacitor can be achieved when the switch is on as shown in Fig. 6b. The current stiffness due to the current source is obtained when the switch is off as illustrated in Fig. 6c.

The concept of dynamic stiffness can be applied to passive networks of higher-order although the augmentation of the circuit order needs to be further justified in the context of a design space. As examples, two second-order passive networks, namely LC and CL networks, are illustrated in Fig. 7a and Fig. 7b, respectively. Without the illustration of the schematics, a third order LCL network or CLC network are readily derived following a similar manner.

A dc/ac power converter topology is constructed utilizing the first order network in Fig. 5. The resulting topology that features static voltage stiffness across ac terminals is illustrated in Fig. 8. Although current stiffness at the ac terminals appears to be feasible, a further examination of the dc link-inductor’s flux balance reveals the infeasibility of the topology if three ac inductors were utilized in place of the ac capacitors illustrated in Fig. 8. Hence, the topology with current stiffness property on the ac side will not be further pursued. If the single-capacitor network in Fig. 6a is utilized to synthesize the dc/ac converter, the feasible topology is illustrated in Fig. 9 with consideration of charge balance of the dc link capacitor.
The topologies shown in Fig. 8 and Fig. 9 can be alternatively derived from the dc/dc converter topologies of buck-boost and cuk converter as recently suggested by Loh in [9]. The synthesis of the dc/ac power converter topologies utilizing the second-order passive networks in Fig. 7 can be carried out in a straightforward manner. Since the stiffness property of the network in Fig. 7a is identical to the single-capacitor network in Fig. 6a, it follows that three-phase ac inductors on the ac side of the switching bridge are required to synthesize the dc/ac converter. In a similar manner, the a dc/ac converter utilizing the second-order CL network in Fig. 7b requires the voltage stiff capacitors on the ac side of the switching bridge.

Since the topologies illustrated in Fig. 8 and Fig. 9 are represented by ideal switches, a semiconductor realization is necessary for practical implementation. For demonstration purpose, only the topology in with single dc link inductor in Fig. 8 is realized with semiconductor switches for both inverter and rectifier applications. As shown in Fig. 10, the semiconductor-realized topology is utilized as an inverter that converts the dc voltage to three-phase ac and is then connected to the utility grid represented by the three-phase voltage sources through an LC filter. Fig. 11 shows the semiconductor realization of same topology for a rectifier application. The current polarity of the dc link inductor and the voltage polarity of the load voltage are indicated in the figure. The operating principle of the grid-connected inverter will be further detailed in the subsequent section.

![Fig. 10 Semiconductor realization of the proposed topology as a dc/ac inverter.](image)

![Fig. 11 Semiconductor realization of the proposed topology as an ac/dc rectifier.](image)

### III. OPERATING PRINCIPLE OF DC/AC INVERTER

The operation of the proposed converter is illustrated with the example of the grid-connected inverter as shown in Fig. 10. The operating principle of the inverter will be explained with reference to the two different intervals corresponding to the on-off states of the dc link switch $S_{dc}$ within a switching period. Fig. 12a and Fig. 12b illustrate the conduction path of load current when $S_{dc}$ is on and when $S_{dc}$ is off, respectively.

![Fig. 12 Conduction path of load current when (a) $S_{dc}$ is on; (b) $S_{dc}$ is off.](image)

#### A. When the switch $S_{dc}$ is on

As illustrated in Fig. 12a, when $S_{dc}$ is on for an interval of $d_{dc}T_s$ with $d_{dc}$ being the duty ratio and $T_s$ being the switching period, the dc link voltage source $V_{dc}$ charges the dc link inductor. In order to avoid the formation of a loop consisting of only of voltage source and capacitors, either one of the switch sets of \{sap, sbp, scp\} and \{san, sbn, san\} has to stay off. The incremental change of flux linkage of the dc link inductor during the interval when $S_{dc}$ is on can be expressed as

$$\Delta \lambda_{S_{dc} \text{ on}} = d_{dc}T_sV_{dc}$$  \hspace{1cm} (1)

#### B. When the switch $S_{dc}$ is off

As illustrated in Fig. 12b, when $S_{dc}$ is off for an interval of $(1-d_{dc})T_s$, the dc link voltage source is isolated. The dc link inductor and the bridge forms a topology that is identical to a conventional CSC. Based on the operating principle of CSC, the constraint of allowing a conduction path for the dc link...
current without shorting the voltages on the ac side has to be satisfied. Consequently, one and only one switch from each of the two sets of \( \{S_{ap}, S_{bp}, S_{cp}\} \) and \( \{S_{an}, S_{bn}, S_{cn}\} \) stays on during the interval when \( S_{dc} \) is off.

Let the voltages across the ac filter capacitors be

\[
\begin{align*}
    v_a &= V_m \cos(\omega t) \\
    v_b &= V_m \cos(\omega t - 2\pi / 3) \\
    v_c &= V_m \cos(\omega t + 2\pi / 3)
\end{align*}
\]

The modulation functions for phase-legs a, b, and c are further assumed to be

\[
\begin{align*}
    m_a &= MI \cos(\omega t + \phi) \\
    m_b &= MI \cos(\omega t + \phi - 2\pi / 3) \\
    m_c &= MI \cos(\omega t + \phi + 2\pi / 3)
\end{align*}
\]

where \( MI \) is the modulation index.

The incremental change of flux linkage of the dc link inductor due to the chopped voltages \( v_a, v_b, \) and \( v_c \) during the interval when \( S_{dc} \) is off can be expressed as

\[
\Delta \lambda_{Sdc_{-off}} = T_s (m_a v_a + m_b v_b + m_c v_c)
\]

Under the assumption of steady-state operation, the requirement of balanced flux linkage of the dc link inductor implies

\[
\Delta \lambda_{Sdc_{-on}} = \Delta \lambda_{Sdc_{-off}}
\]

Substitution of equations (1) and (4) into (5) will result in

\[
d_{dc} V_{dc} = \frac{3}{2} T_s \cdot MI \cdot V_m \cos \phi
\]

If the voltage transfer ratio \( R_v \) is defined to be the ratio between the magnitude of the ac line-line voltage right at the converter output, it follows

\[
R_v = \sqrt{3} V_m / V_{dc} = \frac{d_{dc}}{(\sqrt{3}/2)MI \cos \phi}
\]

Due to the fact that the CSC operating mode of the bridge is only limited to the switching interval of \( (1-d_{dc})T_s \), when the switch \( S_{dc} \) is off, the modulation index is subject to the following constraint in order to ensure the realizability of the modulation schemes.

\[
0 \leq MI < (1-d_{dc})
\]

It is worth noting the voltage transfer ratio \( R_v \) given by (7) is not limited by an upper bound since the modulation index \( MI \) can be chosen to be arbitrarily small (theoretically). However, there exists a lower bound of \( R_v \), which is given by

\[
R_{v_{min}} = \frac{d_{dc}}{(\sqrt{3}/2)(1-d_{dc})\cos \phi}
\]

A plot of the lower bound of the voltage transfer ratio under the assumption of unity power factor is illustrated in Fig. 13.

IV. MODULATION STRATEGIES

A carrier-based modulation scheme is adopted. The modulation functions for the switches \( S_{ap}, S_{bp}, S_{cp} \) are \( m_{ap}, m_{bp}, \) and \( m_{cp} \), respectively. The modulation functions for the switches \( S_{an}, S_{bn}, S_{cn} \) are \( m_{an}, m_{bn}, \) and \( m_{cn} \), respectively. These modulation functions satisfy the following constraints.

\[
\begin{align*}
    m_{ap} + m_{bp} + m_{cp} &= 1 - d_{dc} \\
    m_{an} + m_{bn} + m_{cn} &= 1 - d_{dc} \\
    m_{ap} - m_{an} &= m_a \\
    m_{bp} - m_{bn} &= m_b \tag{10} \\
    m_{cp} - m_{cn} &= m_c
\end{align*}
\]

The constraints in (10) indicate that non-unique solutions exist for the modulation functions. One set of the modulation functions are constructed as follows:

\[
\begin{align*}
    m_{ap} &= \Phi(m_a) m_a + m_0, \quad m_{an} = -\Phi(m_a) m_a + m_0 \\
    m_{bp} &= \Phi(m_b) m_b + m_0, \quad m_{bn} = -\Phi(m_b) m_b + m_0 \\
    m_{cp} &= \Phi(m_c) m_c + m_0, \quad m_{cn} = -\Phi(m_c) m_c + m_0
\end{align*}
\]

where the zero sequence \( m_0 \) is given by

\[
m_0 = \frac{1 - d_{dc} - \max[|m_a|, |m_b|, |m_c|]}{3}
\]

The function \( \Phi(\cdot) \) in (11) is defined as

\[
\Phi(x) = \begin{cases} 1 & \text{if } x \geq 0 \\ 0 & \text{otherwise} \end{cases}
\]

The plots of the zero sequence \( m_0 \) and the modulation functions are shown in Fig. 14.
Once the modulation functions are determined, the switching functions \( h_{ap}, h_{bp}, \) and \( h_{cp} \) specify the switching states of the switches \( S_{ap}, S_{bp}, \) and \( S_{cp} \) generated by comparing the modulation functions and a triangle carrier as illustrated in Fig. 15. It can be observed that during the interval of \((1-d_{dc})T_s\), when the switch \( S_{dc} \) is off, the switching functions \( h_{ap}, h_{bp}, \) and \( h_{cp} \) satisfy

\[
h_{ap} + h_{bp} + h_{cp} = 1
\]  

(14)

The switch \( S_{dc} \) is on when the switching function \( h_{dc}=1 \) during the interval of \( d_{dc}T_s \). The same comparison approach is applied to generate the switching functions \( h_{ap}, h_{bp}, \) and \( h_{cp} \) for the switches \( S_{ap}, S_{bp}, \) and \( S_{cp} \) such that they satisfy the following condition when the switching \( S_{dc} \) is off.

\[
h_{ap} + h_{bp} + h_{cp} = 1
\]  

(15)

Table I tabulates all available switching states of the converter.

### V. Simulation Results

In order to verify the operating principle described in Section III and the modulation strategy in Section IV, a detailed numerical simulation of a 5kW converter has been carried out utilizing the simulation software package Saber™.

![Fig. 14 Plots of (a) phase leg modulation functions \( m_a, m_b, \) and \( m_c \); (b) the zero sequence \( m_0 \); (c) the modulation functions \( m_{ap}, m_{bp}, \) and \( m_{cp} \) for switches \( S_{ap}, S_{bp}, \) and \( S_{cp} \), respectively; (d) the modulation functions \( m_m, m_m, \) and \( m_m \) for switches \( S_{ap}, S_{bp}, \) and \( S_{cp} \), respectively.](image)

The salient parameters of the circuit and the operating condition are listed in Table II. The LC filter is designed such that the resonant frequency is at 1 kHz, which results in 40 dB attenuation of the switching harmonics that are close to the 10 kHz. It has been well understood the filter size can be further reduced with higher switching frequency.

### Table I List of the switching states of the converter.

<table>
<thead>
<tr>
<th>State #</th>
<th>( h_{dc} )</th>
<th>( h_{ap} )</th>
<th>( h_{bp} )</th>
<th>( h_{ap} )</th>
<th>( h_{bp} )</th>
<th>( h_{ap} )</th>
<th>( h_{bp} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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</tbody>
</table>

Table II List of the salient parameters of the simulation model.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC link inductor</td>
<td>( L_{dc} )</td>
</tr>
<tr>
<td>Filter inductor</td>
<td>( L_f )</td>
</tr>
<tr>
<td>Filter capacitor</td>
<td>( C_f )</td>
</tr>
<tr>
<td>Source voltage line-line</td>
<td>( V_{source} )</td>
</tr>
<tr>
<td>Source frequency</td>
<td>( f_{source} )</td>
</tr>
<tr>
<td>DC link voltage</td>
<td>( V_{dc} )</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>( f_{carrier} )</td>
</tr>
</tbody>
</table>

The simulation the ac current flowing into the power grid, the filter capacitor voltages, the dc link inductor voltage and currents results are shown in Fig. 16a-c. Fig. 16d illustrates the phase \( a \) grid voltage and current under the unity power-factor operating condition.
VI. CONCLUSION

This paper has presented the concept of dynamic stiffness, which in turn is employed as a powerful tool to derive a family of power converters characterized by the dynamic stiffness at the boundary between the passive network and the switching network. One of the salient features of the converters with dynamic stiffness is that their expanded voltage and current transfer ratios. The proposed topologies are favorably compared to the multiple-stage cascaded solutions in the regard of reduced component count and the promising potential to improve reliability and cost competitiveness.

One of the proposed topologies has been accompanied with detailed analysis within the application of a grid-connected inverter that is capable of converting dc to high-quality ac voltages/currents compatible with the existing power grids over a wide operating input range. The detailed numerical simulation results verify the validity of the theoretical analysis and demonstrate the superb spectral performance of the modulation strategy. Due to the limited space, detailed design tradeoffs and the benchmark of the performance of the converter against the conventional solutions have not been included and will be reported in future publications.

REFERENCES


Fig. 16 Numerical simulation results: (a) three-phase ac currents into the grid; (b) three-phase voltages across each of the ac filter capacitors; (c) dc link inductor voltage and current; (d) the phase - grid voltage and current illustrating the unity power factor operation.