A Framework for Verification of SystemC TLM Programs

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Abstract:
Due to their increasing complexity, today's SoC (System on Chip) systems are subject to a variety of faults (e.g., single-event upset, component crash, etc.), thereby their verification a highly important task of such systems. However, verification is a complex task in part due to the large scale of integration of SoC systems and different levels of abstraction provided by modern system design languages such as SystemC. In this dissertation, we propose a framework to facilitate the verification of SystemC TLM programs. This framework has five steps, namely defining formal semantics, model extraction, fault modeling, model slicing, and model checking.