Achieving high energy-efficiency is a key requirement for many emerging smart sensors and portable computing systems. While digital signal processing (DSP) has been the de-facto technique for implementing ultra-low power systems, analog signal processing (ASP) provides an attractive and alternate approach that can not only achieve high energy efficiency but also high computational density. Conventional ASP techniques are based on a top-down design approach, where proven mathematical principles and related algorithms are mapped and emulated using computational primitives inherent in the device physics. An example being the translinear principle, which is the state-of-the-art ASP technique, that uses the exponential current-to-voltage characteristics for designing ultra-low-power analog processors. However, elegant formulations could result from a bottom-up approach where device and bias independent computational primitives (e.g. current and charge conservation principles) are used for designing “approximate” analog
signal processors. The hypothesis of this proposal is that many signal processing
algorithms exhibit an inherent calibration ability due to which their performance remains
unaffected by the use of “approximate” analog computing techniques.

In this research, we investigate the theory, synthesis and implementation of high
performance analog processors using a novel piecewise-linear (PWL) approximation
algorithm called margin propagation (MP). MP principle utilizes only basic conservation
laws of physical quantities (current, charge, mass, energy) for computing and therefore is
scalable across devices (silicon, MEMS, microfluidics). However, there are additional
advantages of MP-based processors when implemented using CMOS current-mode
circuits, which includes: 1) the operation of the MP processor requires only addition,
subtraction and threshold operations and hence is independent of transistor biasing (weak,
moderate and strong inversion) and robust to variations in environmental conditions (e.g.
temperature); and 2) improved dynamic range and faster convergence as compared to the
translinear implementations.

We verify our hypothesis using two analog signal processing applications: (a) design of
high-performance analog low-density parity check (LDPC) decoders for applications in
sensor networks; and (b) design of ultra-low-power analog support vector machines
(SVM) for smart sensors. Our results demonstrate that an algorithmic framework for
designing margin propagation (MP) based LDPC decoders can be used to trade-off its
BER performance with its energy efficiency, making the design attractive for applications
with adaptive energy-BER constraints. We have verified this trade-off using an analog
current-mode implementation of an MP-based (32,8) LDPC decoder. Measured results
from prototypes fabricated in a 0.5 μm CMOS process show that the BER performance of
the MP-based decoder outperforms a benchmark state-of-the-art min-sum decoder at SNR levels greater than 3.5 dB and can achieve energy efficiencies greater than 100pJ/bit at a throughput of 12.8 Mbps.

In the second part of this study, MP principle is used for designing an energy-scalable support vector machine (SVM) whose power and speed requirements can be configured dynamically without any degradation in performance. We have verified the energy-scaling property using a current-mode implementation of an SVM operating with 8 dimensional feature vectors and 18 support vectors. The prototype fabricated in a 0.5μm CMOS process has integrated an array of floating gate transistors that serve as storage for up to 2052 SVM parameters. The SVM prototype also integrates novel circuits that have been designed for interfacing with an external digital processor. This includes a novel current-input current-output logarithmic amplifier circuit that can achieve a dynamic range of 120dB while consuming nanowatts of power. Another novel circuit includes a varactor based temperature compensated floating-gate memory that demonstrates a superior programming range than other temperature compensated floating-gate memories.

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