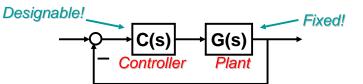


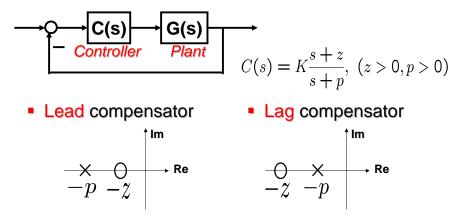
Closed-loop design by root locus



- Place closed-loop poles at desired location
 - by tuning the gain C(s)=K.
- If root locus does not pass the desired location, then reshape the root locus
 - by adding poles/zeros to C(s).

Compensation

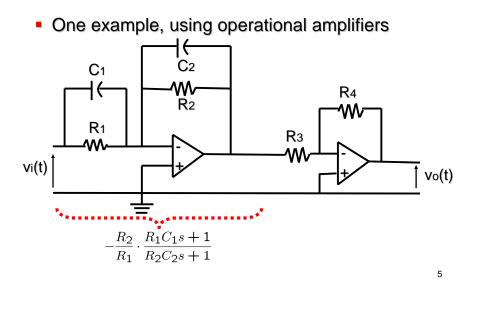
Lead and lag compensators (review)



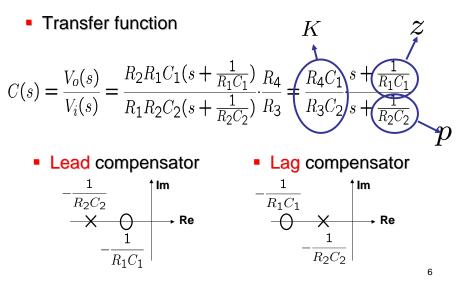
The reason why these are called "lead" and "lag" will be explained in frequency response approach (later in this course).

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Compensator realization



Compensator realization (cont'd)



Roles of lead and lag compensators

Lead compensator (Done)

• Improve transient response $C_{Lead}(s) = K_1 \frac{s+z_1}{s+p_1}$

- Improve stability
- Lag compensator (Today)

$$C_{Lag}(s) = K_2 \frac{s+z_2}{s+p_2}$$

- Reduce steady state error
- Lead-lag compensator (Today)
 - Take into account all the above issues.

$$C_{LL}(s) = C_{Lead}(s)C_{Lag}(s)$$

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Radar tracking system

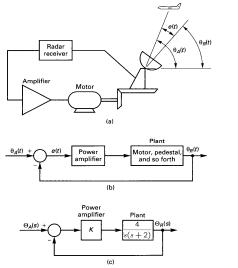


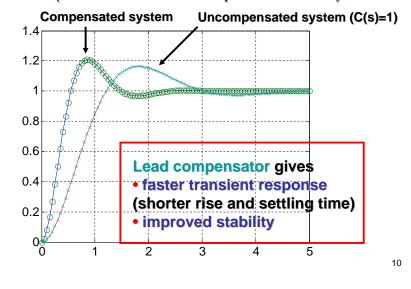




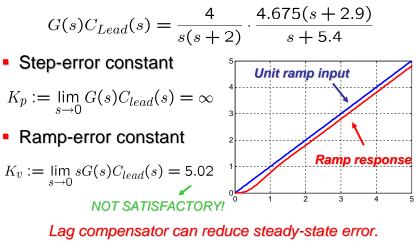
Figure 7.1 Radar tracking system

Lead-lag compensator design Consider a system G(s) $G(s) = \frac{4}{s(s+2)}$ Controller Plant Analysis of CL system for C(s)=1 Damping ratio ζ=0.5 **Desired pole** Undamped natural freq. ωn=2 rad/s Im Ramp-error constant Kv=2 $2\sqrt{3}i$ Performance specification Damping ratio ζ=0.5 Undamped natural freq. on=4 rad/s $^{-2}$ Re Ramp-error constant Kv=50 9

Comparison of step responses (after lead compensation)



Error constants (after lead compensation)



How to design lag compensator

• Lag compensator
$$C_{Lag}(s) = \frac{s+z}{s+p}$$

We want to increase ramp-error constant

$$K_v = \lim_{s \to 0} sG(s)C_{Lead}(s)C_{Lag}(s) = 5.02 \cdot \frac{z}{p} > 50$$

Take, for example, z=10p.

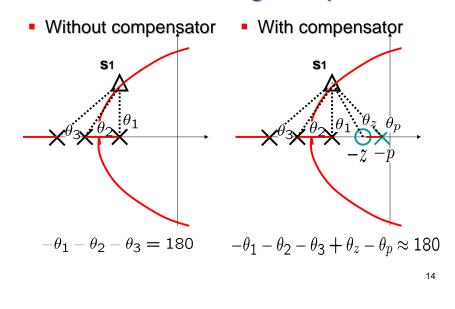
 We do not want to change CL pole location s1 so much (already satisfactory transient).

$$\left. \begin{array}{c} 1 + G(s_1)C_{Lead}(s_1) = 0 \\ C_{Lag}(s_1) \approx 1 \end{array} \right\} \longrightarrow 1 + G(s_1)C_{Lead}(s_1)C_{Lag}(s_1) \approx 0$$

Guidelines to choose z and p

- The zero and the pole of a lag compensator should be close to each other, for $C_{Lag}(s_1) \approx 1$
- The pole of a lag compensator should be close to the origin, to have a large ratio z/p, leading to a large ramp-error constant Kv.
- However, the pole of a lag compensator too close to the origin may be problematic:
 - Difficult to realize (recall op-amp realization)
 - Slow settling (due to closed-loop pole near the origin)

Root locus with lag compensator



How to design lag compensator

• For the desired CL pole $s_1 = -2 + 2\sqrt{3}j$

$$C_{Lag}(s_1) \approx 1 \iff \left| \frac{s_1 + 10p}{s_1 + p} \right| \approx 1 \quad \angle \left(\frac{s_1 + 10p}{s_1 + p} \right) \approx 0$$

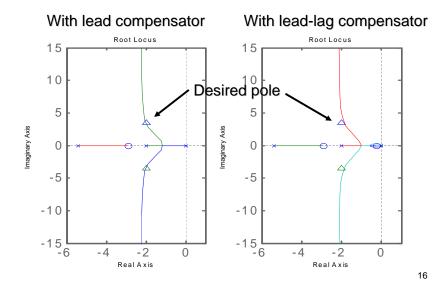
Take a small p (by trial-and-error!)

$$p = 0.025 \longrightarrow \left| \frac{s_1 + 10p}{s_1 + p} \right| = 0.97 \ \angle \left(\frac{s_1 + 10p}{s_1 + p} \right) \approx -2.88^{\circ}$$

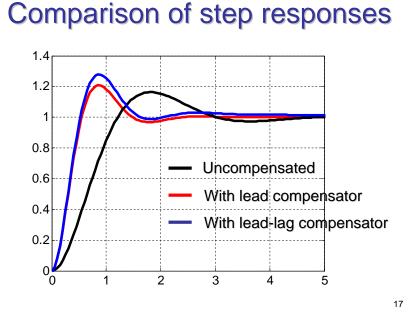
Lead-lag controller

$$C_{LL}(s) = 4.675 \frac{s+2.9}{s+5.4} \cdot \frac{s+0.25}{s+0.025}$$

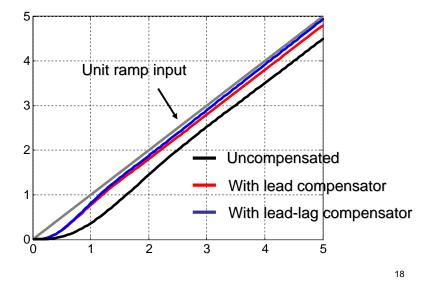
Root locus



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Comparison of ramp responses



Summary and exercises

- Controller design based on root locus
 - Lag compensator design
 - Lag compensator improves steady state error.
 - Lead-lag compensator design
 - Lead-lag compensator improves stability, transient and steady-state responses.
- Next, frequency response and Bode plot