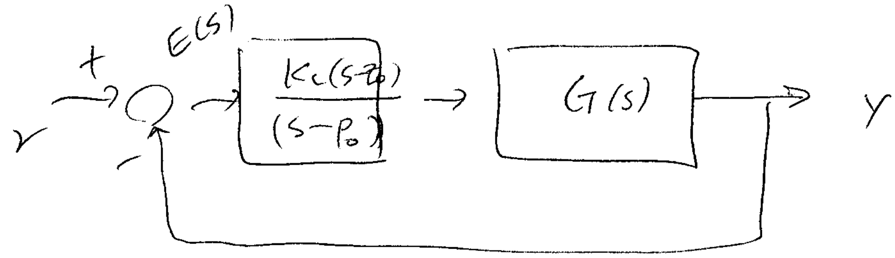
(1)

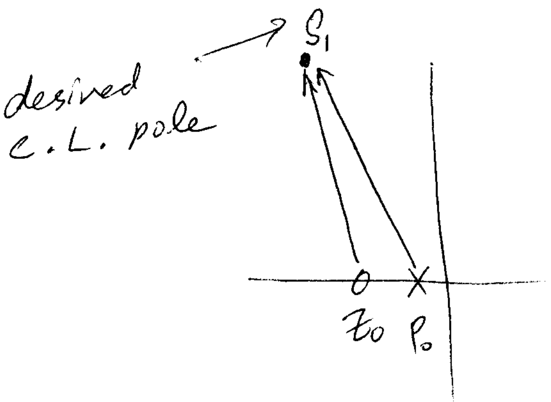
Simplified Procedure (corresponding to a request from the class)

Another way to design Phase Lag Compensator is to start with $C(s) = K_c \left(\frac{s - z_0}{s - p_0}\right)$



We will pick z_0 p_0 such that $|s_1| > |z_0|, |p_0|$ — (1)

↑ desired closed loop poles



Phase Lag

$\Rightarrow |z_0| > |p_0|$

pick also $(z_0) \simeq p_0$ so that negative angle contribution gets minimized.

C.E. $1 + C(s_1)G(s_1) = 0$

$$1 + \underbrace{K_c \frac{(s_1 - z_0)}{(s_1 - p_0)}}_{\simeq K_c} G(s_1) = 0 \Rightarrow \underbrace{1 + K_c G(s_1) = 0}$$

Step I obtain K_c ⟶ approximation

$$K_c = -\frac{1}{G(s_1)}$$

← desired C.L. pole

Step II

Calculate steady-state error (ex. step input $r(t) = 1(t)$)

$$e_{ss}^{d} = \lim_{s \to 0} sE(s) = \lim_{s \to 0} s \cdot \frac{1}{s} \frac{1}{1 + \frac{K_c(s - z_0)}{(s - p_0)} G(s)}$$

desired steady state error

$$= \frac{p_0}{K_c z_0 \, \text{DC gain } G(s)} = \boxed{\frac{p_0}{z_0 K_c} \cdot \frac{1}{G(0)}}$$

② Step III pick z_0 smaller than $|s_0|$

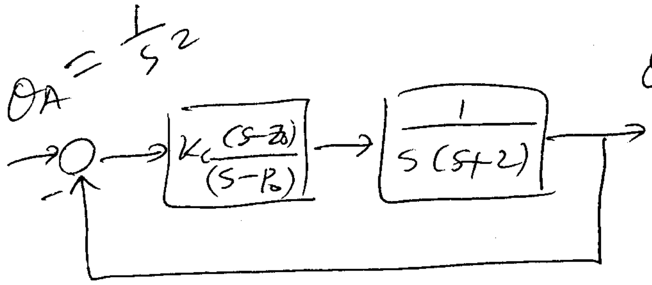
then $P_0 = e_{ss}^{d} \dfrac{z_0 k_c}{\ } G(0)$ ← DC gain of $G(s)$

This is for the unit step input $R(s) = \frac{1}{s}$ (→ P_0)

e_{ss}^{d}: customer gives you

k_c: matched according to S_1

Revisit



Step I

pick $S_1 = -1 + j \Rightarrow 1 + K_c G(s_1) = 0$

obtain $K_c = 2$

Step II

Calculate steady state error for unit ramp

$$e_{ss}^{d} = 0.2 = \lim_{s \to 0} s E(s) = \lim_{s \to 0} s \frac{1}{s^2} \left[\frac{1}{1 + \frac{K_c (s - z_0)}{(s - p_0)} \cdot \frac{1}{s(s+2)}} \right]$$

$$\frac{2}{10} = \frac{1}{k_c \frac{z_0}{P_0} \frac{1}{2}} = \frac{2P_0}{K_c z_0}$$

Step III

pick $z_0 = -0.1 \ll |S_1| = \sqrt{2}$

then $P_0 = \dfrac{K_c z_0}{10} = \dfrac{2 \cdot [-0.1]}{10}$

$= -0.02$

$$C(s) = \frac{2(s+0.1)}{(s+0.02)}$$

Final Answer.