MID-TERM EXAMINATION, ECE418 FALL SEMESTER 2006

Instructions

- Only one A4 (8’’ x 11’’) cheat sheet allowed. Use additional sheets if necessary.
- There are three questions in this exam. Only one of the problems will be counted towards your grade. If you solve more than one problem, the answer with the maximum score will be counted.
- Each question comes with hints on how to approach the problem. The hints are only suggestions and you may not choose to follow the exact steps.
- Partial credit will be provided if steps towards solving the problem are correct but the final answer is incorrect. Make sure that you indicate how you are approaching the problem.

Assumptions

- All transistors (pMOS and nMOS) have equal gate transconductance $g_m$ and drain transconductance $g_d$. The pMOS transistor is indicated by a circle at its gate.
- The wires in the diagrams are connected only where solder dots (black dots) are located.
Problem 1 (20 points)
Compute the following parameters for the circuit given below:

a) Small signal gain \( A_{\text{diff}} = \frac{\Delta V_{\text{out}}}{\Delta V_{\text{in}}^+ - \Delta V_{\text{in}}^-} \) [10 points]

b) Output voltage swing [3 points]

c) Input voltage swing [3 points]

d) Power consumption [4 points]

Hints
- First identify all current mirrors and current sources/sinks. (Remember when input current of the transistor is fixed, the gate-to-source voltage is approximately fixed)
- The key to this problem is transistor Q13 and how does voltage Vx change when the input voltage changes. Use small signal models for Q12 and Q13 to find the relationship between Vin+ and Vx.
- Identify the differential pair and use symmetry assumptions
- Once you have identified how Vx changes, trace the path of current from Q2 through the mirrors to the output stage and simplify.
Problem 2 (20 points)

For the circuit below, the size (width-to-length ratio) of transistors Q6, Q7 and Q4 is **twice** the transistors Q2, Q3, Q5. Compute the following parameters for the circuit given below:

- **e)** Small signal gain \( A_{\text{diff}} = \frac{\Delta V_{out}}{\Delta V_{in}} \)  [10 points]
- **f)** Output voltage swing.  [3 points]
- **g)** Input voltage swing  [3 points]
- **h)** Power consumption [4 points]

**Hints**
- The key to this problem is to understand why the size of Q6, Q7 and Q4 is twice that of Q5, Q3 and Q2.
- Use one of the concepts from your homework to solve for the network Q3, Q4, Q5, Q6 and Q7.
- Identify all the current mirrors and then solve for small signal gain.
Problem 3 (20 points)

Compute the following parameters for the circuit given below:

i) Small signal gain $A_{\text{diff}} = \frac{\Delta V_{\text{out}}}{(\Delta V_{\text{in}^+} - \Delta V_{\text{in}^-})}$ [10 points]

j) Output voltage swing [3 points]

k) Input voltage swing [3 points]

l) Power consumption [4 points]

Hints

- The key to this problem is to figure out what Q4 does. And how does the gate of Q4 change when $V_{\text{in}^+}$ changes?

- What is Q3 and Q4?

- Identify all current mirrors and point of symmetry (if any?).

- Why is the current through Q10 equal to $3I_b$?